INTEGRATED CIRCUITS

Semiconductors for Wireless Communications

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Applications Handbook
IC17b **1998**

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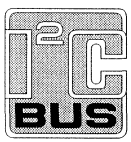
DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PREFACE

Semiconductors for Wireless Communications

Welcome to the latest edition of our Data Handbook "Semiconductors for Wireless Communications". Wireless communications is one of the fastest growing markets segments in the electronics business today. And no one has more to offer in this area than Philips Semiconductors. We supply semiconductor components for everything from cordless, cellular and paging products to exciting new applications, like wireless LAN, Personal Communications Systems (PCS), Global Positioning System (GPS), audio products, industrial control, security systems, and more.

What better place to start, therefore, with your search of wireless communication devices than with this Data Handbook. To make selections easier, we have split the book into two parts, parts a and b. In part a, you'll find IC selection charts, wireless system solutions and all our current wireless semiconductor data sheets. As a further aid, we can also supply all these data sheets on a separately available CD-ROM. To supplement this data, part b of the Data Handbook contains a selection of wireless application reports. These reports give detailed design examples, in-depth system information and practical advice on how to get the most from our wireless semiconductors.

For more information on how we can help with your wireless designs, or to speak to a local sales representative, in the U.S. call 1 800 447 1500, ext. 1253; in Europe fax +31 40 272 4825; in Asia/Pacific fax +852 319 7890, or in Japan fax +81 3 3740 5057. Or visit our worldwide web site at http://www.semiconductors.philips.com

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REPLACED/WITHDRAWN TYPES

The following type numbers were included in the previous issue of this data handbook, but are not in the current edition.

TYPE NUMBER	REASON FOR DELETION
CGY2010G	Nearest replacement: CGY2013G
CGY2011G	Nearest replacement: CGY2013G
CGY2023G	Nearest replacement: CGY2021G
NE570	Replaced by SA570
NE571	Replaced by SA571
NE572	Replaced by SA572
NE575	Replaced by SA575
NE576	Replaced by SA576
NE577	Replaced by SA577
NE578	Replaced by SA578
NE600	Replaced by SA600
NE602A	Replaced by SA602A
NE604A	Replaced by SA604A
NE605	Replaced by SA605
NE612A	Replaced by SA612A
NE614A	Replaced by SA614A
NE615	Discontinued
NE624	Replaced by SA624
NE625	Replaced by SA625
NE627	Replaced by SA627
NE630	Replaced by SA630
NE5200	Replaced by SA5200
NE5204A	Replaced by SA5204A
NE5205A	Replaced by SA5205A
NE5209	Replaced by SA5209
NE5219	Replaced by SA5219
NE/SA5750	Discontinued
NE/SA5751	Discontinued
PCA5097	Discontinued
PCD5032	Is not widely promoted
PCD5090	Discontinued
PCD5097	Is not widely promoted
PCF5075	Replaced by PCD5077
TDA8780M	Discontinued
UAA2072M	Replaced by UAA2043M

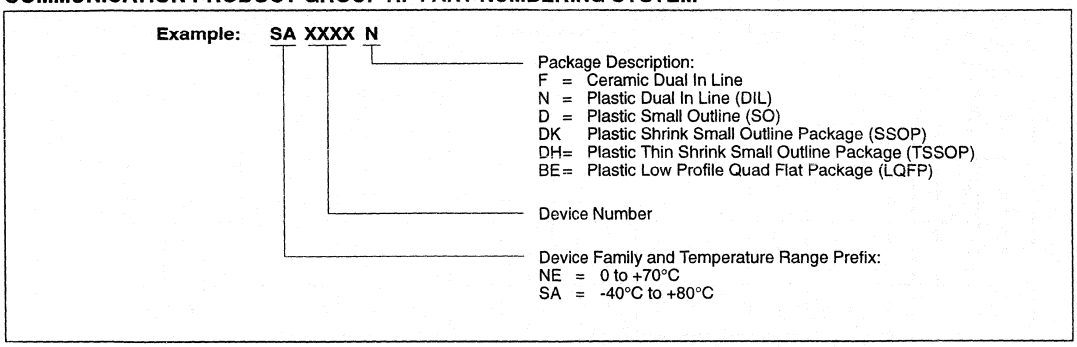
Semiconductors for Wireless Communications

Replacement list

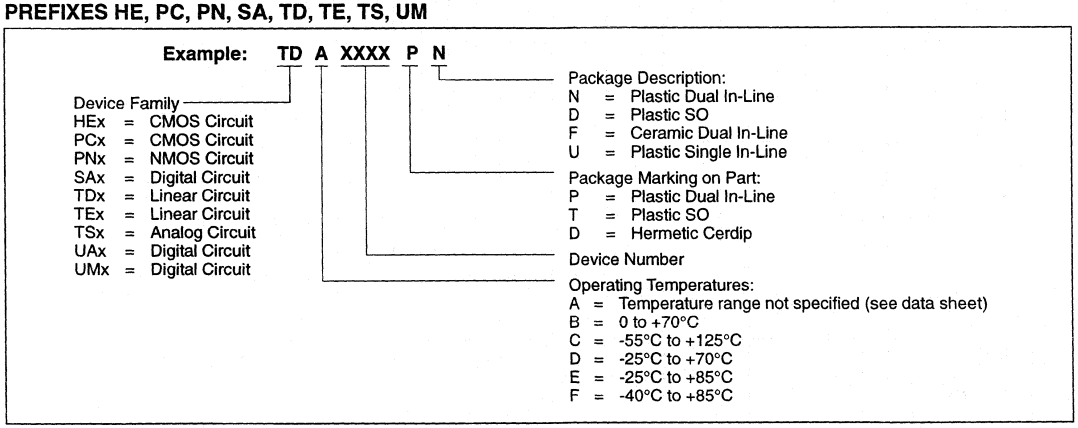
TYPE NUMBER	REASON FOR DELETION
UMA1005T	Not widely promoted
UMA1014	Not widely promoted. Nearest replacement: UMA1015AM
UMA1017M	Not widely promoted. Nearest replacement: UMA1020M
UMA1019AM	Discontinued. Nearest replacement: UMA1021M
UMA1019M	Discontinued. Nearest replacement: UMA1021M
UMA1020AM	Discontinued. Nearest replacement: UMA1021M

Ordering Information

COMMUNICATION PRODUCT GROUP RF PART NUMBERING SYSTEM



PHILIPS PRODUCTS PART NUMBERING SYSTEM
PREFIXES HE, PC, PN, SA, TD, TE, TS, UM



System Standard—Product Selector Guide

System Standard—Product Selector Guide

PRODUCTS			TARGET SYSTEMS															
Function	Type	Description	Cellular							Cordless					Wireless Data			
			(N)AMPS /(E) TACS	IS–54/–136 TDMA	IS–95 CDMA	GSM	DCS1800	PCS	PDC	CTO	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS	
RF Amplifiers											X	X						
	SA5200	Gain block–1 GHZ										X				X		
RF Front End																		
	SA611	1 GHz low volt LNA and mixer	X	X	X				X			●			●			
	SA2420	2.45GHz low voltage RF transceiver										●			●			
	SA621	1GHz low volt LNA, mixer and VCO	●	●	●				X			●						
	SA1620	Low voltage GSM RF transceiver				●												
	SA1921	Satellite/Cellular dual–band RF front–end				●												
	SA1920	PCS/Cellular dual–band RF front–end		●				●										
	UAA2073(A)M	Image reject GSM front–end				●												
	UAA2077AM	Image reject front–end for DECT											●					
	UAA2077BM	2GHz image reject front–end					●											
	UAA2077CM	2GHz image reject front–end						●										
	UAA2067G	Image reject 1.8GHz for DECT											●					
	UAA2080T	Advanced pager receiver																X
	UAA2082	Advanced pager receiver																●
Synthesizers/Prescalers																		
	UMA1015AM	Low–voltage, dual–1GHz	●								●					●		
	UMA1018M	Low–voltage, single loop–2 GHz	X		●	●												
	UMA1020M	Low–voltage, low noise–2.2 GHz						X					●	X	●			
	UMA1021M	Low–voltage, very low noise–2.2 GHz				●	●	●	●			●	●	●	●			
	UMA1022	Low voltage, very low noise–2.2 GHz				●	●	●	●			●	●	●	●			
	SA7025	Low–voltage, Fractional–N—1.04 GHz		●		X			●			●						
	SA8025A	Low–voltage, Fractional–N—1.8 GHz		●	●			●	●			●						
	SA7016	1.3GHz low voltage fractional–N synthesizer	●	●	●	●			●			●				●		
	SA8016	2.5GHz low voltage fractional–N synthesizer		●			●	●	●					●	●			
	SA7026	1.3GHz low voltage fractional–N dual frequency synthesizer	●	●	●	●			●			●				●		
	SA8026	2.5GHz low voltage fractional–N dual frequency synthesizer		●			●	●	●					●	●			

FSystem Standard—Product Selector Guide

PRODUCTS			TARGET SYSTEMS														
			Cellular							Cordless					Wireless Data		
Function	Type	Description	(N)AMPS /(E) TACS	IS–54/–136 TDMA	IS–95 CDMA	GSM	DCS1800	PCS	PDC	CTO	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS
Mixer/IF/Demod																	
	SA605	High perf/wide BW mixer FM/IF	X	X								X	X	X	X	X	
	SA606/7/8	Low–voltage, high perf mixer FM/IF	●	●						●	●					●	
	SA626	Low–voltage/Wide BW/fast RSSI										●		●			
	SA636	SA626 with Wideband data output											X		●	●	
	SA637	SA626 with Digital IF		●				●									
	SA639	Low–voltage mixer FM/IF w/switch										X	●		●		
	SA1630	Low voltage transceiver w/74 dB VGA							X			X			●		
	SA1638	Low–voltage GSM IF transceiver				●											
	SA647	IF Digital Receiver		●				●									
Power Amplifiers and Transmitters																	
	SA900	I/Q transmit modulator		●								X					
	SA910	Variable gain RF predriver amplifier	●									X					
	SA2410	2.45 GHz PA and T/R Switch													●		
	SA9025	Transmit modulator with 2.2 GHz fractional–N synthesizer integrated		●				●									
	CGY2013	GSM 4W power amplifier				●											
	CGY2021	DCS/PCS 2W power amplifier					●	●									
	CGY2030	DECT 0.5W power amplifier											●				
	CGY2032	DECT 0.5W power amplifier											●				

"●" = Recommended part–type/system solution

"x" = Alternate solution

FRONT-END, INTEGRATED CIRCUITSE

	DESCRIPTION[3]	V_{CC} (V)	I_{CC} (mA)	PINS	Pkg[2]	INPUT FREQUENCY
Image Reject Front-End Systems						
SA1920	Dual-band 800/1900 MHz LNA + IRM + IFamp.	3.6 – 3.9	HB Rx : 41.1 HB Tx : 21.3 @ 3.75 V	48	BE	869 – 960 MHz or 1.93-1.99 GHz
SA1921	Dual-band 900/1550 MHz LNA + IRM + IFamp.	3.6 – 3.9	HB Rx : 38.6 HB Tx : 18.8 @ 3.75 V	48	BE	935 – 960 MHz or 1.525 – 1.559 GHz
UAA2067G	LNA + IRM + Mod. + VCO	3 – 5.5	Rx : 24 Tx : 42 @ 3.6 V	32	BE	1.8 – 1.9 GHz
UAA2077AM	LNA + IRM	3.15 – 5.3	27 @ 4 V	20	DK	1.8 – 1.9 GHz
UAA2077BM	LNA + IRM + Tx down-convert mixer	3.6 – 5.3	Rx : 27 Tx : 14 @ 4 V	20	DK	1.8 – 2 GHz
UAA2077CM	LNA + IRM + Tx down-convert mixer	3.6 – 5.3	Rx : 36 Tx : 14 @ 3.75 V	20	DK	1.8 – 2 GHz
Image Reject Front-End Systems						
UAA2073M	LNA + IRM + Tx down-convert mixer	3.6 – 5.3	Rx : 26 Tx : 12 @ 3.75 V	20	DK	925 – 960 MHz
UAA2073AM	LNA + IRM + Tx down-convert mixer	3.6 – 5.3	Rx : 26 Tx : 12 @ 3.75 V	20	DK	925 – 960 MHz
Integrated Front-End Systems						
SA611	LNA + Mixer	2.7 – 5.5	7 mA @ 3 V @ 3 V	20	DK	LNA 1.2 GHz Mixer 1.2 GHz
SA621	LNA + Mixer + VCO	2.7 – 5.5	12/9.3[1] @ 3 V	20	DK	LNA 1.2 GHz Mixer 1.2 GHz
Mixer Systems						
SA602A	Mixer + Oscillator	4.5 – 8.0	2.4 @ 6 V	8	N, D	500 MHz
SA612A	Mixer + Oscillator	4.5 – 8.0	2.4 @ 6 V	8	N, D	500 MHz

Front-end, Integrated (high performance) — Selection guide

POWER GAIN (dB)	NOISE FIGURE (dB)	INPUT IP3 (dBm)	1 dB COMP. (dBm)	IMAGE REJECTION (dB)	INPUT IMPED.	OUTPUT IMPED.	FEATURE HIGHLIGHTS
F_{RF} = 2 GHz							
22	4.5	LB : 9 HB : 12	24 – 25	35	50 Ω	50 Ω	Dual-band 800 MHz & 1.9 GHz Tripple-mode AMPS/DAMPS/PCS
22	4.5	LB : 9 HB : 12	24 – 25	35	50 Ω	50 Ω	Dual-band 900 MHz & 1.5 GHz
30	5.8	–25	–33	34	190 Ω 0.8 pF diff.	50 Ω asym.	RF to IF DECT transceiver (DSH)
20	4.3	–17	–22	32	60 Ω 1 pF diff.	1 kΩ diff.	3.15 V, 4.3 dB DECT front-end (DSH)
20	4.3: DCS	–17	–23	32	60 Ω 1 pF diff.	1 kΩ diff.	DCS 1800 front-end
22	3.8: DCS 4.0: PCS	–17	–24	38	60 Ω 0.8 pF diff.	1 kΩ diff.	PCS1900/DCS1800 front-end
F_{RF} = 900 GHz							
23	3.25	–15	–23	37	150 Ω 1 pF diff.	1 kΩ diff.	3.6 V phase 2 GSM receiver
22	3.6	–15	–23	45	150 Ω 1 pF diff.	1 kΩ diff.	GSM high IF
F_{RF} = 900 GHz							
15/–20[1]	1.9	–5/+25[1]	–16		50 Ω	50 Ω	• Low voltage • Exellent Noise Figure • LNA Overload Mode
Mixer 1.2 GHz	7	9.5	+4	–9		50 Ω	
15/–20[1]	1.9	–5/+25[1]	–16		50 Ω	50 Ω	• Low Voltage • Excellent Noise Figure • LNA Overload Mode
7	9.5	+4	–9		50 Ω	High	• Low Phase-Noise • Internal VCO
Mixer F_{RF} = 45 MHz							
17	5.0	–13	–25		1.5 kΩ	1.5 kΩ	• Excellent Noise Figure • High Gain
17	5.0	–13	–25		1.5 kΩ	1.5 kΩ	• Excellent Noise Figure • High Gain

Front-end, Integrated (high performance) — Selection guide

	DESCRIPTION[3]	V_{CC} (V)	I_{CC} (mA)	PINS	Pkg[2]	INPUT FREQUENCY
RF Amplifiers						
SA5200	Dual Gain Stage	4.0 – 9.0	4.2/95 µA[1] @ 5 V (per) (amplif.)	8	D	DC – 1.2 GHz
SA5204A	Wideband Amp	5.0 – 8.0	25 @ 6 V	8	N, D	DC – 350 MHz
SA5205A	Wideband Amp	5.0 – 8.0	25 @ 6 V	8	N, D	DC – 550 MHz
SA5209	Variable Gain Amp	4.5 – 7.0	43 @ 5 V	16	N, D	DC – 850 MHz
SA5219	Variable Gain Amp	4.5 – 7.0	43 @ 5 V	16	N, D	DC – 700 MHz

Notes

1. Amplifier: Enabled/Disabled
2. Package Descriptions:
   a) D: = Small Outline (SO14/16/20)
   b) N: = Dual In-line (DIL)
   c) DK: = Shrink Small Outline Package (SSOP20)
   d) BE: = Low Quad Flat Package (LQFP)
3. IRM: Image Reject Mixer
   LNA: Low Noise Amplifier
   DSH: Double Superheterodyne
   diff.: differential
   asym.: asymmetrical

Front-end, Integrated (high performance) — Selection guide

POWER GAIN (dB)	NOISE FIGURE (dB)	INPUT IP3 (dBm)	1 dB COMP. (dBm)	IMAGE REJECTION (dB)	INPUT IMPED.	OUTPUT IMPED.	FEATURE HIGHLIGHTS
RF F_{RF} = 900 MHz (NE/SA 5200), 100 MHz (others)							
7.5/13.5[1] (per) (amplif.)	3.6	–1.8	+3.2		50 Ω	50 Ω	• DC to 1.2 GHz Operation • Power- Down Mode
19	6.0 (50 Ω) 4.8 (75 Ω)	–2	+4		50 Ω	50 Ω	• DC to 350 MHz Operation
19	6.0 (50 Ω) 4.8 (75 Ω)	–2	+4		50 Ω	50 Ω	• DC to 550 MHz Operation
25 (voltage)	9.3	+13 (output)	–3		1.2 Ω	60 Ω	• DC to 850 MHz Operaton • Gain Control Pin
25 (voltage)	9.3	+13 (output)	–3		1.2 Ω	60 Ω	• DC to 700 MHz Operation • Gain Control Pin

Notes

1. Amplifier: Enabled/Disabled
2. Package Descriptions:
   a) D: = Small Outline (SO14/16/20)
   b) N: = Dual In-line (DIL)
   c) DK: = Shrink Small Outline Package (SSOP20)
   d) BE: = Low Quad Flat Package (LQFP)
3. IRM: Image Reject Mixer
   LNA: Low Noise Amplifier
   DSH: Double Superheterodyne
   diff.: differential
   asym.: asymmetrical

FRONT-END, DISCRETE

SOCKET	SYSTEM FREQ. (MHz)	I_C (MA)	V_{CE} (V)	F_T (GHz)	GAIN (dB) @ 900 MHz	NOISE (dB) @ 900 MHz	GAIN (dB) @ 1.9 GHz	NOISE (dB) @ 1.9 GHz	PACKAGE				
									SOT23	SOT323	SOT343[1]	SOT353	SOT363
LNA	900	3	4.5	17	20	1	22	1.6			BFG403W		
	900 & 1900	2 – 5	3 – 12	9	17	1.2	10	1.9	BFR505	BFS505	BFG505W	BFC505	BFM505
	900 & 1900	3 – 30	3 – 12	9	17	1.2	10	1.9	BFR520	BFS520	BFG520W	BFC520	BFM520
	900 & 1900	1 – 10	2 – 4.5	22	21	1.2	29	0.9			BFG410W		
	900 & 1900	3 – 25	2 – 4.5	22	20	1.2	28	0.8			BFG425W		
Mixer	900	5 – 30	3 – 10	6	13	1.9			BFR93A	BFR93AW	BFG93AW		
	900 & 1900	2 – 5	3 – 12	9	17	1.2	10	1.9	BFR505	BFS505	BFG505W	BFE505	BFM505
	900 & 1900	3 – 30	3 – 12	9	17	1.2	10	1.9	BFR520	BFS520	BFG520W	BFE520	BFM520
	900 & 1900	1 - 10	2 – 4.5	22	21	1.2	29	0.9			BFG410W		
	900 & 1900	3 – 25	2 – 4.5	22	20	1.2	28	0.8			BFG425W		
Buffer & VCO	900	3 – 20	3 – 10	6	14	2.1			BFR92A	BFR92AW			
	900	5 – 30	3 – 10	6	13	1.9			BFR93A	BFR93AW			
	900 & 1900	2 – 5	3 – 12	9	17	1.2	10	1.9	BFR505	BFS505	BFG505W	BFC505	BFM505
	900 & 1900	3 – 30	3 – 12	8	17	1.2	10	1.9	BFR520	BFS520	BFG520W	BFC520	BFM520
	900 & 1900	1 – 10	2 – 4.5	22	21	1.2	29	0.9			BFG410W		
	900 & 1900	3 – 25	2 – 4.5	22	20	1.2	28	0.8			BFG425W		
IF	40 – 100	3 – 20	3 – 12	1.2	20 dB gain @ 100 MHz				BF547	BF547W			
	100 – 250	3 – 20	3 – 8	2.8	25 dB gain @ 250 MHz				BFS17A	BFS17W			
	>250	3 – 20	3 – 10	5	25 dB gain @ 500 MHz				BFR92A	BFR92AW			

Note

1. Typically the gain is 2 – 3 dB higher in SOT343 packages.

IF SYSTEMS

	V_{CC} (V)	I_{CC}	PINS	Pkg	INPUT FREQ. (MHz)	IF FREQ (MHz)	FRF = 45 MHz		
							INPUT SENSI-TIVITY	MIXER GAIN (dB)	INPUT IP_3 (dBm)
FM IF									
SA604A	4.5 – 8	3.3 mA @ 6 V	16	D,N	25	25	0.22(1)	-	-
SA614A	4.5 – 8	3.3 mA @ 6 V	16	D,N	25	25	0.22(1)	-	-
SA624	4.5 – 8	3.4 mA @ 6 V	16	D,N	25	25	0.22(1)	-	-
Mixer/FM IF									
SA605	4.5 – 8	5.7 mA @ 6 V	20	D,DK,N	500	25	0.22	13	–10
SA615	4.5 – 8	5.7 mA @ 6 V	20	D,DK,N	500	25	0.22	13	–10
SA625	4.5 – 8	5.8 mA @ 6 V	20	D,DK,N	500	25	0.22	13	–10
Low Voltage Mixer/FM IF									
SA606	2.7 – 7	3.5 mA @ 3 V	20	D,DK,N	150	2	0.31	17	–9
SA616	2.7 – 7	3.5 mA @ 3 V	20	D,DK,N	150	2	0.31	17	–9
SA676	2.7 – 5.5	3.5 mA @ 3 V	20	D,DK	100	2	0.45	17	–10
SA607	2.7 – 7	3.5 mA @ 3 V	20	D,DK,N	150	2	0.31	17	–9
SA608	2.7 – 7	3.5 mA @ 3 V	20	D,DK,N	150	2	0.31	17	–9
SA626	2.7 – 5.5	6.5 mA @ 3 V	20	D,DK	500	25	0.54(2)	11(2)	–16(2)
SA636	2.7 – 5.5	6.5mA @ 3V	20	D,DK	500	25	0.54(2)	11(2)	–16(2)
SA639	2.7 – 5.5	8.5 mA @ 3 V	24	DH	500	25	2.24(4)	12(4)	–12.5(4)
Low Voltage Mixer/Digital IF									
SA637	2.7 – 5.5	3.5 mA @ 3 V	20	D,DK	200	2	$\frac{-117\ dBm^3}{0.31\ \mu V}$	7	–17
SA647	2.7 – 5.5	5.9 @ 3 V	20	DK	200	2	–112 dBm		–28
SA1630	2.7 – 5.5	Tx: 26.5 Rx: 33.5 @3 V	48	BE	400				
SA1638	2.7 – 5.5	Tx: 22 Rx: 18 @3 V	48	BE	400				

RSSI RANGE (dB)	FAST RSSI	FREQ. CHECK PIN	IF FILTER MATCH (kHz)	OUTPUT OP AMPS	FEATURE HIGHLIGHTS
FM IF					
90	-	-	455	-	• High Sensitivity
80	-	-	455	-	• Wide IF BW
90	x	-	455	-	
Mixer/FM IF					
90	-	-	455	-	• High Sensitivity
80	-	-	455	-	• High Input Frequency
90	x	-	455	-	
Low Voltage Mixer/FM IF					
90	-	-	455	Audio Op Amp RSSI Op Amp	• High Sensitivity
80	-	-	455	Audio Op Amp RSSI Op Amp	• Low Power
70	-	-	455	Audio Op Amp RSSI Op Amp	• Audio Op Amp RSSI Buffered
90	-	x	455	Audio Op Amp RSSI Op Amp	• Audio/RSSI Output Op Amps
90	-	x	455	Audio Buffered RSSI Op Amp	• Power-Down Mode (SA626/636/639)
90	x	-	10.7 MHz	Audio Buffered RSSI Op Amp	
90	x	-	10.7 MHz	RSSI Op Amp	
90	x	-	10.7 MHz	Audio Buffered RSSI Op Amp Post-detect Amp Data Switch	
Low Voltage Mixer/Digital IF					
90	x	-	455 kHz	RSSI Op Amp	
90	x	-	455 kHz	RSSI Op Amp	• Improved mixer gain and sensetivity over SA637
					• Wireless LAN using DSSS modulation • Digital IF Gain Control of 70 dB in steps of 2 dB
					• GSM 900 Mhz • DCS 1.8 GHz • uadrature up & down mixer stage

Notes

1. Measured with a Philips MESA602A mixer prior to the IF input.
2. Measured at f_{RF} = 240 MHz.
3. Represents the –3 dB Input Limiting point (dBm). Also shown in μV units into a 50 Ω matching network.
4. Measured at f_{RF} = 110 MHz.

Temperature Ranges
SA: –40 to +85 °C.

Package DescriptionsIF Filter Match
D:
Small Outline - 16 DK: Shrink Small Outline Package (SSOP) - 20455 kHz = 1.5 kΩ
Small Outline - 20 N: Dual In-Line Plastic - 16, 2010.7 MHz = 330 Ω.

IF Filter Match
455 kHz = 1.5 kΩ
10.7 MHz = 330 Ω.

FREQUENCY SYNTHESIZERS

	V_{CC}	I_{CC}	PINS	Pkt	MAX RF/INPUT FREQ.	CHANNEL SPACING	FRACTIONAL -N DIVIDER	AUXILIARY SYNTHE-SIZER	APPLICA-TIONS
Fractional-N Frequency Synthesizers									
SA 7016DH	2.7 to 5.5 V	5 mA @ 3 V	16	TSSOP 16	1.3 GHz		x		IS-54/-136, IS-95, PDC, GSM digital cellular
SA 7025DK	2.7 to 5.5 V	7.5 mA @ 3 V	20	SSOP 20	1.0 GHz (main) 150 MHz (aux)		x	x	IS-54/-136, IS-95, PDC, GSM digital cellular
SA 7026DK	2.7 to 5.5 V	6.5 mA @ 3 V	20	SSOP 20	1.3 GHz (main) 550 MHz (aux)		x	x	IS-54/-136, IS-95, PDC, GSM digital cellular
SA 8016DH	2.7 to 5.5 V	6.5 mA @ 3 V	16	TSSOP 16	2.5 GHz		x		ISM band, IS-54/-136, IS-95, PDC, GSM digital cellular
SA 8025ADK	2.7 to 5.5 V	11 mA @ 3 V	20	SSOP 20	1.8 GHz (main) 150 MHz (aux)		x	x	PHS digital cordless, U.S. PCS, PDC digital cellular
SA 8026DK	2.7 to 5.5 V	8.5 mA @ 3 V	20	SSOP 20	2.5 GHz (main) 550 MHz (aux)		x	x	ISM band, IS-54/-136, IS-95, PDC, GSM digital cellular

Frequency synthesizers — Selection guide

	V_{CC}	I_{CC}	PINS	Pkt	MAX RF/INPUT FREQ.	CHANNEL SPACING	FRACTIONAL -N DIVIDER	AUXILIARY SYNTHE-SIZER	APPLICA-TIONS
Frequency Synthesizers									
UMA 1015M	2.6 to 5.5 V	9 mA @ 3 V	20	SSOP 20	1.1 GHz 1.1 GHz	5 – 1000 kHz		x (dual)	AMPS/TA CS cellular CT1/CT2 cordless
UMA 1015AM	2.7 to 5.5 V	8.7 mA @ 3 V	20	SSOP 20	1.1 GHz	5 – 1000 kHz		x (dual)	AMPS/TA CS cellular lower cost replaceme nt of UMA 1015M
UMA 1018M	2.7 to 5.5 V	10 mA @ 5.5 V	20	SSOP 20	1250 MHz (main) 300 MHz (aux)	10 – 2000 kHz		x	GSM digital cellular
UMA 1020M	2.7 to 5.5 V	12 mA @ 5.5 V	20	SSOP 20	2400 MHz (main) 300 MHz (aux)	10 – 2000 kHz		x	DECT digital cordless, DCS 1800, PHS
UMA 1021M	2.7 to 5.5 V	10 mA @ 5.5 V	20	SSOP 20	2200 MHz	10 – 2000 kHz			GSM, WLAN, DECT digital cordless, DCS 1800, PHS
UMA 1022M	2.7 to 5.5 V	13 mA @ 3 V	20	SSOP 20	2200 MHz (main) 500 MHz (aux)	10 – 2000 kHz		x	900 MHz & 2 GHz applic-ations

Frequency synthesizers — Selection guide

	V_{CC}	I_{CC}	PINS	Pkt	MAX INPUT FREQ.	MAX COM-PARE FREQ.	INPUT SENSITIVITY	DIVIDE RATIO
Prescalers								
SA 701N,D	2.7 to 6 V	4.5 mA @ 3 V	8	DIP, S08	1.1 GHz	65 kHz/ 270 kHz	–35 dBm	128/129, 64/65
SA 702N,D	2.7 to 6 V	4.5 mA @ 3 V	8	DIP, S08	1.1 GHz	1000 kHz	–35 dBm	64/66/72

TRANSMITTERS ICs

TYPE NUMBER	FREQUENCY RANGE (OUTPUT) (MHz)	FREQUENCY RANGE (SYNTHESIZER) (MHz)	SUPPLY VOLTAGE (V)	I_{CC} (FULL POWER) (mA)	DIFFERENTIAL OUTPUT (dBm)	TRANSMIT OFFSET FREQUENCY (MHz)	PACKAGE	FEATURE HIGHLIGHTS
CELLULAR								
SA900	820 – 860 (AMPS) 820 – 920 (Dual)	N/A	4.5 – 5.1	42 (AMPS) 68 (Dual)	2	90 – 140	LQFP48	BiCMOS I/Q transmit RF modulator with on-chip crystal osc. and VCO
SA9025	820 – 920 (Dual) *1.840 – 1.920 (PCS) with ext. up-conv.*	800 – 2.200	3.6 – 3.9	95 (AMPS) 52(Dual)	11	90 – 180	LQFP48	Higly integrated I/Q transmit RF- modulator with 2.2 GHz dual synth. for 800 & 1900 Tripple mode TDMA

MMICs AMPLIFIERS

TYPE NUMBER	FREQUENCY BAND	SUPPLY VOLTAGE (V)	LOAD POWER (W)	OUTPUT POWER (dBm)	POWER GAIN (dB) MIN.	EFFICIENCY (%)	PACKAGE	FEATURE HIGHLIGHTS
CELLULAR								
CGY2021G	1.71 – 1.785 or 1.85 – 1.91 GHz	4.8	3.2	34	34	55	LQFP48	GaAs MMIC 2 W DCS/PCS Power Amplifier
CGY2013G	880 – 915 MHz	3.6	4	35.5	35.5	45	LQFP48	GaAs MMIC 4 W GSM Power Amplifier
SA910	820 – 905 MHz	2.7 – 5.5	0.5	24	32	35	SSOP20	BiCMOS Low-voltage 900 MHz variable gain pre-amplifier
CORDLESS								
CGY2030M	1.88 – 1.90 GHz	3.6	0.5	27	27	40	SSOP16	GaAs MMIC 500 mW amplifier
CGY2032TS	1.88 – 1.90 GHz	3.6	0.5	27	27	50	SSOP16	GaAs MMIC 500 mW amplifier
WLAN (ISM band)								
SA2410	2.4 – 2.5 GHz	3.0 – 5.5		18.5	29	25	TQFP32	2.5 GHz power amplifier and T/R switch for WLAN (ISM-band)

MODULE AMPLIFIERS

TYPE	FREQUENCY BAND (MHz)	SUPPLY VOLTAGE (V)	MIN. LOAD POWER (W)	DRIVE POWER (mW)	MIN. POWER GAIN (dB)	MIN./TYP. EFFICIENCY (%)	PACKAGE	PACKAGE THICKNESS (mm)
ANALOG CELLULAR - AMPS								
BGY115A	824 – 849	6	1.2	2	27.8	45/50	SOT321	4
BGY118A	824 – 849	4.8	1.2	2	27.8	50/55	SOT321	4
BGY119A	824 – 849	4.8	1.2	2	27.8	50/55	SOT359	3
BGY122A	824 – 849	4.8	1.2	2	27.8	50/55	SOT388	2
BGY120A[1]	824 – 849	3.6	1.2	1	30.8	50/55	NO388	2
ANALOG CELLULAR - (E)TACS								
BGY115B	872 – 905	6	1.2	2	27.8	45/50	SOT321	4
BGY118B	872 – 905	4.8	1.2	2	27.8	50/55	SOT321	4
BGY119B	872 – 905	4.8	1.2	2	27.8	50/55	SOT359	3
BGY122B	872 – 905	4.8	1.2	2	27.8	50/55	SOT388	2
BGY120B[1]	872 – 905	3.6	1.2	1	30.8	50/55	NO388	2
ANALOG CELLULAR - SPREAD SPECTRUM								
BGY115D	902 – 928	6	1.2	2	27.8	45/50	SOT321	4
BGY118D	898 – 928	4.8	1.2	2	27.8	50/55	SOT321	4
BGY119D	898 – 928	4.8	1.2	2	27.8	50/55	SOT359	3
BGY122D[1]	898 – 928	4.8	1.2	2	27.8	50/55	SOT388	2
DIGITAL CELLULAR - GSM								
BGY205	880 – 915	6	3.5	2	32.5	45 (typ.)	SOT321B	3
BGY204	880 – 915	4.8	3.2	2	32.5	45 (typ.)	SOT321B	3
BGY206	880 – 915	4.8	3	3	30	45 (typ.)	SOT388	3
BGY240[1]	880 – 915	3.5	3	1	35	45	SOT388	2

Note

1. Objective specification

DISCRETE AMPLIFIERS

TYPE NUMBER	FREQUENCY (MHz)	SUPPLY VOLTAGE (V)	LOAD POWER (W)	POWER GAIN (dB) MIN.	EFFICIENCY (%)		THERMAL RESISTANCE[3] (K/W)	PACKAGE
					MIN.	TYP.		
ANALOG CELLULAR								
BLT80	900	7.5	0.8	6	60	67	22[4]	SOT223
BLT81	900	7.5	1.2	6	60	70	32[5]	SOT223
BLT80	900	6.0	0.8	7 (typ.)		70	22[4]	SOT223
BLT81	900	6.0	1.2	6.5 (typ.)		70	32[5]	SOT223
BLT70	900	4.8	0.6	6	60		39[6]	SOT223
BLT71	900	4.8	1.2	6	60		24[7]	SOT223
BLT71/8	900	4.8	1.2	11	55	63	50	SOT96
BLT61[2]	900	3.6	1.2	10	50	63	35[8]	SOT96 (SO8pl)
DIGITAL CELLULAR/CORDLESS								
BFG540W	900	6	18 dBm	18				SOT343
BFG540W	1900	3.6	14 dBm	11				SOT343
BFG10W/x	900	6	28 dBm	10				SOT343
BFG10W/x	1900	3.6	20 dBm	6				SOT343
BFG11W/x	1900	3.6	26 dBm	6				SOT343
BFG21W	1900	3.6	0.4	11	50			SOT343
BLT82	900	6.0	3.5	8	50	65	32[9]	SOT96 (SO8pl)

APPLICATION	SUPPLY VOLTAGE (V)	LOAD POWER (W)	1st STAGE	2nd STAGE	3rd STAGE
Analog	6.0	1.2	BFG540W/x	BLT80	BLT81*
	4.8	1.2	BFG540W/x	BLT70	BLT71
	3.6	1.2	BFG520W/x	BFG10W/x	BLT61
	4.8	1.2	BFG10W/x	BLT71/8	
GSM	6.0	3.5	BFG520W/x	BFG10W/x	BLT82
DECT, PHS	3.6	0.4	BFG540/x BFG540W/x BFG425W	BFG10/x BFG10W/x BFG21W	BFG11/x BFG11W/x

Notes

1. Objective specification
2. Preliminary specification
3. Junction to soldering joint
4. P_{tot} = 2 W, T_g = 131 °C
5. P_{tot} = 2 W, T_g = 110 °C
6. P_{tot} = 2 W, T_g = 95 °C
7. P_{tot} = 3.5 W, T_g = 90 °C
8. P_{tot} = 2 W, T_g = 115 °C
9. P_{tot} = 1.9 W, T_g = 115 °C
10. P_{tot} = 1.9 W, T_g = 115 °C
11. P_{tot} = 1 W, T_g = 130 °C.

BASEBAND PROCESSORS

	PART TYPE	APPLICATION	V_{DD}	I_{DD}	PACKAGE
PCD5041	BMC (Burst Mode Controller)	DECT	2.7 – 6.0	15 mA Typ. Active	64-Pin QFP
PCD5042	BMC (Burst Mode Controller)	DECT	2.7 – 6.0	15 mA Typ. Active	64-Pin QFP
PCD5043	BMC (Burst Mode Controller)	DECT	2.7 – 6.0	15 mA Typ. Active	64-Pin QFP
PCD5091/2/3/4/5	Baseband Processor	DECT	2.7 – 3.6	--	QFP 100 LQFP 100
PCD5096	Universal Codec	DECT ISDN	2.7 – 3.6	--	QFP 44
PCF5083	Signal Processor	GSM/DCS/PCS	2.7 – 3.6	--	128-Pin LQFP
PCF507X	Baseband & Audio Interface	GSM/DCS/PCS	2.7 – 3.6	--	80-Pin LQFP
P90CL301	16-bit Low Voltage Micro Controller	GSM/DCS/PCS	2.7 – 3.6	--	
PCF5077	Power Amplifier Controllers	GSM/DCS/PCS	2.7 – 5.5	--	SSOP16
SA5752	Audio Companding VOX and Amplifier	AMPS TACS	2.7 – 5.5	3.1 mA Typ. 125 µA Stdby	20-Pin SOL 20-Pin SSOP
SA5753	Audio Filter and Control	AMPS TACS	3.0 – 5.5	1.7 mA Typ. 600 µA Stdby	20-Pin SOL 20-Pin SSOP
UMA1002	Data processor for cellular radio	AMPS TACS	2.7 – 5.5	0.8 mA Typ.	28-Pin SOL 32-Pin LQFP
PCF5001	POCSAG decoder	PAGERS	1.5 – 6.0	60 µA Typ.	28-Pin Mini-Pack 32-Pin QFP
PCD5002	APOC1/POCSAG decoder	PAGERS	1.5	50 µA Typ.	32-Pin LQFP
PCD5003	Advanced POCSAG paging decoder	PAGERS	1.5 – 6.0	50 µA Typ. (ON) 25 µA Typ. (OFF)	32-Pin LQFP
PCD5008	FLEX decoder	PAGERS	1.8 – 3.3	6.8 µA Typ.	32-Pin LQFP

COMPANDORS

	V_{CC}	I_{CC}	PINS	PACKAGES	ALC	REFERENCE VOLTAGE	UNITY GAIN	POWER DOWN	KEY FEATURES	APPLICATIONS
SA570	6 – 24 V	3.2 mA	16	D, F, N	Both channels	Fixed 1.8 V	775 mVms	No	-Excellent unity gain tracking error -Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
SA571	6 – 18 V	3.2 mA	16	D, F, N	Both channels	Fixed 1.8 V	775 mVms	No	-Excellent unity gain tracking error -Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
SA572	6 – 22 V	6 mA	16	D, F, N	Both channels	Fixed 2.5 V	100 MVms	No	-Independent attack & release time -Good THD -Needs an ext summing op amp	High Performance Audio Circuits "Hi-Fi Studio Quality"
SA575	3 – 7 V	3 – 5.5 mA(1)	20	D, DK, N	Right channels	$V_{CC}/2$	100 mVms	No	-2 Uncommitted on-chip op amps available -Low voltage	Consumer Audio Audio Circuits "Commercial Quality"
SA576	2 – 7 V	1 – 3 mA(1)	14	D, N	Right channels	$V_{CC}/2$	100 mVms	No	-Low power -Low external component count	Battery Powered Systems "Commercial Quality"
SA577	2 – 7 V	1 – 2 mA(1)	14	D, N	Right channels	$V_{CC}/2$	10 mV to 1 V(ms)	No	-Low power -Programmable unity gain	Battery Powered Systems "Commercial Quality"

SA578	2 – 7 V	1 – 2 mA[1]	16	D, N	Right channels	$V_{CC}/2$	10 mV to 1 V(ms)	Yes (170 µA)	-Low power -Programmable unity gain -Power down -Mute function summing capability (DTMF) -600 Ω Drive Capability	Battery Powered Systems "Commercial Quality"

Note

1. SA5752/5753 are also Excellent Audio Processor Components fro High Performance Cordless and Cellular Applications that include the Companding Function.
   ICC varies with VCC.
   Packages include: SA –40 to +80 °C; N: Plastic DIP; D: Plastic SO; F: Cer DIP; DK: SSOP (Shrink Small Outline Package).
   Applications include: Cordless Phones, Cellular Phones, Wireless Mics, Modems, Consumer Audio and Two-way Communications.

FIRST GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 3.5 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE					
	LEADED	SURFACE-MOUNT				
	SOT54	SOT23	SOT89	SOT143	SOT223	SOT323
(1)		BFT25				
(2)		BF747 BF547				BF547W
(3)	BF689K BF763	BFS17				BFS17W
(4)		BFS17A		BFG17A		
(5)		BFR53				
(6)			BFQ17		BFG16A	

SECOND GENERATION WIDEBAND TRANSISTORS (f_T up to 6 GHz)

f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE					
		CERAMIC	SURFACE-MOUNT				
		SOT122	SOT23	SOT89	SOT143 (note 1)	SOT223	SOT323
(7)	NPN		BFR92(A)		BFG92A (/X)(/XR)		BFR92AW
	PNP		BFT92				BFT92W
(8)	NPN		BFR93(A)		BFG93A (/X)(/XR)	BFG94	BFR93AW
(9)	PNP		BFT93				BFT93W
(10)	NPN		BFR106	BFQ19		BFG97	
	PNP			BFQ149		BFG31	
(11)	NPN	BFQ34		BFQ18A		BFG35	
(12)	NPN	BFQ68					
(13)	NPN	BFQ136					

Note

1. SOT143 package is available with alternative pinning.
   European pinning - no type number suffix; USA pinning - suffix /X; Japanese pinning - suffix /XR.
   Brackets around the suffixes (/X) and (/XR) denote pinning options. No brackets means no options,
   (e.g. BFG10W/X: only available with USA pinning).

THIRD GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 8 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE				
	CERAMIC	SURFACE-MOUNT			
	SOT172	SOT23	SOT143 (note 1)	SOT223	SOT323
(14)		BFQ67	BFG67 (/X)(/XR)		BFQ67W
(15)			BFG197 (/X)(/XR)	BFG198	
(16)	BFQ135			BFG135	
(17)	BFQ270				

Note

1. SOT143 package is available with alternative pinning.
   European pinning - no type number suffix; USA pinning - suffix /X; Japanese pinning - suffix /XR.
   Brackets around the suffixes (/X) and (/XR) denote pinning options. No brackets means no options,
   (e.g. BFG10W/X: only available with USA pinning).

FOURTH GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 10 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE							
	CERAMIC	SURFACE-MOUNT						
	SOT172	SOT23	SOT143 (note 1)	SOT223	SOT323	SOT343 (note 1)	SOT353	SOT363
(18)		BFT25A	BFG25A/X		BFS25A	BFG25AW (/X)(/XR)		
(19)		BFR505	BFG505 (/X)(/XR)		BFS505	BFG505W (/X)(/XR)	BFC505 BFE505	BFM505
(20)		BFR520	BFG520 (/X)(/XR)		BFS520	BFG520W (/X)(/XR)	BFC520 BFE520	BFM520
(21)		BFR540	BFG540 (/X)(/XR)	BFG541	BFS540	BFG540W (/X)(/XR)		
(22)			BFG590 (/X)(/XR)	BFG591		BFG590W (/X)(/XR)		
(23)	BFQ621		BFG10(/X)			BFG10W/X		
(24)			BFG11(/X)			BFG11W/X		

Note

1. SOT143 and SOT343 packages are available with alternative pinning.
   European pinning - no type number suffix; USA pinning - suffix /X; Japanese pinning - suffix /XR.
   Brackets around the suffixes (/X) and (/XR) denote pinning options. No brackets means no options,
   (e.g. BFG10W/X: only available with USA pinning).

FIFTH GENERATION NPN WIDEBAND TRANSISTORS (f_T up to 25 GHz)

f_T / I_C CURVE (see Fig.1)	PACKAGE
	SURFACE-MOUNT
	SOT343
(25)	BFG403W
(26)	BFG410W
(27)	BFG425W
(28)	BFG21W

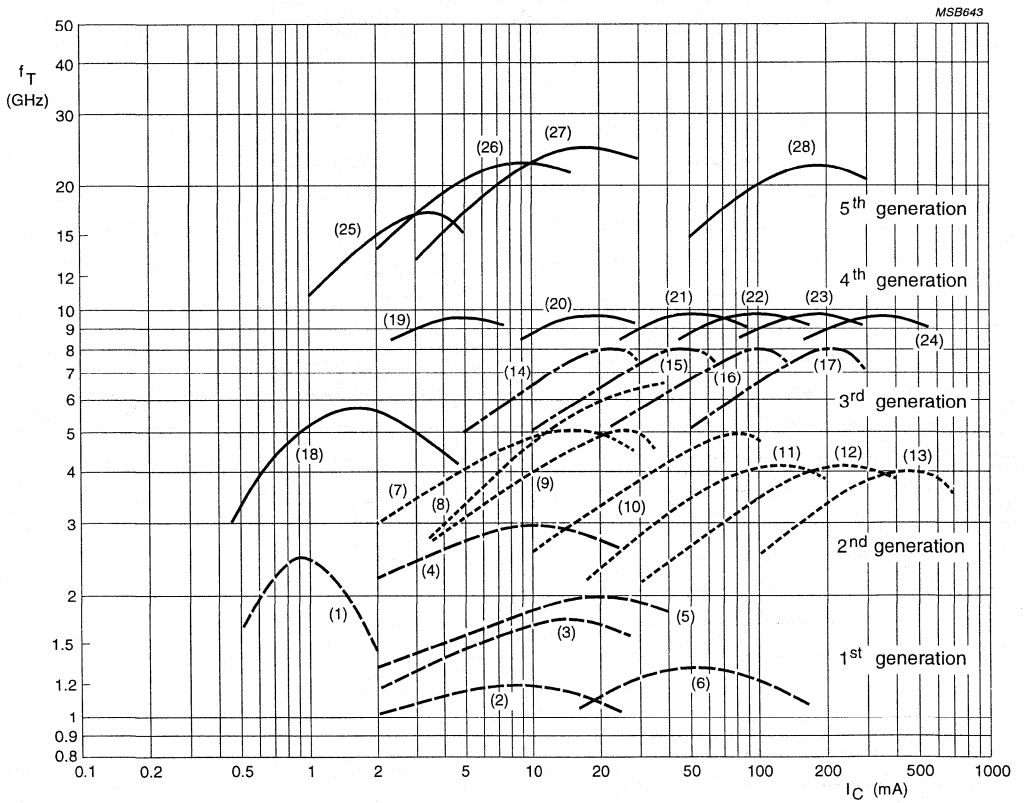


Fig.1 Transition frequency as a function of collector current for the five generations of RF bipolar wideband transistors.

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BF547	(2)	NPN	SOT23	20	50	300
BF547W	(2)	NPN	SOT323	20	50	300
BF689K	(3)	NPN	SOT54	15	25	360
BF747	(2)	NPN	SOT23	20	50	300
BF763	(3)	NPN	SOT54	25	25	360
BFC505	(19)	NPN	SOT353	8	18	500
BFC520	(20)	NPN	SOT353	8	70	1000
BFE505	(19)	NPN	SOT353	8	18	500
BFE520	(20)	NPN	SOT353	8	70	1000
BFG10(/X)	(23)	NPN	SOT143	8	250	250
BFG10W/X	(23)	NPN	SOT343	10	250	400
BFG11(/X)	(24)	NPN	SOT143	8	500	400
BFG11W/X	(24)	NPN	SOT343	8	500	760
BFG16A	(6)	NPN	SOT223	25	150	1000
BFG17A	(4)	NPN	SOT143	15	50	300
BFG25A/X	(18)	NPN	SOT143	5	6.5	32
BFG25AW(/X)(/XR)	(18)	NPN	SOT343	5	6.5	500
BFG31	(10)	PNP	SOT223	15	100	1000
BFG35	(11)	NPN	SOT223	18	150	1000
BFG67(/X)(/XR)	(14)	NPN	SOT143	10	50	380
BFG92A(/X)(/XR)	(7)	NPN	SOT143	15	25	400
BFG93A(/X)(/XR)	(8)	NPN	SOT143	12	35	300
BFG94	(8)	NPN	SOT223	12	60	700
BFG97	(10)	NPN	SOT223	15	100	1000
BFG135	(16)	NPN	SOT223	15	150	1000
BFG197(/X)(/XR)	(15)	NPN	SOT143	10	100	350
BFG198	(15)	NPN	SOT223	10	100	1000
BFG403W	(25)	NPN	SOT343	4.5	3.6	16
BFG410W	(26)	NPN	SOT343	4.5	12	54
BFG425W	(27)	NPN	SOT343	4.5	30	135
BFG505(/X)(/XR)	(19)	NPN	SOT143	15[1]	18	150
BFG505W(/X)(/XR)	(19)	NPN	SOT343	15[1]	18	500
BFG520(/X)(/XR)	(20)	NPN	SOT143	15[1]	70	300

Note

1. V_{CES}.

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BF547	1.2		20	100								
BF547W	1.2		20	100								
BF689K	1.8	4		100	3	16[3]	200					
BF747	1.2		20	100								
BF763	1.8	5		800								
BFC505	7.3	1.8		900	3.5		2000					
BFC520	7	1.3		900								
BFE505	9	1.2		900	1.9		2000					
BFE520	9	1.1		900	1.9		2000					
BFG10(/X)			7[3]	1900								
BFG10W/X			10[2][3]	900		7[3]	1900					
BFG11(/X)			5[3]	1900								
BFG11W/X						6[2][3]	1900					
BFG16A	1.5		10	500								
BFG17A	2.8	2.5	15	800								
BFG25A/X	5	1.8	18	1000								
BFG25AW(/X)(/XR)	5	2	16	1000								
BFG31	5		16	500		12	800	550			70	10
BFG35	4		15	500		11	800	750			100	10
BFG67(/X)(/XR)	8	1.7	17	1000	2.5	10	2000					
BFG92A(/X)(/XR)	5	2	16	1000	3	11	2000					
BFG93A(/X)(/XR)	6	1.7	16	1000	2.3	10	2000					
BFG94	6	2.7		500	3	13.5	1000	500	21.5	34	45	10
BFG97	5.5	2	16	500		12	800	700			70	10
BFG135	7		16	500		12	800	850			100	10
BFG197(/X)(/XR)	7.5	2.3	16	1000		10	2000					
BFG198	8		18	500		15	800	700			70	8
BFG403W	17	1		900	1.6		2000			6	1	1
BFG410W	22	0.9		900	1.2		2000			15	10	2
BFG425W	25	0.8		900	1.2		2000			22	25	2
BFG505(/X)(/XR)	9	1.6	20	900	1.9	13	2000		4	10	5	6
BFG505W(/X)(/XR)	9	1.6	19	900	1.9	12	2000		4	10	5	6
BFG520(/X)(/XR)	9	1.6	19	900	1.9	13	2000	275	17	26	20	6

Notes

1. At d_{im} = –60 dB, measured according to DIN45004B, par. 6.3: 3-tone test.
2. Minimum value.
3. Power gain G_p.

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFG520W(/X)(/XR)	(20)	NPN	SOT343	15[1]	70	500
BFG540(/X)(/XR)	(21)	NPN	SOT143	15[1]	120	500
BFG540W(/X)(/XR)	(21)	NPN	SOT343	15[1]	120	500
BFG541	(21)	NPN	SOT223	15[1]	120	650
BFG590(/X)(/XR)	(22)	NPN	SOT143	15	200	400
BFG590W(/X)(/XR)	(22)	NPN	SOT343	15	200	500
BFG591	(22)	NPN	SOT223	15	200	2000
BFM505	(19)	NPN	SOT363	8	18	500
BFM520	(20)	NPN	SOT363	8	70	1000

Note

1. V_{CES}.

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFG520W(/X)(/XR)	9	1.6	17	900	1.85	11	2000	275	17	26	20	6
BFG540(/X)(/XR)	9	1.9	18	900	2.1	11	2000	500	21	34	40	8
BFG540W(/X)(/XR)	9	1.9	16	900	2.1	10	2000	500	21	34	40	8
BFG541	9	1.9	15	900	2.1	9	2000	500	21	34	40	8
BFG590(/X)(/XR)	5		13	900		7.5	2000					
BFG590W(/X)(/XR)	5		13	900		7.5	2000		21		80	5
BFG591	7		13	900		7.5	2000					
BFM505	9	1.4	17	900	1.9	10	2000					
BFM520	9	1.7	15	900	1.9	9	2000					

Note

1. At $d_{im} = -60$ dB, measured according to DIN45004B, par. 6.3: 3-tone test.

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFQ17	(6)	NPN	SOT89	25	150	1000
BFQ18A	(11)	NPN	SOT89	18	150	1000
BFQ19	(10)	NPN	SOT89	15	100	1000
BFQ34	(11)	NPN	SOT122	18	150	2700
BFQ67	(14)	NPN	SOT23	10	50	300
BFQ67W	(14)	NPN	SOT323	10	50	300
BFQ68	(12)	NPN	SOT122	18	300	4500
BFQ135	(16)	NPN	SOT172	19	150	2700
BFQ136	(13)	NPN	SOT122	18	600	9000
BFQ149	(10)	PNP	SOT89	15	100	1000
BFQ270	(17)	NPN	SOT172	19	500	10000
BFQ540	(21)	NPN	SOT89	12	120	1200
BFQ621	(23)	NPN	SOT172	16	150	800
BFR53	(5)	NPN	SOT23	10	50	250
BFR92	(7)	NPN	SOT23	15	25	300
BFR92A	(7)	NPN	SOT23	15	25	300
BFR92AW	(7)	NPN	SOT323	15	25	300
BFR93	(8)	NPN	SOT23	12	35	300
BFR93A	(8)	NPN	SOT23	12	35	300
BFR93AW	(8)	NPN	SOT323	12	35	300
BFR94A	(8)	NPN	SOT122	25	150	3500
BFR106	(10)	NPN	SOT23	15	100	500
BFR505	(19)	NPN	SOT23	15[1]	18	150
BFR520	(20)	NPN	SOT23	15[1]	70	300
BFR540	(21)	NPN	SOT23	15[1]	120	480
BFS17	(3)	NPN	SOT23	15	25	300
BFS17A	(4)	NPN	SOT23	15	25	300
BFS17W	(3)	NPN	SOT323	15	50	300
BFS25A	(18)	NPN	SOT323	5	6.5	32
BFS505	(19)	NPN	SOT323	15[1]	18	150
BFS520	(20)	NPN	SOT323	15[1]	70	300
BFS540	(21)	NPN	SOT323	15[1]	120	500
BFT25	(1)	NPN	SOT23	5	6.5	30
BFT25A	(18)	NPN	SOT23	5	6.5	32
BFT92	(7)	PNP	SOT23	15	25	300
BFT92W	(7)	PNP	SOT323	15	35	300
BFT93	(9)	PNP	SOT23	12	35	300

Note

1. V_{CES}.

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFQ17	1.5		16	200		6.5	800					
BFQ18A	4											
BFQ19	5.5	3.3	11.5	500		7.5	800					
BFQ34	4	8	16.3	500				1200	26	45	120	15
BFQ67	8	1.7	14	1000	2.7	8	2000					
BFQ67W	8	2	13	1000	2.7	8	2000					
BFQ68	4		13	800				1600	28	47	240	15
BFQ135	6.5		17	500		13.5	800	1200			120	18
BFQ136	4		12.5	800				2500			500	15
BFQ149	5	3.75	12	500								
BFQ270	6		16	500		10	1000	1600			240	18
BFQ540	9	1.9		900				500			40	8
BFQ621	7		18.5	500				1200			120	18
BFR53	2	5[2]		500		10.5	800					
BFR92	5	2.4	18	500				150			14	10
BFR92A	5	2.1	14	1000	3	8	2000	150			14	10
BFR92AW	5	2	14	1000	3	8	2000					
BFR93	5	1.9	16.5	500								
BFR93A	6	1.9	13	1000	3	7	2000	425			30	8
BFR93AW	5	1.5	13	1000	2.1	8	2000					
BFR94A	3.5	8		200	5	13.5	500					
BFR106	5	3.5	11.5	800				350			50	9
BFR505	9	1.6	17	900	1.9	10	2000		4	10	5	6
BFR520	9	1.6	15	900	1.9	9	2000		17	26	20	6
BFR540	9	1.9	14	900	2.1	7	2000	550	21	34	40	8
BFS17	1	4.5		500								
BFS17A	2.8	2.5	13.5	800				150			14	10
BFS17W	1.6	4.5		500								
BFS25A	5	1.8	13	1000								
BFS505	9	1.6	17	900	1.9	10	2000		4	10	5	6
BFS520	9	1.6	15	900	1.9	9	2000		17	26	20	6
BFS540	9	1.9	14	900	2.1	8	2000		21	34	40	8
BFT25	2.3	3.8	18	500		12	800					
BFT25A	5	1.8	15	1000								
BFT92	5	2.5	18	500				150			14	10
BFT92W	5	2.5	17	500	3	11	1000					
BFT93	5	2.4	16.5	500				300			30	5

Notes

1. At $d_{im} = -60$ dB, measured according to DIN45004B, par. 6.3: 3-tone test.
2. Maximum value.

PRODUCT DATA

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFT93W	(9)	PNP	SOT323	12	50	300
MPSH10		NPN	SOT54	25	40	1000
PMBT3640		PNP	SOT23	12	80	350
PMBTH10		NPN	SOT23	25	40	400
PMBTH81		PNP	SOT23	20	40	400

DEVELOPMENT TYPES

TYPE NUMBER	f_T / I_C CURVE (see Fig.1)	POLARITY	PACKAGE	RATINGS		
				V_{CEO} (V)	I_C (mA)	P_{tot} (mW)
BFG21W	(28)	NPN	SOT343	4.5	200[1]	600

Note

1. Typical value.

PRODUCT DATA

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFT93W	5	2.4	15.5	500	3	10	1000					
MPSH10	0.65[2]											
PMBT3640	0.5[2]											
PMBTH10	0.65[2]											
PMBTH81	0.6[2]											

Notes

1. At d_{im} = –60 dB, measured according to DIN45004B, par. 6.3: 3-tone test.
2. Minimum value.

DEVELOPMENT TYPES

TYPE NUMBER	CHARACTERISTICS, typical values											
	f_T (GHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	F (dB)	G_{UM} (dB)	@ f (MHz)	V_o[1] (mV)	P_L (dBm)	ITO (dBm)	@ I_C (mA)	& V_{CE} (V)
BFG21W	18[2]		10[2][3]	1900								

Notes

1. At d_{im} = –60 dB, measured according to DIN45004B, par. 6.3: 3-tone test.
2. Minimum value.
3. Power gain G_p.

LINE-UPS

Analog cellular (AMPS, (E)TACS, NMT) 900 MHz

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
1	BFG540/X	BLT80	BLT81	1.2	6
1	BFG540/X	BLT70	BLT71	1.2	4.8
1	BFG10W/X	BLT71/8	–	1.2	4.8

Digital cellular (GSM) 900 MHz

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
1	BFG540W/X	BFG10W/X	BLT82	3.5 pulsed	6

Portable transmitters (860 MHz to 960 MHz)

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	SUPPLY VOLTAGE (V)
Bipolar					
1	BFG540	BLT80	BLT81	1.2	6
15	BFG93A	BLT80	BLT92/SL	3	7.5

RF wideband transmitters for pager front-end (see Fig.2)

FUNCTION	TYPE NUMBER	REMARKS
RF amplifier	BFC505	higher gain, lower noise, high isolation (0.3 mA)
	BFG403W	high performance, low voltage, low current
	BFR505	higher gain, lower noise (1 mA)
	BFT25A	lowest current (0.2 mA)
Oscillator, mixer or buffer	BFQ67	choice of the transistor is determined by the available current and the required performance
	BFR92A	
	BFR505	
	BFT25A	

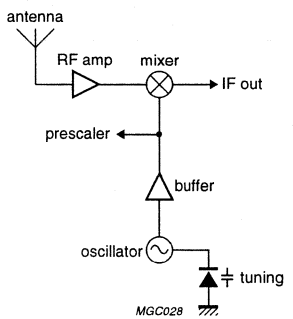


Fig.2 Typical front-end section for pagers.

RF wideband transistors for the receiver section in cordless/cellular phones (see Fig.3)

FUNCTION	TYPE NUMBER	SYSTEM FREQUENCY (MHz)	FEATURES
LNA	BFC505	1900	high isolation gain, low noise current
	BFG410W	900; 1900; 2500	very low noise
	BFG425W	900; 1900; 2500	very low noise
	BFR505	900; 1900	good performance at low current (1 mA)
	BFR520	900; 1900	higher gain, lower noise (10 mA)
Mixer	BFE505	900; 1900	balanced mixer in a single SOT353 package
	BFG505	900; 1900	good performance, low current
	BFG410W	900; 1900; 2500	low noise, high isolation
	BFG520	900; 1900	higher power to IF (10 mA)
	BFR93A	900	low cost, acceptable performance
Buffer and VCO	BFG410W	900; 1900; 2500	excellent isolation
	BFG505	1900	buffer and VCO in a single SOT353 package
	BFQ67	900	third generation, good performance
	BFR92A	900	excellent VCO, good buffer, low-cost
	BFR93A	900	excellent VCO, good buffer, low-cost
	BFR505	900; 1900	good VCO, high-gain buffer, low current
	BFR520	900; 1900	good VCO, higher output power
IF	BFS17A	40 to 100	any first or second generation transistor

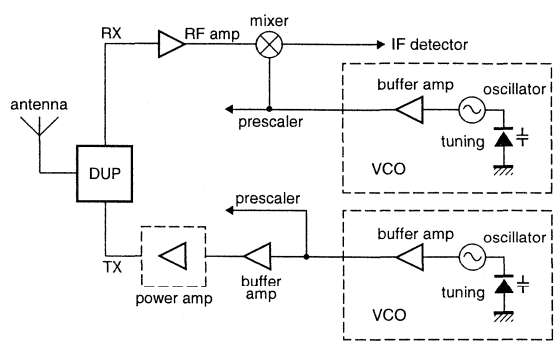


Fig.3 Typical RF section for cordless and cellular phones.

RF wideband transistors for the receiver section in cordless/cellular phones (see Fig.3)

FUNCTION	SYSTEM FREQUENCY (MHz)	SOT23	SOT323	SOT143 (1)	SOT343 (1)	SOT353	SOT363
LNA	900; 1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900; 1900	BFR 520	BFS520	BFG520	BFG520W	BFC520	BFM520
Mixer	900	BFR93A	BFR93AW	BFG93A			
	900; 1900	BFR505	BFS505	BFG505	BFG505W	BFE505	BFM505
	900; 1900	BFR520	BFS520	BFG520	BFG520W	BFE520	BFM520
Buffer and VCO	900	BFR92A	BFR92AW	BFG92A			
	900	BFR93A	BFR93AW	BFG93A			
	900	BFQ67	BFQ67W	BFG67			
	900; 1900	BFR505	BFS505	BFG505	BFG505W	BFC505	BFM505
	900; 1900	BFR520	BFS520	BFG520	BFG520W	BFC520	BFM520
IF	40 to 100	BF547	BF547W				
		BFS17	BFS17W	BFG17A			
		BFR92A	BFR92AW	BFG92A			

Note

1. Also available in /X and /XR versions.

RF wideband transistors for the power amplifier section in cordless/cellular phones (see Fig.4)

SYSTEM	SUPPLY VOLTAGE (V)	P_{out} (mW)	SOT143	SOT343
CT1, CT1+, CT2, CT2+, CT3	3.3	driver for PA2	BFG67	
			BFG505	BFG505W
			BFG520	BFG520W
		15	BFG67	
		20	BFG520	BFG520W
		40	BFG540	BFG540W
DECT, PHP	3.3	400	BFG540/X	BFG540W/X
			BFG10/X	BFG10W/X
			BFG11/X	BFG11W/X

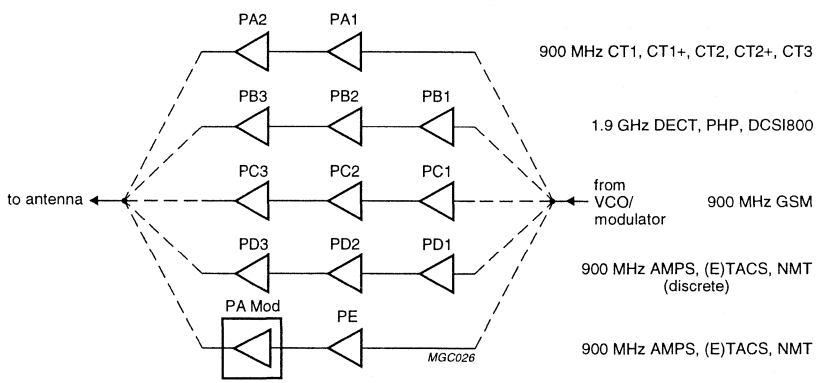


Fig.4 Typical power amplifier section for cordless and cellular phones.

MOSFETs for power/battery management and DC-DC convertor

Selection guide

MOSFETS FOR POWER/BATTERY MGT AND DC-DC CONVERTOR SELECTOR GUIDE

TYPE	DESCRIPTION	PACKAGE	V_{DS} (V)	RDS (ON)	@ V_{GS} (V)	P_{max} (W)
BSH103	N-channel enhancement mode MOS transistor	SOT23	30	520mΩ	2.5	0.5
BSH104	N-channel enhancement mode MOS transistor	SOT23	12	270mΩ	2.5	0.5
BSH105	N-channel enhancement mode MOS transistor	SOT23	12	180mΩ	2.5	0.5
BSH106	N-channel enhancement mode MOS transistor	SOT363	12	180mΩ	2.5	0.7
BSH107	N-channel enhancement mode MOS transistor	TSOP-6	12	70mΩ	2.5	0.8
BSH203	P-channel enhancement mode MOS transistor	SOT23	30	1300mΩ	2.5	0.5
BSH204	P-channel enhancement mode MOS transistor	SOT23	12	680mΩ	2.5	0.5
BSH205	P-channel enhancement mode MOS transistor	SOT23	12	450mΩ	2.5	0.5
BSH206	P-channel enhancement mode MOS transistor	SOT363	12	450mΩ	2.5	0.7
BSH207	P-channel enhancement mode MOS transistor	TSOP-6	12	180mΩ	2.5	0.8
BSN20W	N-channel enhancement mode vertical DMOS transistor	SOT323	50	15 Ω	10	0.2
BSP030	N-channel enhancement mode vertical DMOS transistor	SOT223	30	30mΩ	10	2
BSP090	P-channel enhancement mode vertical DMOS transistor	SOT223	30	90mΩ	10	2
BSP130	N-channel enhancement mode MOS transistor	SOT223	300	8 Ω	10	2
BSP255	P-channel enhancement mode MOS transistor	SOT223	300	17 Ω	10	2
PHC20512	Complementary enhancement mode MOS transistors	SO8	30	50+125 mΩ	10	2
PHC21025	Complementary enhancement mode MOS transistors	SO8	30	100+250 mΩ	10	2
PHC2300	Complementary enhancement mode MOS transistors	SO8	300	8+17 W	10	2
PHN1013	N-channel enhancement mode MOS transistor	SO8	30	13mΩ	10	2
PHN205	Dual N-channel enhancement mode MOS transistors	SO8	30	50+50m Ω	10	2
PHN210	Dual N-channel enhancement mode MOS transistors	SO8	30	100+100 mΩ	10	2
PHP212	Dual P-channel enhancement mode MOS transistors	SO8	30	125+125 mΩ	10	2
PHP212L	Dual P-channel enhancement mode MOS transistors	SO8	30	125+125 mΩ	4.5	2
PHP225	Dual P-channel enhancement mode MOS transistors	SO8	30	250+250 mΩ	10	2

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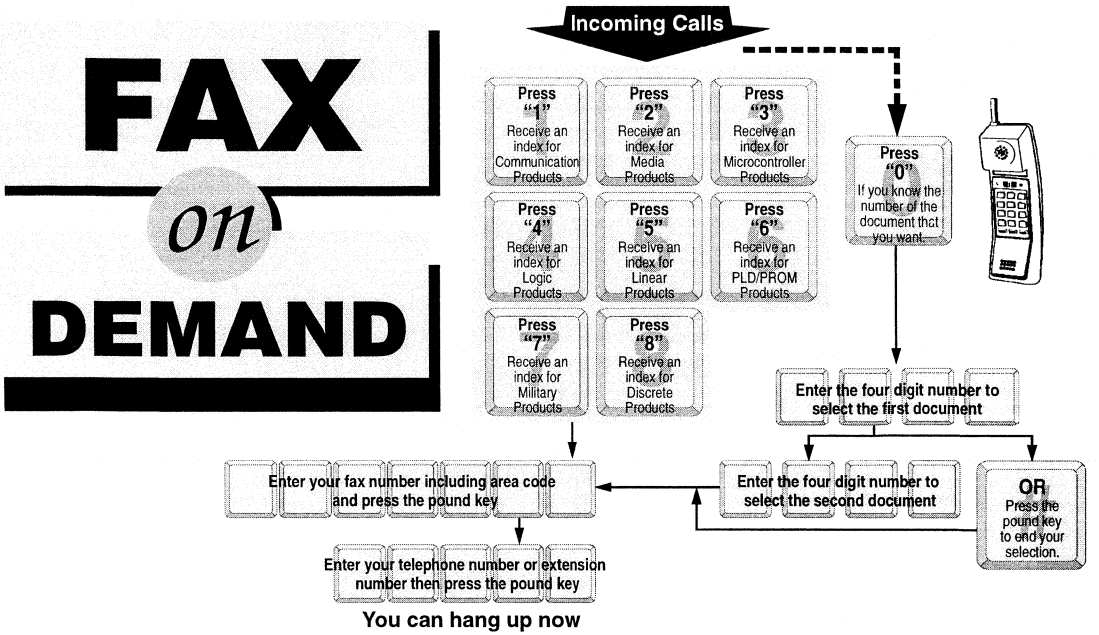
FAX-on-DEMAND System



What is it?

The FAX-on-DEMAND system is a computer facsimile system that allows customers to receive selected documents by fax automatically.

How does it work?

To order a document, you simply enter the document number. This number can be obtained by asking for an index of available documents to be faxed to you the first time you call the system.

Our system has a selection of the latest product data sheets from Philips with varying page counts. As you know, it takes approximately one minute to FAX one page. This isn't bad if the number of pages is less than 10. But if the document is 37 pages long, be ready for a long transmission!

Philips Semiconductors also maintains product information on the World-Wide Web. Our home page can be located at:
http://www.semiconductors.philips.com

Who do I contact if I have a question about FAX-on-DEMAND?

Contact your local Philips sales office.

FAX-on-DEMAND phone numbers:

England (United Kingdom, Ireland)	44-181-730-5020
France	33-1-40-99-60-60
Italy	39-167-295502
North America	1-800-282-2000

Locations soon to be in operation:

Hong Kong
Japan
The Netherlands

INTRODUCTION

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GSM (GLOBAL SYSTEM FOR MOBILE COMMUNICATIONS) DIGITAL CELLULAR ICs

In 1992 Philips produced the first single-chip baseband signal processor for GSM. Today our low voltage GSM ICs cover all functions–from antenna to microphone.

GSM digital cellular ICs

Three highly integrated ICs are available for the RF section: the SA1620 RF transceiver, the SA1638 IF transceiver and the UMA1021M RF synthesizer. The ICs support high IF frequencies to allow simple, low-cost filters to be used for image-rejection.

The BGY204 Power Amplifier Module provides an off-the-shelf solution for 2-Watt GSM transmitters. CGY2011G is an alternative MMIC solution.

The PCF5077 Power Amplifier Controller ensures that PA on/off and output characteristics meet GSM/DCS1800 requirements, Phase II.

The baseband and audio interface is now a single-chip interface between the RF transceiver, the microphone and ear piece and the baseband processor. It integrates an audio Codec and auxiliary AD/DA converter for AGC, AFC and power management.

The baseband DSP includes the TDMA timer. An on-chip ROM contains firmware program modules to perform all necessary processing algorithms. Special attention has now been given to equalization in order to improve performance in hilly areas and fast-moving vehicles.

Philips Semiconductors' GSM ICs include:

SA1620 - Low voltage GSM RF transceiver

SA1638 - Low voltage GSM IF transceiver

UMA1021M - Low voltage frequency synthesizer for radio telephones

BGY204 - Power amplifier module

CGY2013G - MMIC power amplifier

UBA1710 - Modulator for GaAs PAs

PCF5077 - Power amplifier controller for GSM systems

TDA8002/TDA8005 - SIM interface

P90CL301 - Low voltage microcontroller

PCF507X - GSM baseband interface

PCF5083 - GSM baseband processor

TEA1095 - Handsfree IC

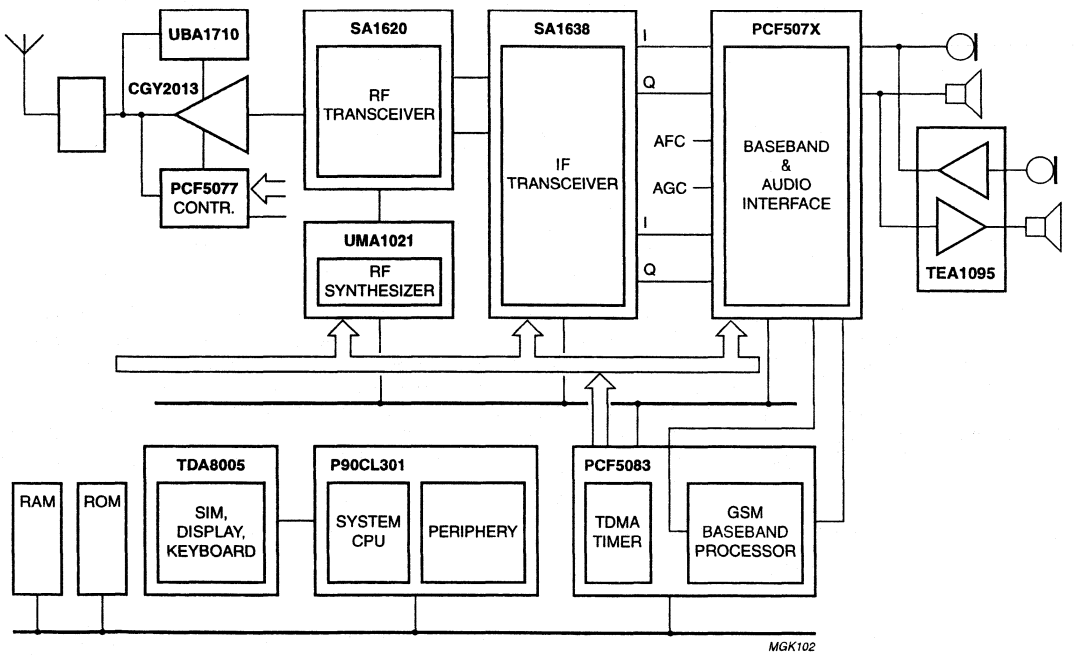


Fig.1 GSM digital cellular ICs.

American Digital Cellular RF transceiver chip–sets (TDMA)

North American Digital Cellular (NADC) IS-54/-136 PCS TDMA RF Transceiver Chipsets

1st generation TDMA RF transceiver chip–set (Single–band 800MHz, Dual–mode AMPS/DAMPS)

The chip–set combines all of the necessary RF and IF functions into **four integrated devices**: the SA621 RF front end, the SA7025 dual frequency synthesizer, the SA900 I/Q transmit modulator and the SA637 digital IF receiver or SA606 FM IF receiver + external I/Q demodulator. These devices were designed as a system and therefore have interface levels which are matched, eliminating the need for additional buffers and interface devices. There is also a common high speed serial interface bus, making addressing the devices simpler. Additionally the frequency plan was designed to eliminate the need for an additional synthesizer and VCO loop. All of these features dramatically reduces the cost and size while improving the performance of the overall system.

Although this is our first IS–54/–136 solution, our 4–chip configuration is one of the most integrated and easy to use chip–set available. For example, the SA900 provides I/Q modulators, the phase shifter, the VGA, a filter, control logic, clock distribution and more in a single IC. The need for two RF synthesizers was eliminated by closely coupling the SA7025 and the SA900 so it is possible to use the main synthesizer to simultaneously generate receive and transmit signals. The integration and connectivity of the chip–set promote significant cost reduction. In addition this integrated solution reduces the time to a final product by simplifying the design effort.

Philips 1st generation TDMA RF transceiver chipset consists of the following ICs:

SA621	1GHz low voltage LNA, mixer and VCO
SA606	Low voltage high performance mixer FM/IF system
SA637	Low-voltage digital IF receiver
SA7025	Low-voltage 1GHz fractional-N synthesizer
SA900	I/Q transmit modulator

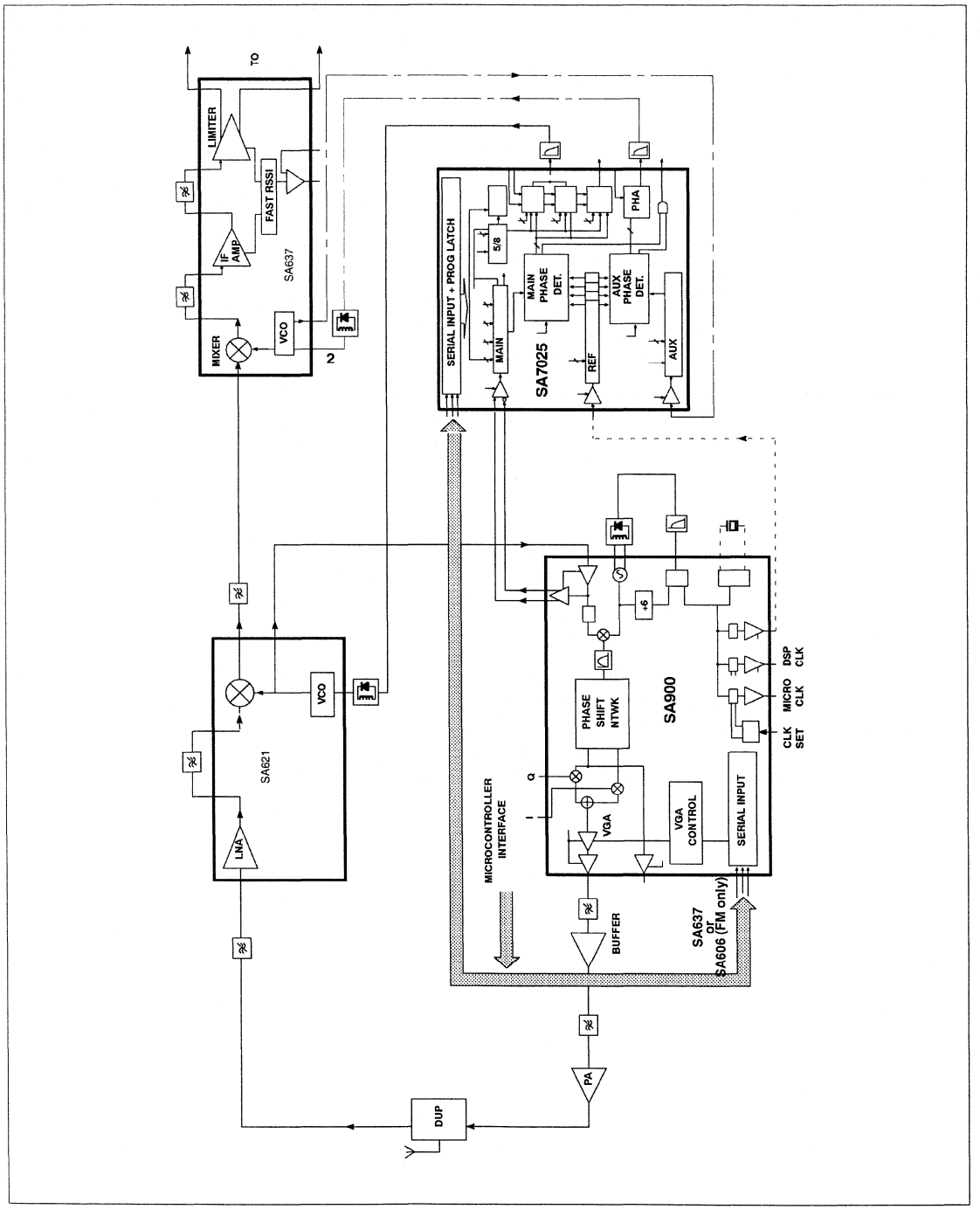
2nd generation TDMA RF transceiver chip–set (Dual–band 800/1900MHz, Triple–mode AMPS/DAMPS/PCS)

This chip–set combines all the necessary RF and IF functions into **three integrated devices**: the SA1920 RF dual–band front end, the SA647 Low power digital IF system receiver and the SA9025 I/Q transmit modulator with integrated dual fractional–N frequency synthesizer. This is the most highly integrated dual–band, triple–mode PCS chip–set available on the market. These devices were designed as a system and therefore have interface levels which are matched, eliminating the need for additional buffers and interface devices. Additionally the frequency plan was designed to eliminate the need for any additional synthesizer and VCO loop. The result is a smaller, cost effective, low–power phone that is ultimately more attractive to the end users.

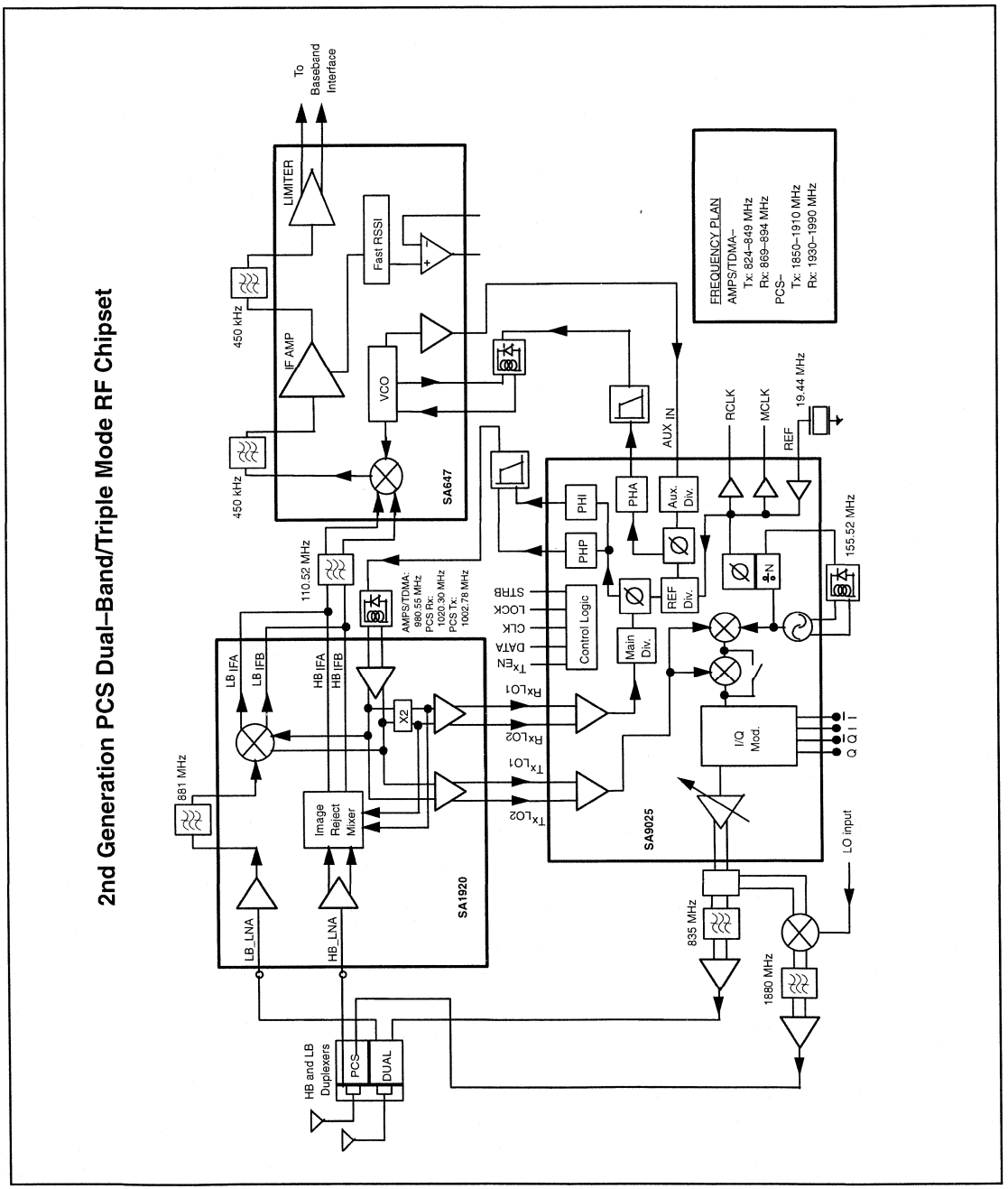
Philips 2nd generation TDMA (PCS) RF transceiver chipset consists of the following ICs:

SA1920	Dual–band 800/1900MHz RF Front–End
SA647	Low–Power FM IF System
SA9025	Transmit Modulator with integrated Dual Fractional–N synthesizer

1st generation TDMA RF transceiver chip–set (AMPS/DAMPS)



2nd generation TDMA RF transceiver chip–set (AMPS/DAMP/PCS)



DECT (DIGITAL ENHANCED CORDLESS TELECOMMUNICATIONS)

Set to become a world standard for cordless, DECT has been renamed to abbreviate "Digital Enhanced Cordless Telecommunications". Philips Semiconductors offers very competitive complete DECT solutions including hardware, software and support for applications ranging from residential to 2-line business systems. Both off-the-shelf and customized solutions are available.

Residential and 2-line business systems

- The RF transceiver incorporates a double superheterodyne receiver that is composed of the UMA1022M 2 GHz dual frequency synthesizer, SA639 FM IF and UAA2067 front end.
- The PCD509x (ABC) family is a range of versatile low-power GAP-compliant single chip baseband processor ICs designed to allow flexibility in the design of residential and small PBX systems and data applications and enables a high degree of customization of the MMI e.g. speaker phone and conference calling.
- The PCD5096 (Universal Codec) integrates two audio codecs, a DSP (performs echo cancellation, conference call, DTMF, dial tone generation) and two PSTN interfaces onto one chip. Together with the ABC family the universal codec meets all the requirements to create two-line PSTN low-cost digital cordless systems and add functionality to high-end corded phones. In addition, the IOM-2 interface can provide analog extensions for ISDN.
- Philips Semiconductors also provides GAP-compatible and approved DECT software tested in compliance with TBR22; both standard catalogue and customized MMIs.

Philips Semiconductors' DECT ICs include:

UAA2067G - Low voltage RF transceiver–2 GHz

SA639 - Low voltage mixer FM IF system with filter amplifier and data switch

UMA1022M - Low voltage frequency synthesizer for radio telephones

CGY2030/CGY2032 - Low voltage MMIC power amplifiers

PCD5091/2/3/4/5 - DECT baseband processor–ADPCM, burst-mode controller and microcontroller

PCD5096 - Universal CODEC

PCA1070/TEA1118A - Line Interface (Basestation)

PCD3316 - Caller ID/Call Waiting (CIDCW)

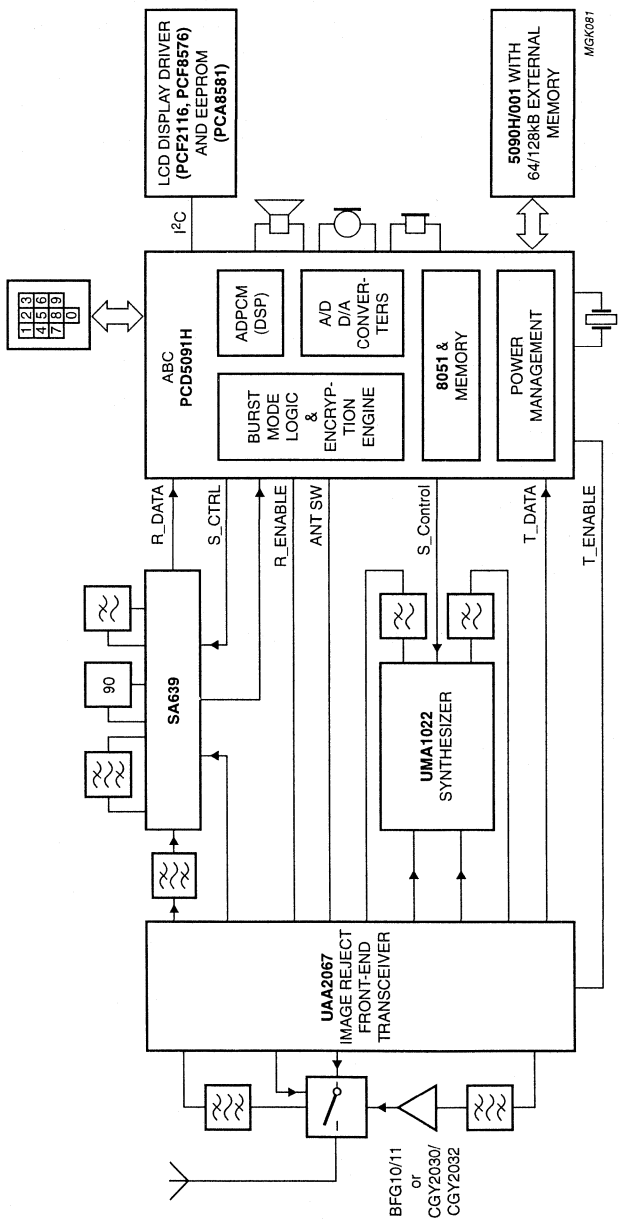


Fig.1 DECT handset chipset.

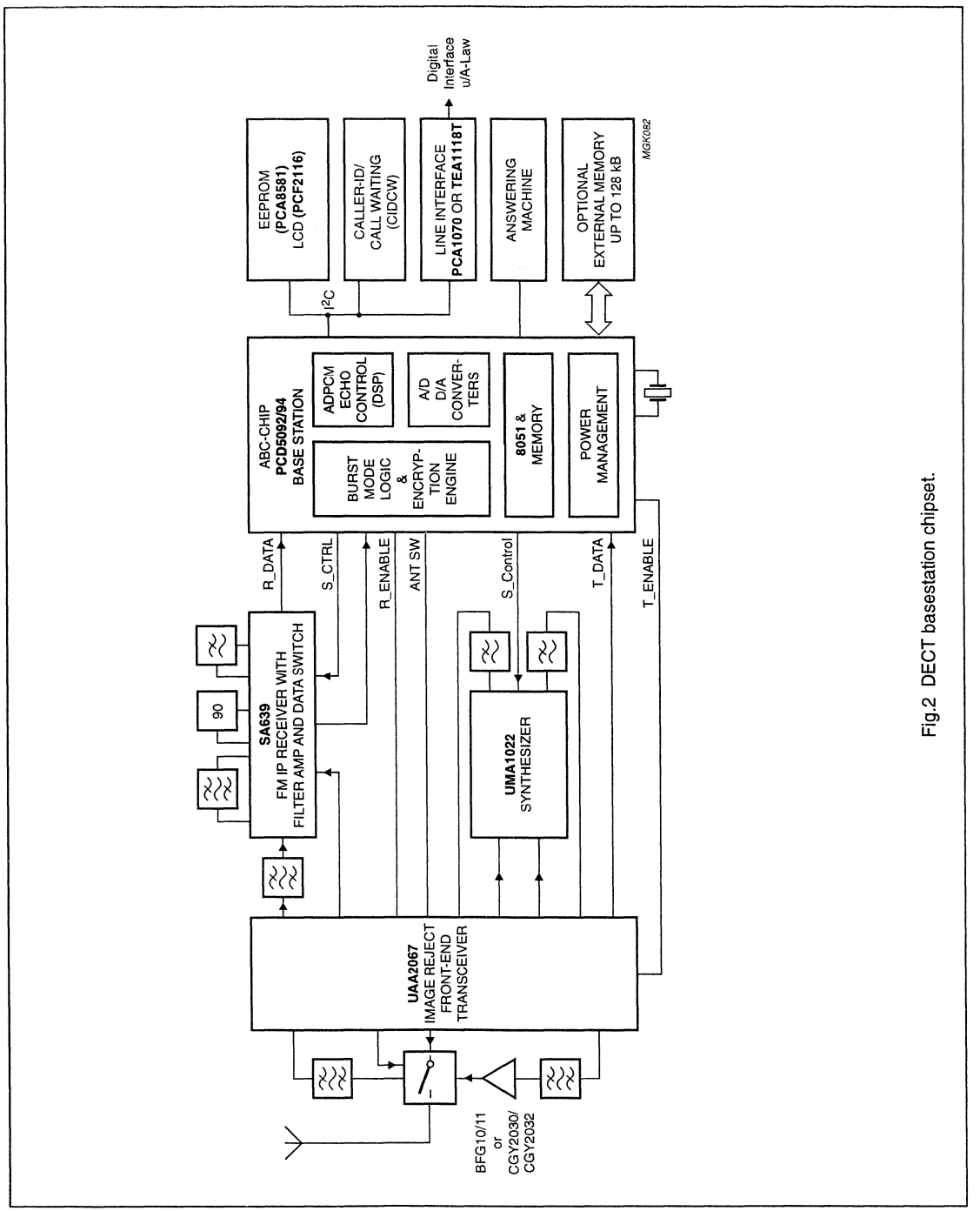


Fig.2 DECT basestation chipset.

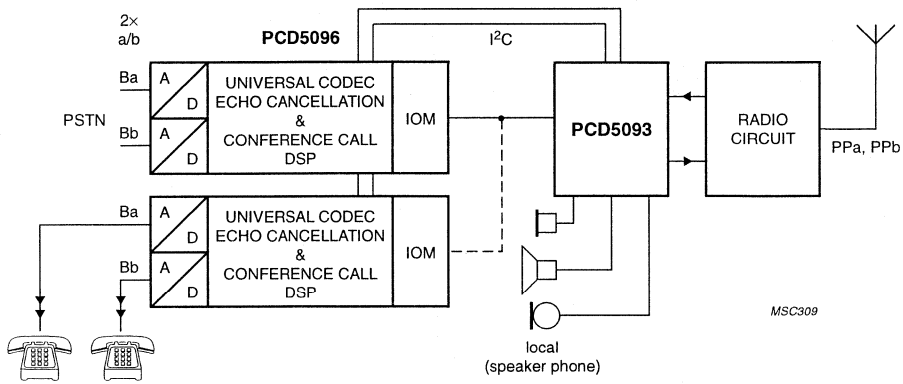


Fig.3 A typical DECT small business system with the PCD5096 universal codec, the single-chip baseband processor (ABC chip) and an RF interface.

AMPS/(E)TACS/CDPD Analog Cellular

Analog Cellular Chipset
AMPS (Advanced Mobile Phone Service)
TACS (Total Access Communication System)
CDPD (Cellular Digital Packet Data)

AMPS/ETACS

The analog cellular market is a consumer market with heavy price pressures on handsets and components. Analog cellular is still the worlds largest cellular system. Development in analog cellular handsets still continues at a faster pace, offering more features, lowering prices and more models.

Manufacturers of handsets face shorter product life cycles, faster Time–to–Market (TtM) and rapidly decreasing market prices. With Philips' long–time experience in analog cellular, our chipset presents a proven solution.

New ICs in the chipset are developed in order to meet market demand for lower cost and faster TtM.

Current AMPS/ETACS

Our chipset uses proven 3V technology to improve power–consumption of a hand–held phone, thus improving talk–time and standby–time.

The chipset is supported by a software package (source–code), consisting of protocol stack and examples for Man–Machine–Interface (MMI) and device drivers.

RF Transceiver

The transceiver section consists of 4 low–voltage, low–power ICs: For the Front–End, either the SA611 or SA621 can be used. Both have high–performance LNA and mixer on–chip. In addition, the SA621 contains an oscillator. With only an external resonator circuit, the SA621 can be configured as a VCO.

For the FM–IF, either the SA606 or the SA616 can be used. Both down–convert the 1st IF signal to provide the audio/data RSSI signals. The UMA1015 dual frequency synthesizer locks the receive and transmit VCOs. In the PA section, the SA910 is the low–voltage, high efficiency, pre–driver IC for the output power transistor (eg. BLT61).

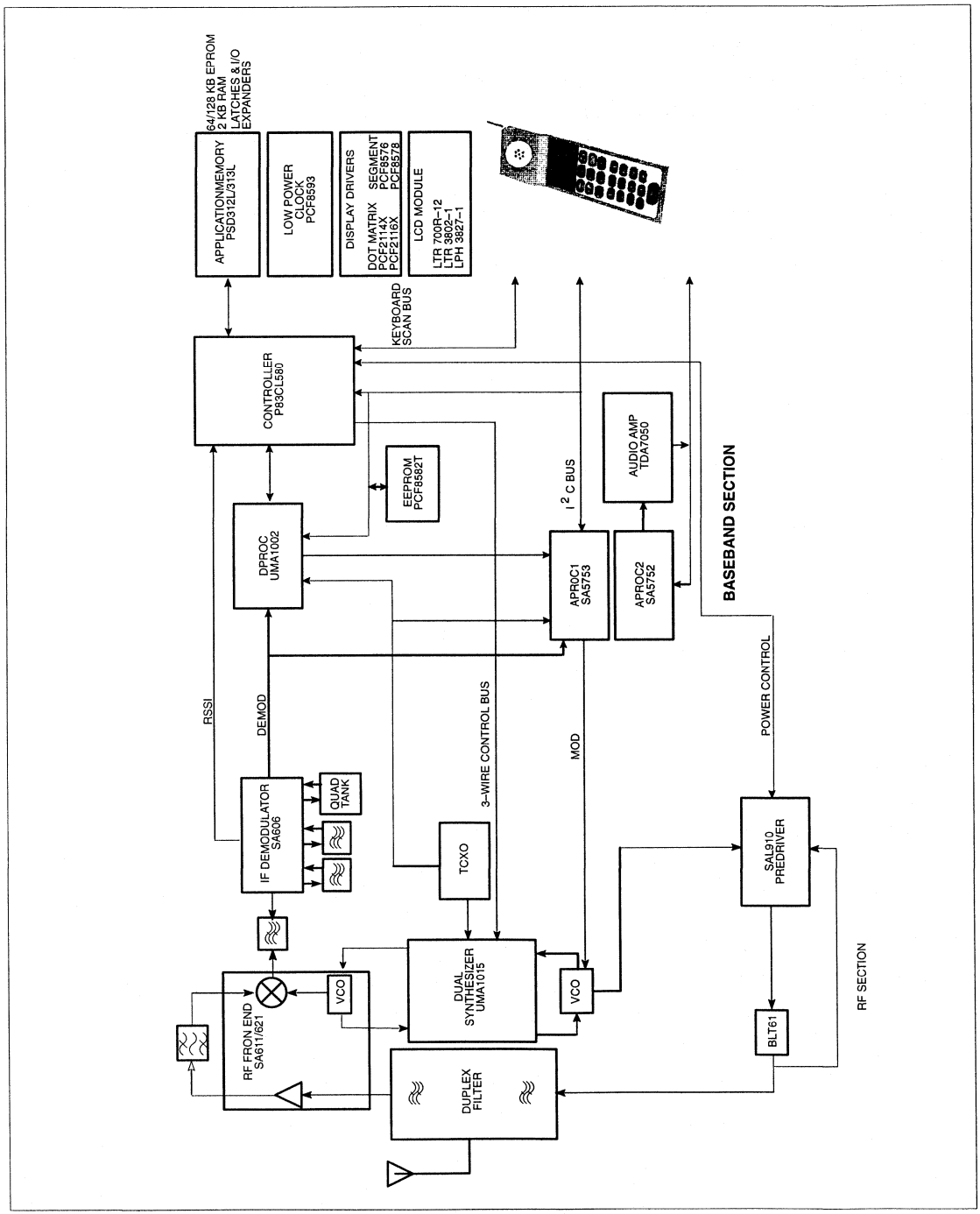
Baseband Section

The AMPS/(E)TACS baseband solution handles all audio and data processing, control and memory functions. The SA5752, SA5753 audio processors and TDA7050 audio amplifier provide companding, VOX, filtering, amplification and control functions needed to meet AMPS and (E)TACS system requirements. The UMA1002 low voltage data processor incorporates all of the necessary data transceiving, processing and SAT functions. The P83CL580 8-bit microcontroller, PCF8582T EEPROM and PSD312L EPROM provide the control and memory for the entire handset.

The Philips Semiconductors AMPS/(E)TACS/CDPD chipset consists of: **IC17 Page**

SA611/621	Low voltage LNA and mixer - 1GHz	
SA606	Low-voltage high performance mixer FM IF system	
UMA1015M	Low-power dual frequency synthesizer for radio communications	
SA5752	Audio processor - companding, VOX and amplifier section	
SA5753	Audio processor - filter and control section	
UMA1002	Data processor for cellular radio (DPROC2)	
P83CL580	8-Bit Microcontroller	
TDA7050	Audio amplifier	
SA910	Variabe gain RF predriver amplifier	

AMPS/(E)TACS/CDPD Analog Cellular



COMPLETE CT0 ANALOG CORDLESS CHIPSET

Philips fully supports all analog cordless standards with chipsets, discrete and module solutions, together with software/firmware, demo boards and comprehensive design-in/application support. Because our baseband modules/chipsets include some commonality in components and software, our CT0 solutions offer a low-risk investment for OEMs wishing to enter the analog cordless market. Demo/evaluation boards are available to cover all CT0 frequencies.

The low-frequency CT0 analog cordless standard is established in many countries at various frequencies around 50 MHz, including:

- France (26/41 MHz)
- Australia (30/39 MHz)
- The Netherlands and Spain (31/40 MHz)
- China, S. Korea, Taiwan, USA, Latin America (46/49 MHz)
- China (48/74 MHz).

As this market continues to grow (in terms of countries and increasing user density), our complete CT0 module/chipset system approach offers a low-cost solution with several competitive advantages. Our CT0-V3A chipset, for example, offers the following functionality:

- Auto-scan multiple-channel access (MCA) system automatically detects and selects a free channel for incoming and outgoing calls
- 1200 bps minimum shift keying (MSK) data transmission for high spectral efficiency and low-energy harmonics
- Supports up to seven handsets
- Call transfer between base unit and each handsets
- 20-bit digital security code, user programmable
- Advanced, patented power-saving scheme
- 10 days of stand-by with 270 mAh battery
- Two-way paging and intercom
- Speakerphone on base unit
- EEPROM for non-volatile storage of repertory memory and security code
- Independent repertory memory for base unit and each handset
- Tone/pulse mix-mode dialing
- Channel display in base unit
- Built-in 'test modes' to facilitate test alignment
- Jumper selectable country options (need to modify RF circuit accordingly).

Other recent additions to our range include the TEA1118 and TEA118A, which are derivatives of our TEA1112 speech/transmission ICs. These new ICs have transmit inputs which handle signals up to 1 Vrms with less than 2% THD, and have low transmit gain (typically 11 dB). The TEA1118A incorporates DTMF, Mute and transmit Mute inputs, and is therefore particularly suitable for CT0.

Philips Semiconductors' CT0 chipset consists of the following ICs:

TDA7052A/AT - 1 Watt low voltage audio power amp with DC volume control

SA676 - Low voltage mixer FM IF system

SA576 - Low power compandor

74V373D - Port extender

PCD3353 or **PCD3755** - DTMF dialler, EEPROM, RAM, microcontroller (handset)

PCD3354A - DTMF dialler, EEPROM, RAM, microcontroller (base station)

TEA1094 - Speaker phone amplifier (base station)

TEA1062A or **TEA1118/A** - Speech and line interfaces (base station)

LC7152M - Dual PLL synthesizer

HEF4511 - Seven-segment driver

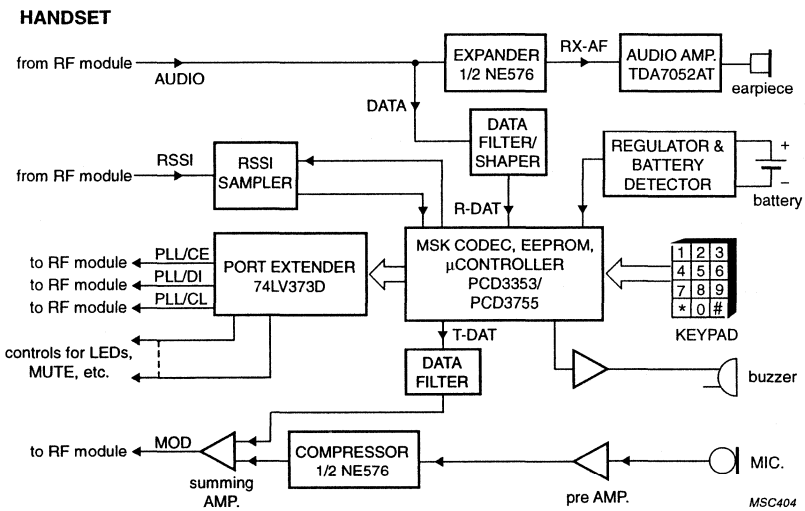


Fig.1 CT0-V3A handset chipset.

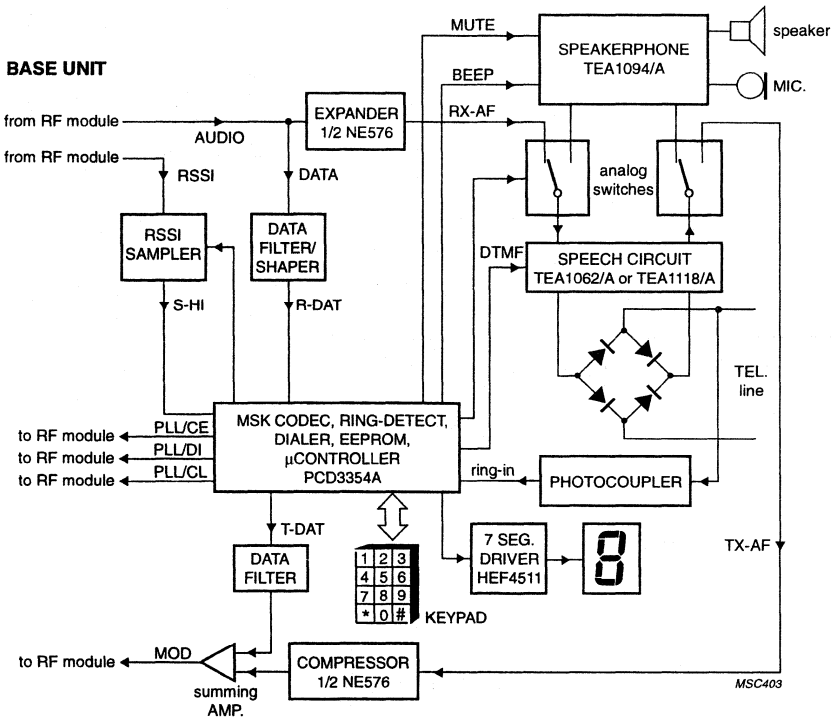


Fig.2 CT0-V3A base unit chipset.

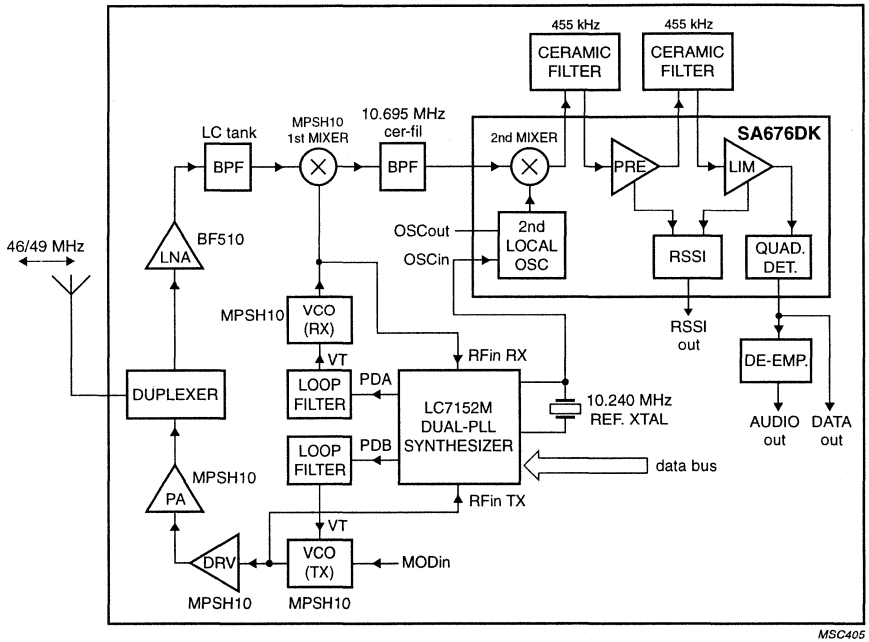


Fig.3 RF module for CT0.

PAGING

FLEX™

FLEX™ is now the de-facto high-speed paging standard with the following advantages:

- More subscribers per given frequency and shorter transmission air time
- Highly improved battery life
- Very robust signal codes (fewer missed or corrupted messages)
- Efficient traffic management for service provider possible.

The FLEXChip™ PCD5008 pager decoder has the following key features:

- FLEX™ paging protocol decoder
- Bitrates: 1600, 3200 and 6400 bps
- 16 short or 8 long addresses, 16 fixed temporary addresses
- Any-phase decoding
- RTC time base and "Over-the-air" time update support
- Compatible with synthesized receivers
- Low Battery Indication (external detector)
- Low profile LQFP32 package
- Low voltage 1.8 to 3.6 V
- Low power consumption by using hardware decoding

A demoboard and application notes are available for this decoder.

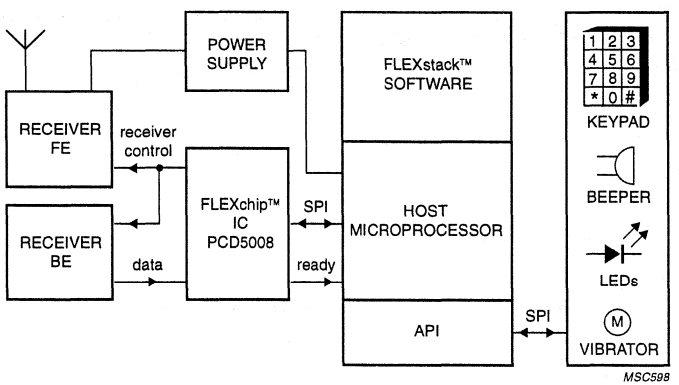


Fig.1 FLEX™ circuit diagram.

POCSAG/APOC1

We offer five advanced chips for all the key functions of beep-only, numeric and alphanumeric pagers:

UAA2080/2 - pager receiver

PCF5001 - POCSAG paging decoder

PCD5003 - advanced POCSAG paging decoder

PCD5002 - advanced POCSAG/APOC1 paging decoder

Evaluation kits and application notes are available for these components.

UAA2080/82 PAGER RECEIVERS

These are high-performance low-power radio receiver circuits primarily intended for VHF and UHF wide-area (country-wide) digital pagers. With a high level of integration, both devices can be used in very thin pagers (e.g. wrist-watch or credit card types). Employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK), the receivers are based on the direct conversion principle (zero IF). Operating up to 2400 baud, the UAA2080/82 are unique in their size, power consumption and performance advantages. The UAA2082 has additionally a low-battery detect voltage of 1.1 V; the internal oscillator is disconnected when using direct injection from a frequency synthesizer, to further reduce current consumption.

Key features include:

- high integration level
- wide frequency range
- low power consumption
- high sensitivity
- high dynamic range
- interfaces directly with the PCF5001, PCD5002, PCD5003
- QFP32, SO28 package or naked chip.

PCF5001 LOW COST POCSAG PAGING DECODER

This is a fully integrated low-power decoder and pager controller, which was specially developed for radio pagers. It interfaces directly to the UAA2080/82 digital paging receivers. It decodes the CCIR radio paging Code No.1 at 512, 1200 and 2400 bits/s data rates and includes a digital input filter for high call success rates.

Key features include:

- extremely cost efficient (low price/performance ration)
- on-chip 114-bit EEPROM storage
- wide supply voltage range (1.5 to 6 V)
- low supply current (60 A with 76.8 kHz crystal)
- data rates up to 2400 bits/s possible
- supports 4 user addresses (Receiver Identity Codes) in 2 independent frames
- drives an LED, a magnetic or piezo ceramic beeper directly and offers optional vibrator type alerting
- silent call storage (up to 8 calls)
- QFP32, SO28 package or naked chip.

PCD5002 Advanced POCSAG and APOC1 paging decoder

The PCD5002 is a very low power pager decoder and controller, capable of handling both standard POCSAG and the advanced APOC1 code. Data rates supported are 512, 200 and 2400 bps using a single 76.8 kHz crystal. On-chip EEPROM is programmable using a minimum supply voltage of 2.5 V.

Key features include:

- POCSAG compatible
- APOC1 compatible for extended battery economy
- data rates supported are 512, 1200 and 2400 bps using a single 76.8 kHz crystal
- advanced ACCESS synchronization algorithm
- 2-bit random and (optional) 4-bit burst error correction
- up to 6 user address frames, independently programmable
- continuous data decoding upon reception of user programmable sync word (optional)
- call alert via beeper, vibrator or LED
- separate power control of receiver and RF oscillator for battery economy
- on-chip EEPROM (384 bit) is programmable using a minimum supply voltage of 2.5 V
- on-chip SRAM buffer for message data
- wake-up interrupt for microcontroller, programmable polarity
- real Time Clock reference output
- on-chip voltage doubler
- I^2C-interface to microcontroller for transfer of data, status/control and EEPROM programming (max 100 kb/s)
- interface to UAA2080 and UAA2082 paging receivers
- wide operating voltage range 1.5 to 6.0 V

PCD5003 POCSAG paging decoder

The PCD5003 is a very low power decoder and pager controller. It supports data rates of 512, 1200 and 2400 bps using a single 76.8 kHz crystal. Its on chip EEPROM is programmable with a minimum supply of 2.5 V.

Key features are:

- low operating current (50 mA ON; 25 mA OFF)
- 2-bit random and (optional) 4-bit burst address error correction
- up to 6 user addresses (RICs), in up to 6 different frames
- standard POCSAG synch. word, plus up to 4 user-programmable synch. words
- received data inversion (optional)
- synthesizer set-up and control interface (3-line serial)
- separate power control or Receiver and RF oscillator for battery economy
- on-chip SRAM buffer for message data
- direct and I^2C-bus control of operating status (ON/OFF)
- wake-up interrupt for microcontroller, programmable polarity
- built-in data filter and bit clock recovery
- low profile package LQFP32

EVALUATION KITS

OM4706 - POCSAG decoder board PCF5001

OM4718 - Test program board for PCF5001

OM4745 - 2080H 173 MHz

OM4746 - 2080H 288 MHz

OM4747 - 2080H 470 MHz

OM4748 - 2080H frequency open

OM4749 - Pager bit error rate test board

OM4759 - PALOMA SW for pager antenna calc.

OM4763 - PCD5003 POCSAG decoder system

OM5837 - Pager demo system for the PCD5008 FLEX™ decoder

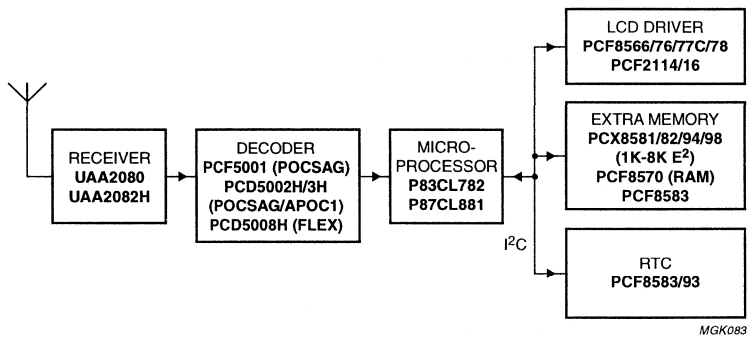


Fig.2 Paging solutions.

GENERAL

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TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under "Serial number/special third letter"

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control and switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A For triacs, after second letter 'R' or 'T'

F For emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L For lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O For opto-triacs, after second letter 'R'

T For 3-state bicolour LEDs, after second letter 'Q'

W For transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112	Germanium, low power signal diode (consumer type)
ACY32	Germanium, low power AF transistor (industrial type)
BD232	Silicon, power AF transistor (consumer type)
CQY17	GaAs, light-emitting diode (industrial type)
RPY84	CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%

B 2%

C 5%

D 10%

E 20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C −55 to +125 °C

D −25 to + 70 °C

E −25 to + 85 °C

F −40 to + 85 °C

G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

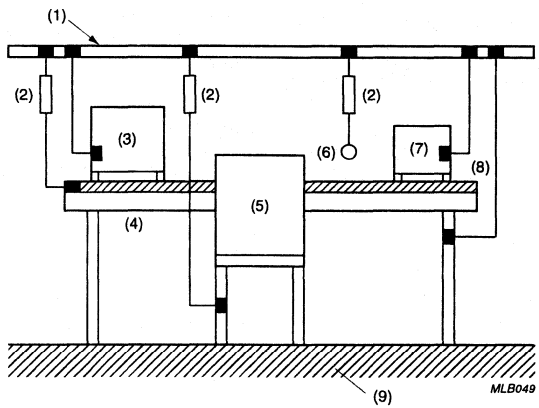
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

APPLICATION INFORMATION

Applications for compandors NE570/571/SA571 AN174

APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the SA570.

BASIC EXPANDOR

Figure 1 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and ΔG cell inputs are tied to V_{IN} so that the gain is proportional to the average value of (V_{IN}). Thus, when V_{IN} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$\text{Gain exp.} = \left[\frac{2\ R_3\ V_{IN}\ (avg)}{R_1\ R_2\ I_B}\right]^2$$

$I_B = 140\mu A$

The maximum input that can be handled by the circuit in Figure 1 is a peak of 3V. The rectifier input current can be as large as $I=3V/R_1=3V/10k=300\mu A$. The ΔG cell input current should be limited to $I=2.8V/R_2=2.8V/20k=140\mu A$. If it is necessary to handle larger input voltages than 0 ±2.8V peak, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 1 shows a pair of input capacitors C_{IN1} and C_{IN2}. It is now necessary to use both capacitors if low level tracking accuracy is not important. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset

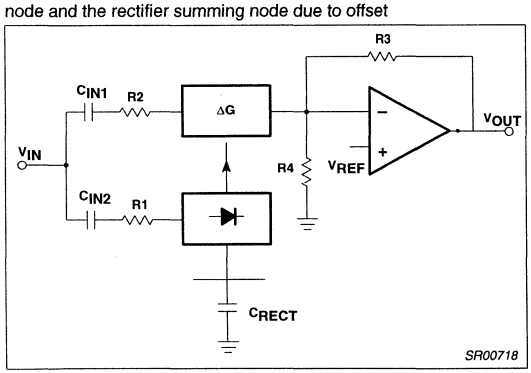


Figure 1. Basic Expandor

voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expandor is biased up to 3V by the DC gain provided by R_3, R_4. The output will bias up to

$$V_{OUTDC} = 1 + \frac{R_3}{R_4}\ V_{REF}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to V_{CC}.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300μA peak current restriction).

BASIC COMPRESSOR

Figure 2 shows how to use the SA570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$\text{Gain comp.} = \left[\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)}\right]^{\frac{1}{2}}$$

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no DC feedback path around the op amp through the ΔG cell, one must be provided externally. The pair of resistors R_{DC} and the capacitor C_{DC} must be provided. The op amp output will bias up to

$$V_{OUTDC} = \left(1 + \frac{R_{DC}}{R_4}\right) V_{REF}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±300μA peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

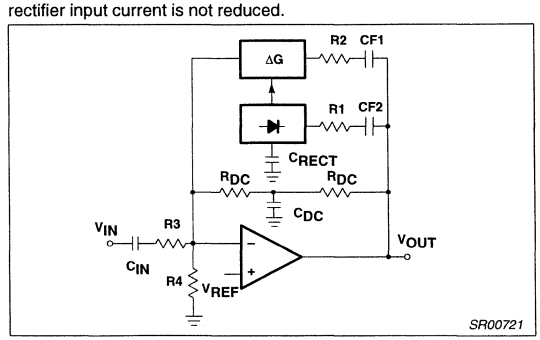


Figure 2. Basic Compressor

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal (input signal meaning the current into the ΔG cell). The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 3 is suitable, as would be any other capable of delivering ±30μA into 100Ω resistor tied to 1.8V.

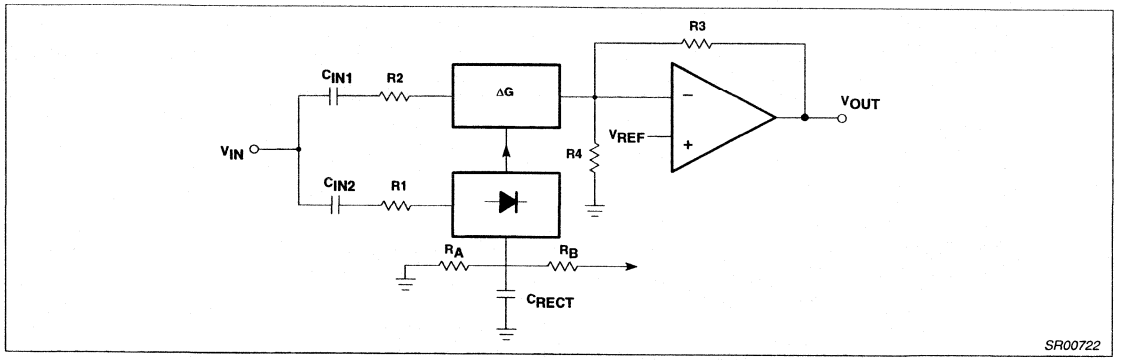


Figure 3. Expandor With Low Level Mistracking

LOW LEVEL MISTRACKING

The compandor will follow a 2-to-1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of <100nA that produces errors at low levels. The magnitude signal level drops to a 1μA average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

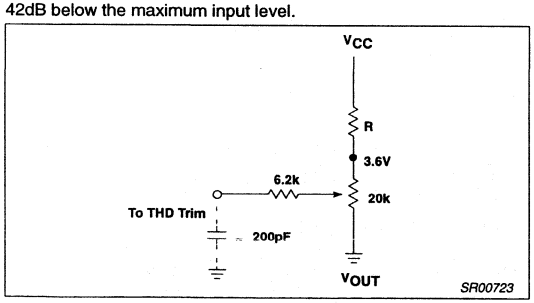


Figure 4. THD Trim Network

It is possible to deviate from the 2-to-1 transfer characteristic at low levels as shown in the circuit of Figure 4. Either R_A or R_B, (but not both), is required. The voltage on C_{RECT} is $2 \times V_{BE}$ plus V_{IN} avg. For low level inputs V_{IN} avg is negligible, so we can assume 1.3V as the bias on C_{RECT}. If R_A is placed from C_{RECT} to AND we will bleed off a current $I=1.3V/R_A$. If the rectifier average input current is less than this value, there will be no gain control input to the ΔG cell so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed $1.3V/R_A$ and the expandor output will become active. For large input signals, R_A will have little effect. The result of this is that we will deviate from the 2-to-1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 5 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_A will be a function of temperature because of the two V_{BE} drops, so the low level tracking will drift with temperature. If a negative supply is available, if would be desirable to tie R_A to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{BE} temperature drift.

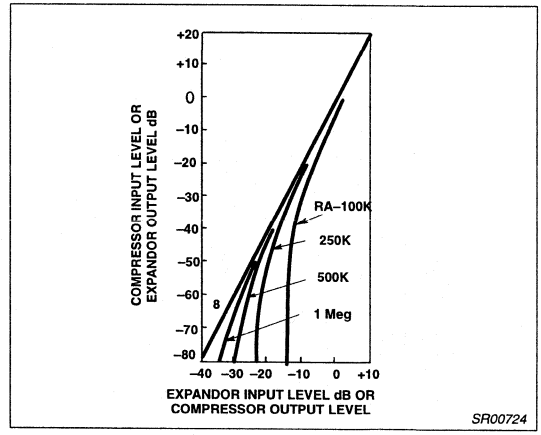


Figure 5. Mistracking With R_A

R_B will supply an extra current to the rectifier equal to $(V_{CC}–1.3V)R_B$. In this case, the expandor transfer characteristic will deviate towards 1-to-1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor, this would lead to a lack of compression at low levels. Figure 6 shows some typical transfer curves. An R_B value of approximately 2.5M would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

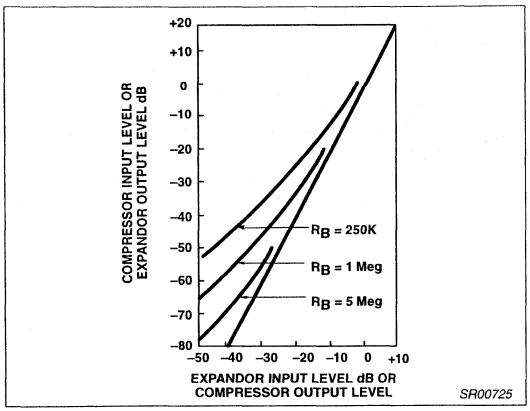


Figure 6. Mistracking With R_B

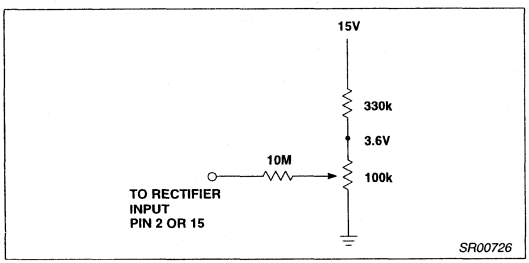


Figure 7. Rectifier Bias Current Compensation

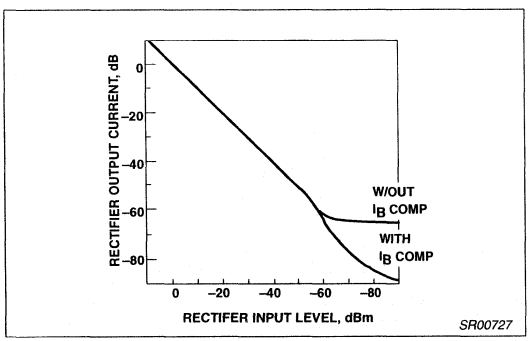


Figure 8. Rectifier Performance With Bias Current Compensation

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100nA. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 7. Figure 8 shows the rectifier performance with and without bias current cancellation.

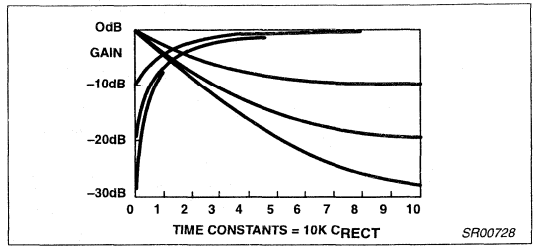


Figure 9. Gain vs Time Input Steps of ±10, ±20, ±30dB

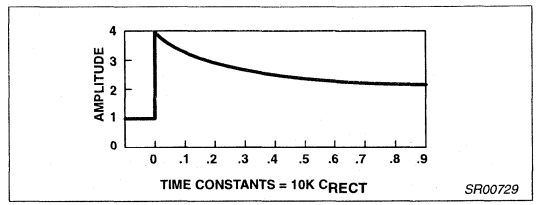


Figure 10. Compressor Attack Envelope +12dB Step

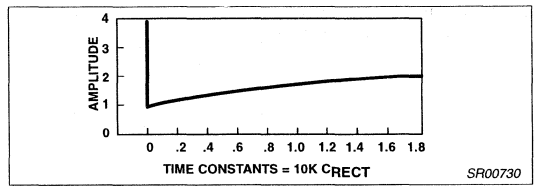


Figure 11. Compressor Release Envelope –12dB Step

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant $10k \times C_{RECT}$. Figure 9 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level.

The attack time is much faster than the decay, which is desirable in most applications. Figure 10 shows the compressor attack envelope for a +12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t=0.15 in the figure. The CCITT recommends an attack time of 3 ±2ms, which suggests an RC product of 20ms. Figure 11 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5 ±9ms. This corresponds to t=0.675 in the figure, which again suggests a 20ms RC product. Since R_1=10k, the CCITT recommendations will be met if C_{RECT}=2μF.

There is a trade-off between fast response and low distortion. If a small C_{RECT} is used to get very fast attack and decay, some ripple

will appear on the gain control line and produce distortion. As a rule, a 1μF C_{RECT} will produce 0.2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where C_{RECT}=2μF, the ripple would cause 0.1% distortion at 1kHz and 0.33% at 800Hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C_{RECT}.

FAST ATTACK, SLOW RELEASE HARD LIMITER

The SA570/571 can be easily used to make an excellent limiter. Figure 12 shows a typical circuit which requires of an SA570/571, of an LM339 quad comparator, and a PNP transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or –1V peak, a comparator threshold is exceeded. The PNP is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10k. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about 0.7μA through the rectifier to prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on Pin 1 or 16 exceeds two diode drops. If C_4 were allowed to become completely discharged, there would be a slight delay before it recharged to >1.2V and activated limiting action.

A stereo limiter can be built out of 1 SA570/571, 1 LM339 and two PNP transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then Pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one PNP transistor and one capacitor C_4 need be used. The release time will then be the product 5k×C_4 since two channels are being supplied current from C_4.

USE OF EXTERNAL OP AMP

The operational amplifiers in the SA570/571 are not adequate for some applications.

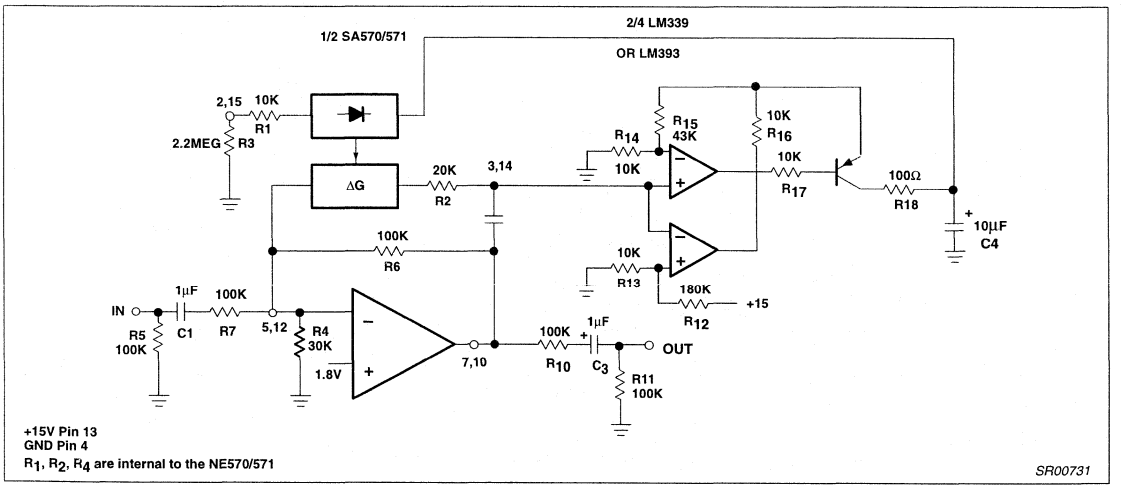


Figure 12. Fast Attack, Slow Release Hard Limiter

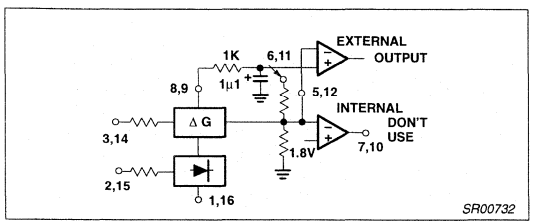


Figure 13. Use of External Op Amp

The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

Figure 13 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either Pin 8 or 9, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the SA570/571 reference (typically about 10μV in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply (+V_{CC} and ground), it must have an input common-mode range down to less than 1.8V.

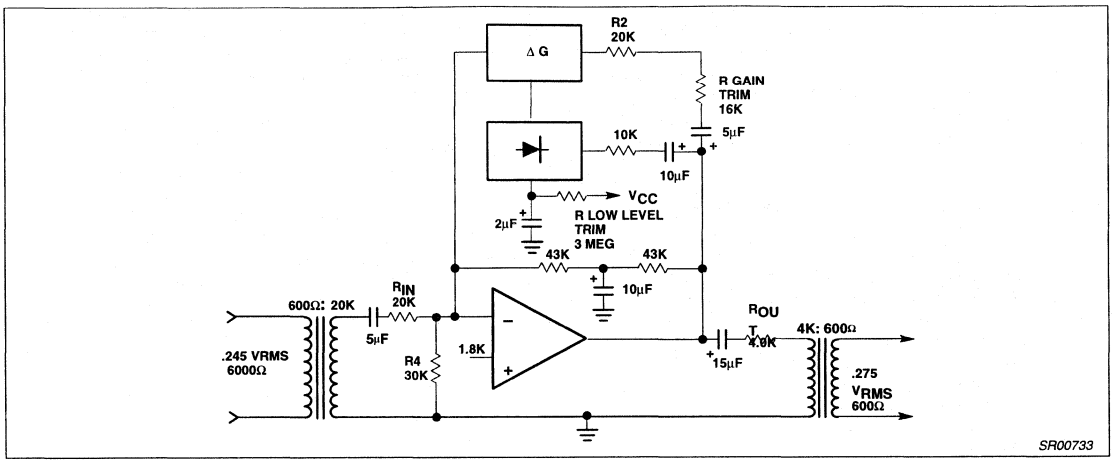


Figure 14. N2 Compressor

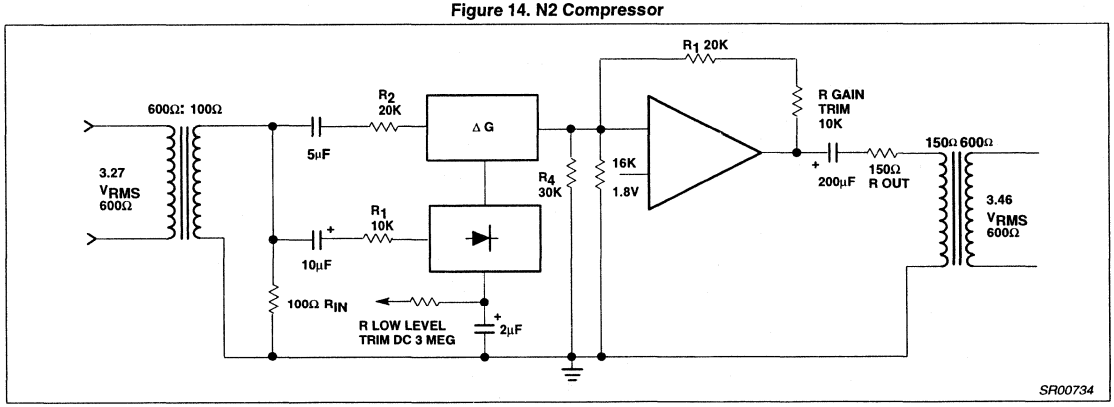


Figure 15. N2 Expandor

N2 COMPANDOR

There are four primary considerations involved in the application of the SA570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.

Figure 14 shows the implementation of an N2 compressor. The input level of $0.245V_{RMS}$ is

stepped up to $1.41V_{RMS}$ by the 600Ω: 20kΩ matching transformer. The 20k input resistor properly terminates the transformer. An internal 20kΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4kΩ output resistor and the 4kΩ: 600Ω output transformer.

The $0.275V_{RMS}$ output level requires a 1.4V op amp output level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

$$R_2 = \frac{Gain^2 \times 2\ R_3\ V_{IN\ avg}}{R_1\ I_B}$$

$$= \frac{1^2 \times 2 \times 20k \times 1.27}{10k \times 140\mu A}$$

$$= 36.3k$$

The external resistance required will thus be 36.3k–20k=16.3k.

The Bell-compatible low level tracking characteristic is provided by the low level trim resistor from C_{RECT} to V_{CC}. As shown in Figure 6, this will skew the system to a 1:1 transfer characteristic at low levels. The 2μF rectifier capacitor provides attack and release times of 3ms and 13.5ms, respectively, as shown in Figures 10 and 11. The R-C-R network around the op amp provides DC feedback to bias the output at DC.

An N2 expandor is shown in Figure 15. The input level of $3.27V_{RMS}$ is stepped down to 1.33V by the 600Ω:100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor

and the 150Ω:600Ω output transformer. With this configuration, the 3.46V transformer output requires a 3.46V op amp output. To obtain this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation

$$R_3 = \frac{R_1\ R_2\ I_B\ \text{Gain}}{2\ V_{IN}\ \text{avg}}$$

$$= \frac{10k\ \text{x}\ 20k\ \text{x}\ 140\mu A\ \text{x}\ 2.6}{2\ \text{x}\ 1.20}$$

$$= 30.3k$$

An external addition to R_3 of 10k is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{RECT} to V_{CC} of about 3M provides matching of the Bell low-level tracking curve, and the 2µF value of C_{RECT} provides the proper attack and release times. A 16k resistor from the summing node to ground biases the output to $7V_{DC}$.

VOLTAGE-CONTROLLED ATTENUATOR

The variable gain cell in the SA570/571 may be used as the heart of a high quality voltage-controlled amplifier (VCA). Figure 16 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of −6dB/V. Trim networks are shown to null out distortion and DC shift, and to fine trim gain to 0dB with 0V of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150µA, (15V and R_{20}=100k), is attenuated a factor of two (6dB) for every volt increase in the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant (C_6×R_1) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a −6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9V of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a 0V bias at A_1's output.

With a 0V control voltage, R_{19} should be adjusted for 0dB gain. At 1V(−6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output DC bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than 0.1% distortion at any gain with a DC output voltage variation of only a few millivolts. The clipping level (140µA into Pin 3, 14) is ±10V peak. A signal-to-noise ratio of 90dB can be obtained.

If several VCAs must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

AUTOMATIC LEVEL CONTROL

The SA570 can be used to make a very high performance ALC as shown in Figure 17. This circuit hook-up is very similar to the basic compressor shown in Figure 2 except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ±1dB for an input range of +14 to −43dB at 1kHz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$\text{Output level} = \frac{R_1\ R_2\ I_B}{2\ R_3}\ \left(\frac{V_{IN}}{V_{IN}\ (\text{avg})}\right)$$

$$I_B = 140mA$$

$$\text{Gain} = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (\text{avg})}\ \text{where}$$

$$\frac{V_{IN}}{V_{IN}\ (\text{avg}} = \frac{\pi}{2\sqrt{2}} = 1.11\ (\text{for sine wave})$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$\text{Gain max} = \frac{\frac{R_1 + R_X}{1.8V}\ \text{x}\ R_2\ \text{x}\ I_B}{2\ R_3}$$

The time constant of the circuit is determined by the rectifier capacitor, C_{RECT}, and an internal 10k resistor.

τ=10k C_{RECT}

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation:

$$\text{THD} = \left(\frac{1\mu F}{C_{RECT}}\right)\left(\frac{1kHz}{\text{freq.}}\right)\ \text{x}\ 0.2\%$$

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 18. Rotation of the dual potentiometer causes the circuit hook-up to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression nor expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1 up to 1:2 expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 18.

HI-FI COMPANDOR

The SA570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple SA570 compressor (Figure 2) is the limited op amp gain at high frequencies.

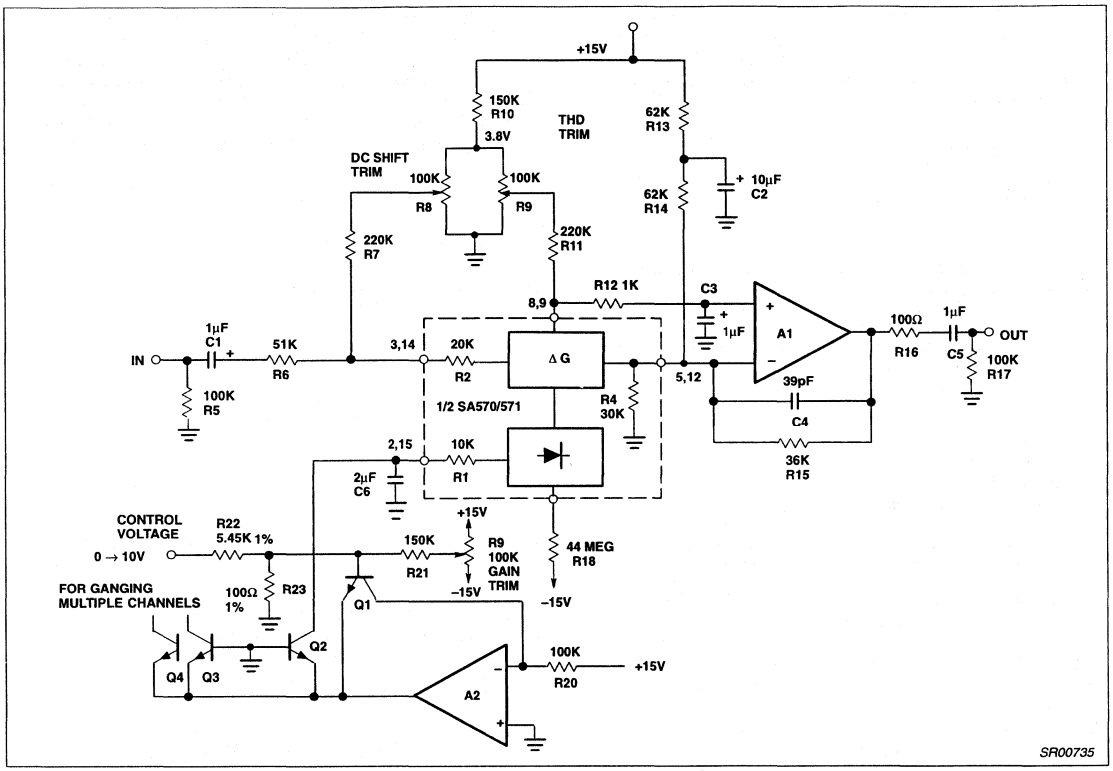


Figure 16. Voltage-Controlled Attenuator

For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about 0.6V/µs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

Figure 20 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 20 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times of the simple expandor and compressor (Figures 1 and 2) become longer at low signal levels. The time constant is not simply $10k \times C_{RECT}$, but is really:

$$\left(10k + 2\left(\frac{0.026V}{I_{RECT}}\right)\right) \times C_{RECT}$$

When the rectifier input level drops from 0dBm to –30dBm, the time constant increases from $10.7k \times C_{RECT}$ to $32.6k \times C_{RECT}$. In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

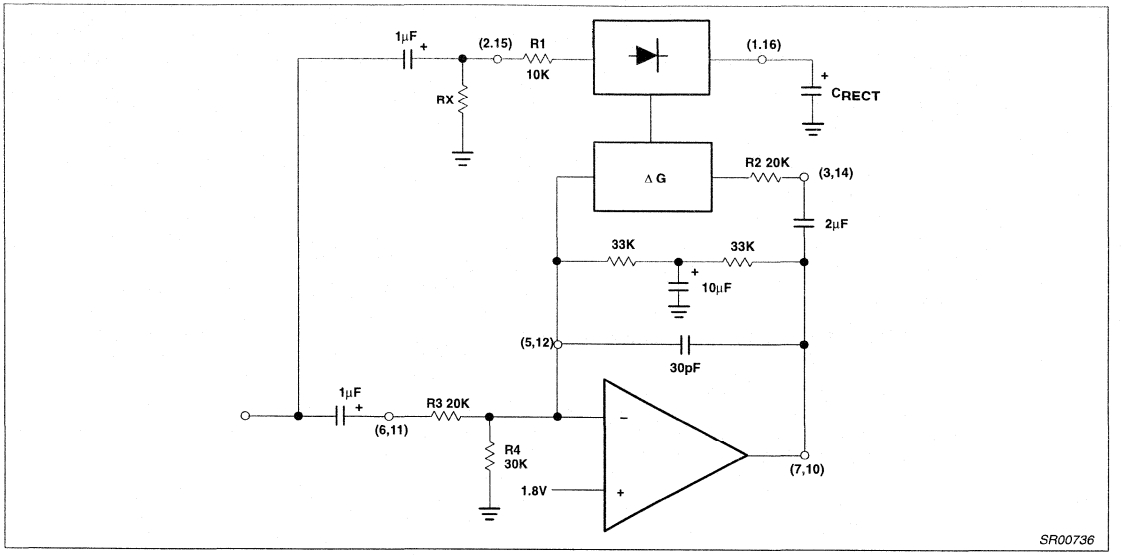


Figure 17. Automatic Level Control

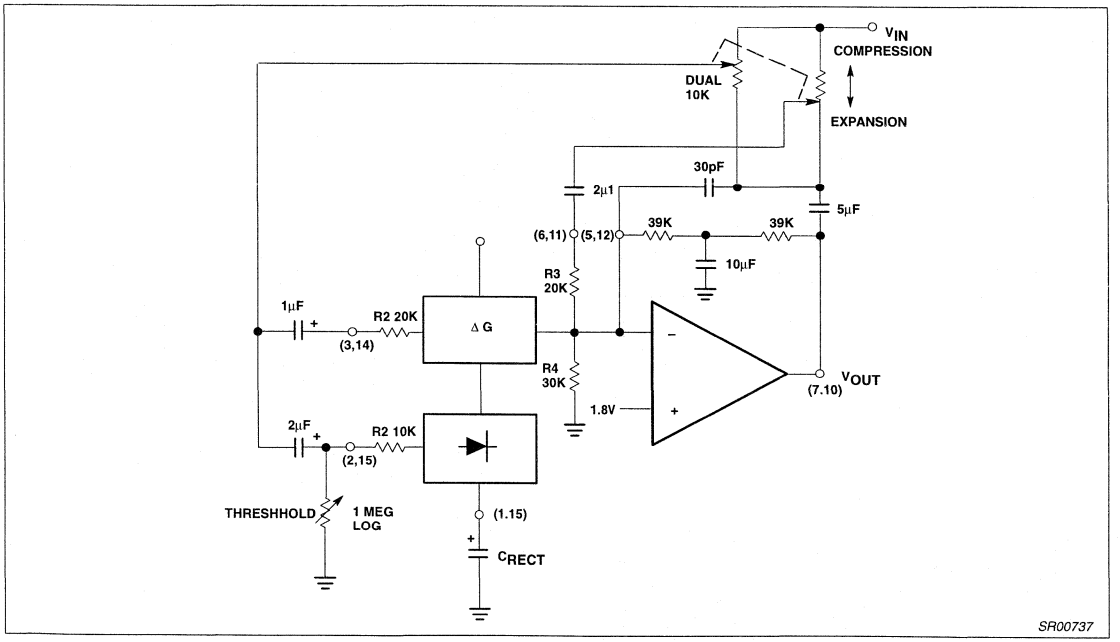


Figure 18. Variable Slope Compressor-Expandor

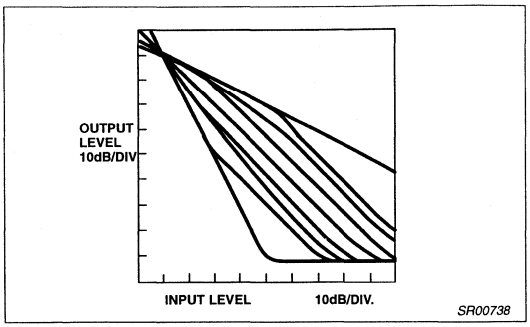


Figure 19. Typical Input-Output Tracking Curves of Variable Ratio Compressor-Expandor

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded, the output will attempt to swing rail to rail. This compressor is limited to approximately a $7V_{P-P}$ output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1µF seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system is changing gain, the change in the background noise level can sometimes be heard.

The compressor in Figure 20 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 21. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0dB. Trim networks are shown for distortion (THD) and DC shift. The distortion trim should be done first, with an input of 0dB at 10kHz. The DC shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

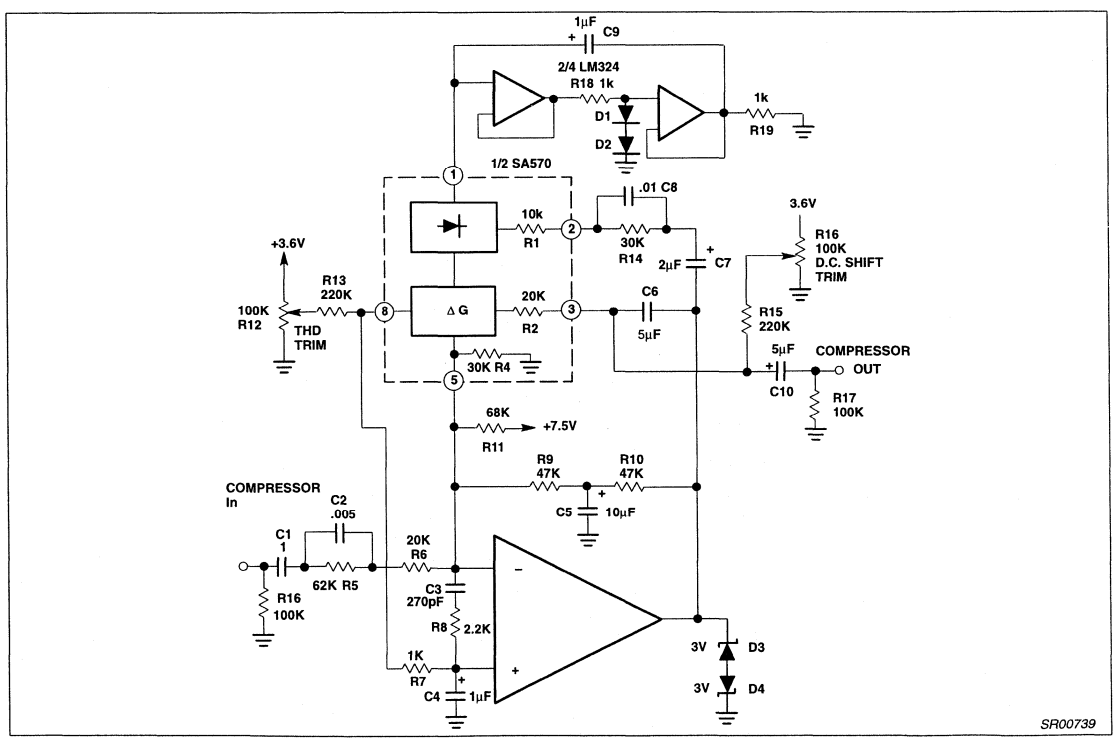


Figure 20. Hi-Fi Compressor With Pre-emphasis

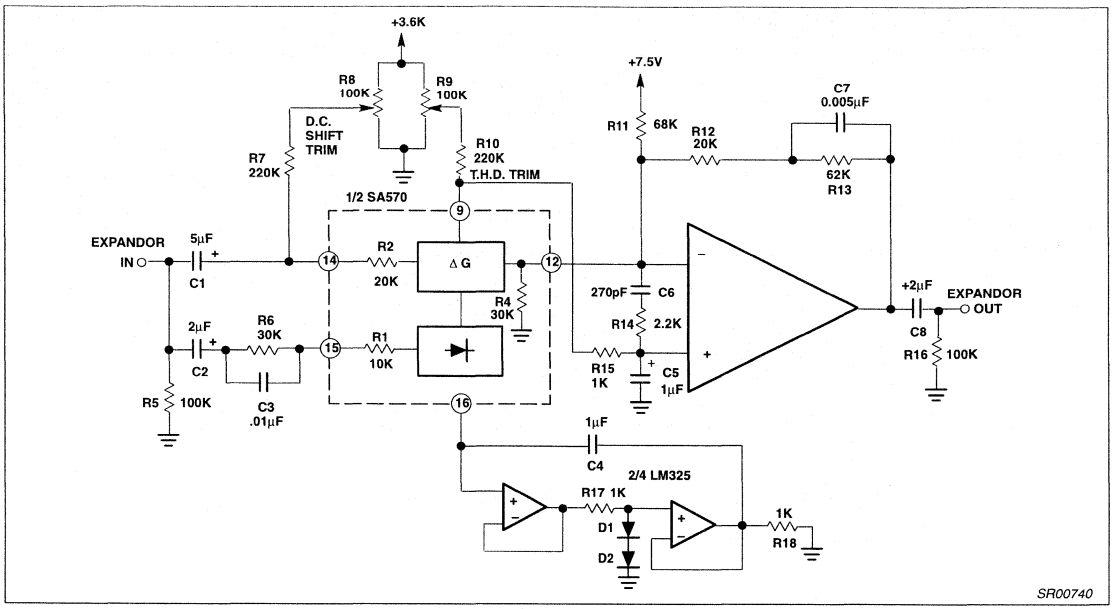
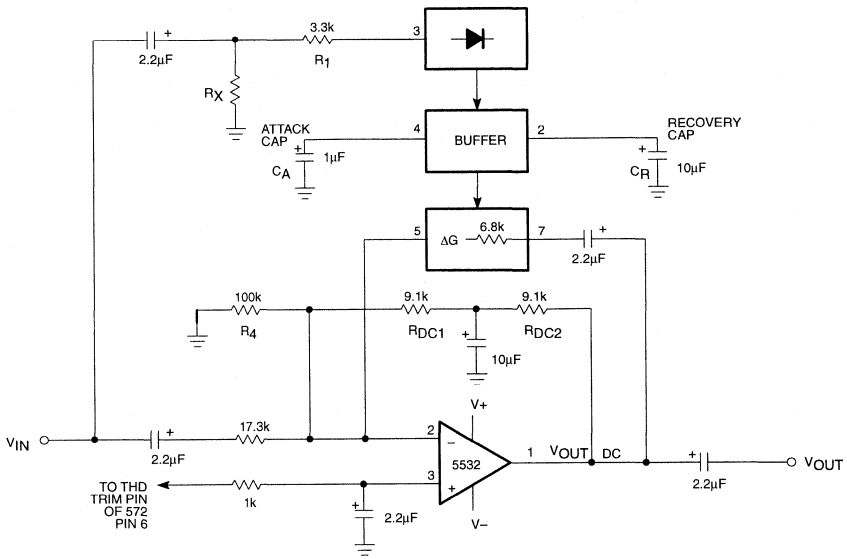


Figure 21. Hi-Fi Expandor With De-emphasis

Automatic level control using the NE572

AN175

NE572 AUTOMATIC LEVEL CONTROL



$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

WHERE: $R_4 = 100k$
$R_{DC1} = R_{DC2} = 9.1k$
$V_{REF} = 2.5V$

$$\text{OUTPUT LEVEL} = \left(\frac{R_1 R_2 I_B}{2R_3}\right)\left(\frac{V_{IN}}{V_{IN(avg)}}\right)$$

WHERE: $R_1 = 6.8k$ (Internal)
$R_2 = 3.3k$
$R_3 = 17.3k$
$I_B = 140\mu A$

$$\text{Gain} = \frac{R_1 R_2 I_B}{2R_3 V_{IN}\ (avg)}$$

ATTACK TIME = (10k) C_A

RECOVERY TIME = (10k) C_R

TO LIMIT THE GAIN AT VERY LOW INPUT LEVELS, ADD R_X:

$$\text{GAIN MAX.} = \frac{\frac{R_1 + R_X}{2.5V} \times R_2 \times I_B}{2R_3}$$

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11$$

(FOR SINE WAVES)

NOTE:
Pin numbers are for side A of the NE572.

SR00753

Compandor cookbook AN176

Compandors are versatile, low cost, dual-channel gain control devices for audio frequencies. They are used in tape decks, cordless telephones, and wireless microphones performing noise reduction. Electronic organs, modems and mobile telephone equipment use compandors for signal level control.

So what is companding? Why do it at all? What happens when we do it? Compandor is the contraction of the two words compressor and expandor. There is one basic reason to compress a signal before sending it through a telephone line or recording it on a cassette tape: to process that signal (music, speech, data) so that all parts of it are above the inherent noise floor of the transmission medium and yet not running into the max. dynamic range limits, causing clipping and distortion. The diagrams below demonstrate the idea; they are not totally correct because in the real world of electronics the 3kHz tone is riding on the 1kHz tone. They are shown separated for better explanation.

Figure 1 is the signal from the source. Figure 2 shows the noise always in the transmission medium. Figure 3 shows the max limits of the transmission medium and what happens when a signal larger than those limits is sent through it. Figure 4 is the result of compressing the signal (note that the larger signal would not be clipped when transmitted).

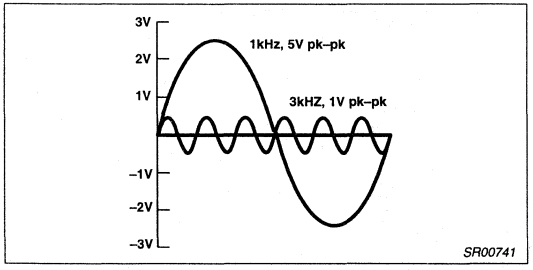


Figure 1. Original Signal Input

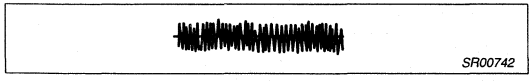


Figure 2. Wide-Band Noise Floor of Transmission Line

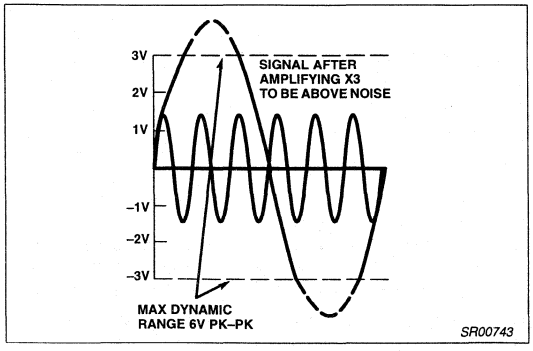


Figure 3.

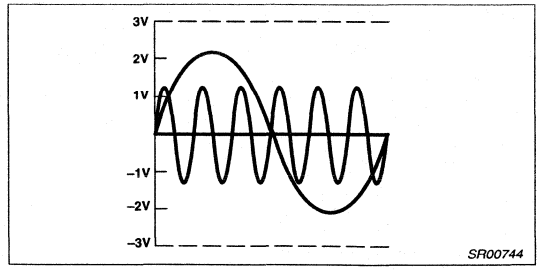


Figure 4. Signal After Compression

The received/playback signal is processed (expanded) in exactly the same — only inverted — ratio as the input signal was compressed. The end result is a clean, undistorted signal with a high signal-to-noise ratio.

This document has been designed to give the reader a basic working knowledge of the Signetics Compandor family. The analyses of three primary applications will be accompanied by "recipes" describing how to select external components (for both proper operation and function modification). Schematic and artwork for an application board are also provided. For comprehensive technical information consult the Compandor Product Guide or the Linear Data Manual.

The basic blocks in a compandor are the current-controlled variable gain cell (ΔG), voltage-to-current converter (rectifier), and operational amplifier. Each Signetics compandor package has two identical, independent channels with the following block diagrams (notice that the 570/71 is different from the 572).

The operational amplifier is the main signal path and output drive.

BLOCK DIAGRAMS

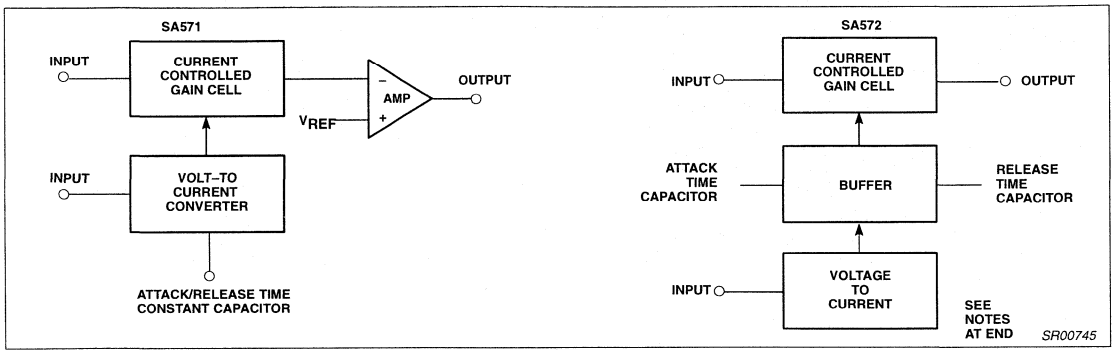


Figure 5. Block Diagrams

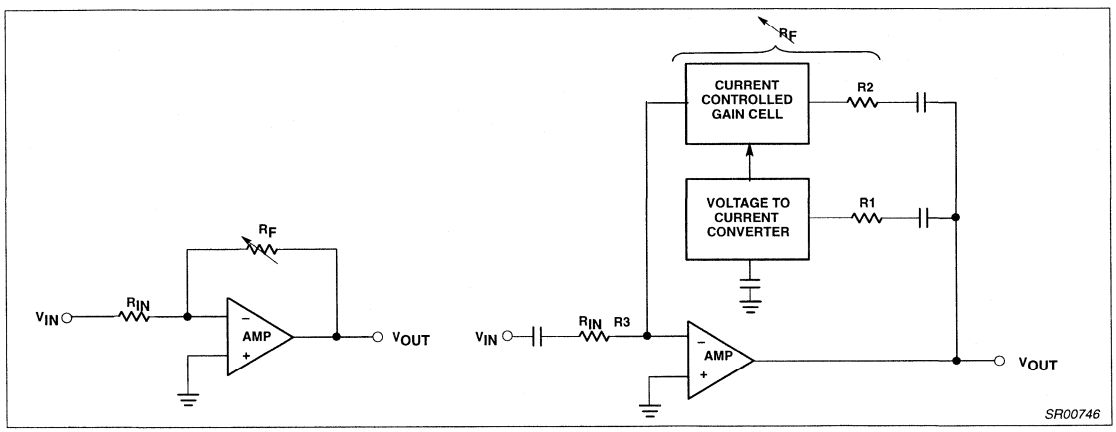


Figure 6. Basic Compressor

The full-wave averaging rectifier measures the AC amplitude of a signal and develops a control current for the variable gain cell.

The variable gain cell uses the rectifier control current to provide variable gain control for the operational amplifier gain block.

The compandor can function as a Compressor, Expandor, and Automatic Level Controller or as a complete compressor/expandor system as described in the following:

1) The COMPRESSOR function processes uncontrolled input signals into controlled output signals. The purpose of this is to avoid distortion caused by a narrow dynamic range medium, such as telephone lines, RF and satellite transmissions, and magnetic tape. The Compressor can also limit the level of a signal.

2) The EXPANDOR function allows a user to increase the dynamic range of an incoming compressed signal such as radio broadcasts.

3) The compressor/expandor system allows a user to retain dynamic range and reduce the effects of noise introduced by the transmission medium.

4) The AUTOMATIC LEVEL CONTROL (ALC) function (like the familiar automatic gain control) adjusts its gain proportionally with the input amplitude. This ALC circuit therefore transforms a widely varying input signal into a fixed amplitude output signal without clipping and distortion.

HOW TO DESIGN COMPANDOR CIRCUITS

The rest of the cookbook will provide you with basic compressor, expandor, and automatic level control application information. A SA571 has been used in all of the circuits. If high-fidelity audio or separately programmable attack and decay time are needed, the SA572 with a low noise op amp should be used.

The compressor (see Figure 6) utilizes all basic building blocks of the compandor. In this configuration, the variable gain cell is placed in the feedback loop of the standard inverting amplifier circuit. The gain equation is $A_V = -R_F/R_{IN}$. As shown above, the variable gain cell acts as a variable feedback resistor (R_F) (See Figure 6).

As the input signal increases above the crossover level of 0dB, the variable resistor decreases in value. This causes the gain to decrease, thus limiting the output amplitude.

Below the crossover level of 0dB, an increase in input signal causes the variable resistor to increase in value, thereby causing the output signal's amplitude to increase.

In the compressor configuration, the rectifier is connected to the output.

The complete equation for the compressor gain is:

$$\text{Gain comp.} = \left[\frac{R_1 R_2 I_B}{2 R_3 V_{IN}(avg)}\right]^{\frac{1}{2}}$$

where: $R_1 = 10k$
$R_2 = 20k$
$R_3 = 20k$
$I_B = 140\mu A$

$V_{IN}(avg)=0.9(V_{IN(RMS)})$

COMPRESSOR RECIPE

1) DC bias the output half way between the supply and ground to get maximum headroom. The circuit in Figure 7 is designed around a system supply of 6V, thus the output DC level should be 3V.

$V_{OUT\ DC}=(1+(2R_{DC}/R_4))\ V_{REF}$

where: $R_4=30k$
$V_{REF}=1.8V$
R_{DC} is external

manipulating the equation, the result is. . .

$$R_{DC} = \left(\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right)\frac{R_4}{2}$$

Note that the $C_{(DC)}$ should be large enough to totally short out any AC in this feedback loop.

2) Analyze the OUTPUT signal's anticipated amplitude.

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will also need to be increased.

By limiting the peak input currents we avoid signal distortion.

3) The input and output coupling caps need to be large enough not to attenuate any desired frequencies ($X_C=1/(6.28xf)$).
4) The C_{RECT} should be 1µF to 2µF for initial setup. This directly affects Attack and Release times.
5) An input buffer may be necessary if the source's output impedance needs matching.
6) Pre-emphasis may be used to reduce noisepumping, breathing, etc., if present. See the SA 571 data sheet for specific details.
7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. Refer to data sheet for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.

8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network. (This technique prevents infinite compression at low input levels.)

The EXPANDOR utilizes all the basic building blocks of the compandor (see Figure 8). In this configuration the variable gain cell is placed in the inverting input lead of the operational amplifier and acts as a variable input resistance, R_{IN}. The basic gain equation for operational amplifiers in the standard inverting feedback loop is $A_V=-R_F/R_{IN}$.

As the input amplitude increases above the crossover level of 0dBM, this variable resistor decreases in value, causing the gain to increase, thus forcing the output amplitude to increase (refer to Figure 11).

Below the crossover level, an increase in input amplitude causes the variable resistor to increase in value, thus forcing the output amplitude to decrease.

The complete equation for the expandor gain is:

Gain expandor=$(2R_3V_{IN}(avg))/R_1R_2I_B$

where: $R_1 = 10k$
$R_2 = 20k$
$R_3 = 20k$
$I_B = 140\mu A$

$V_{IN}(avg)=0.9\ (V_{IN(RMS)})$

In the expandor configuration the rectifier is connected to the input.

EXPANDOR RECIPE

1) DC bias the output halfway between the supply and ground to get maximum headroom. The circuit in Figure 9 is designed around a system supply of 6V so the output DC level should be 3V.

$V_{OUT\ DC}=(1+R_3/R_4)V_{REF}$

where: $R_3 = 20k$
$R_4 = 30k$
$V_{REF} = 1.8V$

Note that when using a supply voltage higher than 6V the DC output level should be adjusted. To increase the DC output level, it is recommended that R_4 be decreased by adding parallel resistance to it. (Changing R_3 would also affect the expandor's AC gain and thus cause a mismatch in a companding system.)

2) Analyze the input signal's anticipated amplitude:

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will also need to be increased. (see INGREDIENTS)

By limiting the peak input currents we avoid signal distortion.

3) The input and output decoupling caps need to be large enough not to attenuate any desired frequencies.

4) The C_{RECT} should be 1µF to 2µF for initial setup.

5) An input buffer may be necessary if the source's output impedance needs matching.

6) De-emphasis would be necessary if the complementary compressor circuit had been pre-emphasized (as in a tape deck application). See the Hi-Fi Expandor application in the Linear Data Manual.

7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. See Linear Data Manual for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.

8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network (see Linear Data Manual). (This technique prevents infinite expansion at low input levels.)

In the ALC configuration, (Figure 10), the variable gain cell is placed in the feedback loop of the operational amplifier (as in the Compressor) and the rectifier is connected to the input.

As the input amplitude increases above the crossover point, the overall system gain decreases proportionally, holding the output amplitude constant.

As the input amplitude decreases below the crossover point, the overall system gain increases proportionally, holding the output amplitude at the same constant level.

The complete gain equation for the ALC is:

$$\text{Gain} = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)}$$

$$\text{Output Level} = \frac{R_1\ R_2\ I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN}\ (avg)}\right)$$

$$\text{where } \frac{V_{IN}}{V_{IN}\ (avg)} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine wave)}$$

Note that for very low input levels, ALC may not be desired and to limit the maximum gain, resistor R_X has been added. The modified gain equation is:

$$\text{Gain max.} = \frac{(R_1 + R_X) \cdot R_2 \cdot I_B}{2\ R_3}$$

$R_X \cong$ ((desired max gain)×26k)–10k

INGREDIENTS

[Application guidelines for internal and external components (and input/output constraints) needed to tailor (cook) each of the three entrees (applications) to your taste.]

R_1 (10kΩ) limits input current to the rectifier. This current should not exceed an AC peak value of ±300µA. An external resistor may be placed in series with R_1 if the input voltage to the rectifier will exceed ±3.0V peak (i.e., 10k×300µA=3.0V).

R_2 (20kΩ) limits input current to the variable gain cell. This current should not exceed an AC peak value of ±140µA. Again, an external resistor has to be placed in series with R_2 if the input voltage to the variable gain cell exceeds ±2.8V (i.e., 20k×140µA).

R_3 (20kΩ) acts in conjunction with R_4 as the feedback resistor (R_F) (expandor configuration) in the equation. (R_3's value can be either reduced or increased externally.) However, it is recommended that R_4 be the one to change when adjusting the output DC level.

R_4 (30kΩ) acts as the input resistor (R_{IN}) in the standard non-inverting op amp circuit. (Its value can only be reduced.)

$V_{OUT\ DC}=(1+(R_3/R_4))V_{REF}$
(for the Expandor)
$V_{OUT\ DC}=(1+(2R_{DC}/R_4))V_{REF}$
(for the Compandor, ALC)

[The purpose of these DC biasing equations is to allow the designer to set the output halfway between the supply rails for largest headroom (usually some positive voltage and ground).]

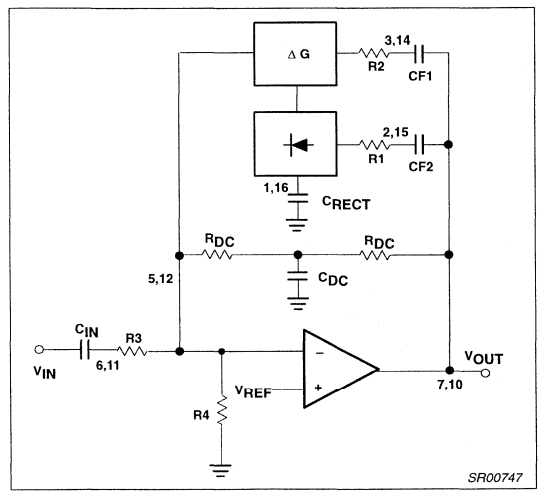


Figure 7. Basic Compressor

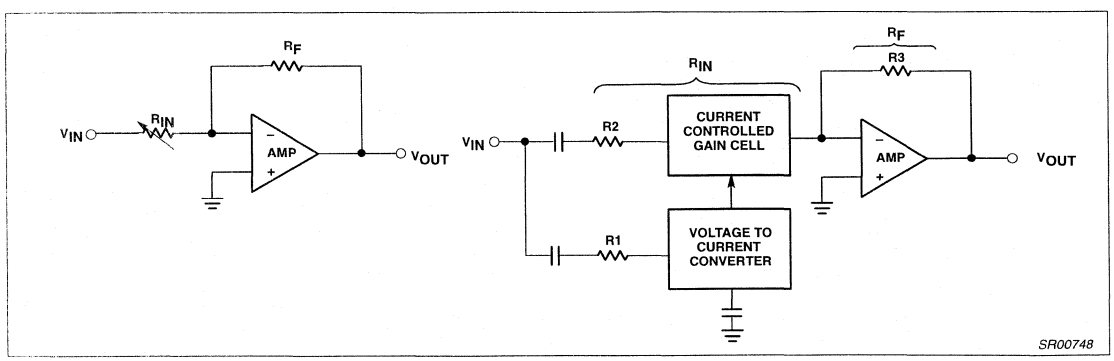


Figure 8. Basic Expandor

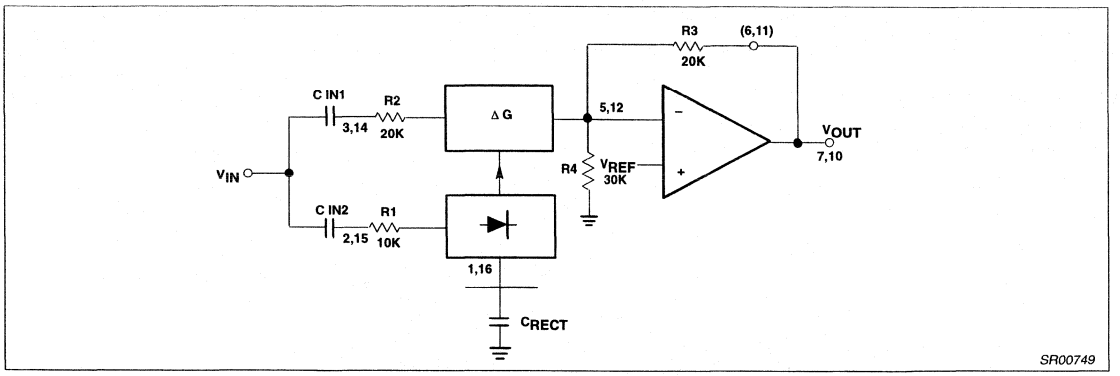


Figure 9. Basic Expandor

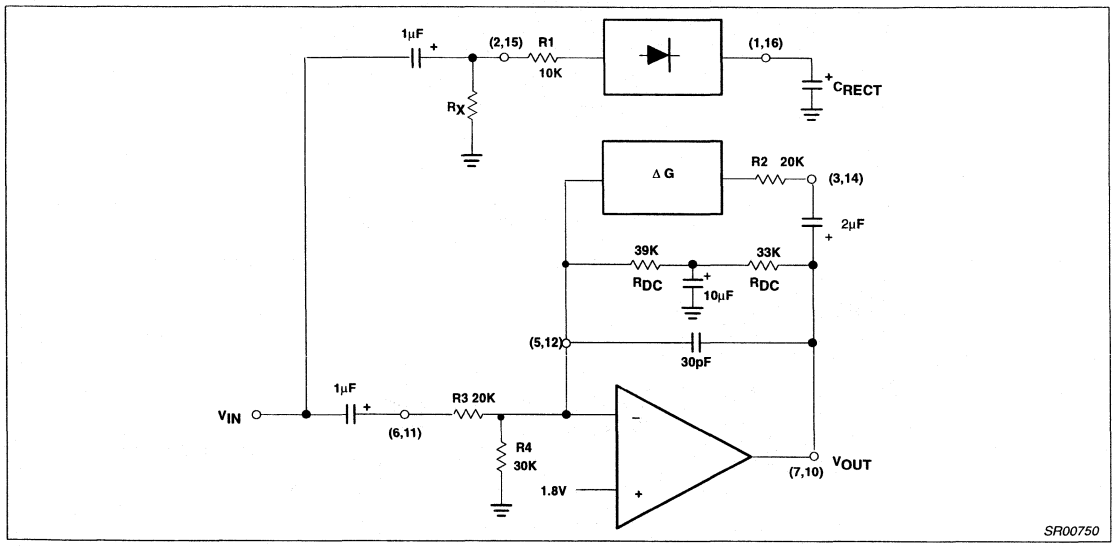


Figure 10. Automatic Level Control

C_{DC} acts as an AC shunt to ground to totally remove the DC biasing resistors from the AC gain equation.

C_F caps are AC signal coupling caps.

C_{RECT} acts as the rectifier's filter cap and directly affects the response time of the circuit. There is a trade-off, though, between fast attack and decay times and distortion.

The time constant is: $10k \times C_{RECT}$

The total harmonic distortion (THD) is approximated by:

$THD \cong (1\mu F/C_{RECT})(1kHz/freq.) \times 0.2\%$

NOTES:
The SA572 differs from the 570/571 in that:
1. There is no internal op amp.
2. The attack and release times are programmed separately.

SYSTEM LEVELS OF A COMPLETE COMPANDING SYSTEM

Figure 11 demonstrates the compressing and expanding functions:

Point A represents a wide dynamic range signal with a maximum amplitude of +16dB and minimum amplitude of –80dB.

Point B represents the compressor output showing a 2:1 reduction in dynamic range (–40dB is increased to –20dB, for example). Point B can also be seen as the dynamic range of a transmission medium. Transmission noise is present at the –60dB level from Point B to Point C.

Point C represents the input signal to the expandor.

Point D represents the output of the expandor. The signal transformation from Point C to D represents a 1:2 expansion.

Expansion and one channel of Compression (which can be switched to Automatic Level Control).

APPLICATION BOARD

Shown below is the schematic (Figure 12) for Signetics' SA571 evaluation/demo board. This board provides one channel of

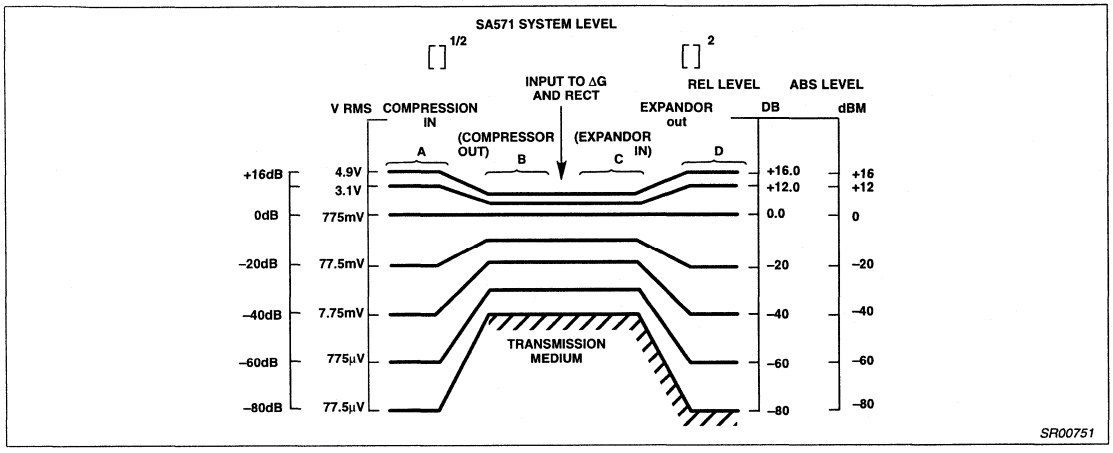


Figure 11. System Levels of a Complete Companding System

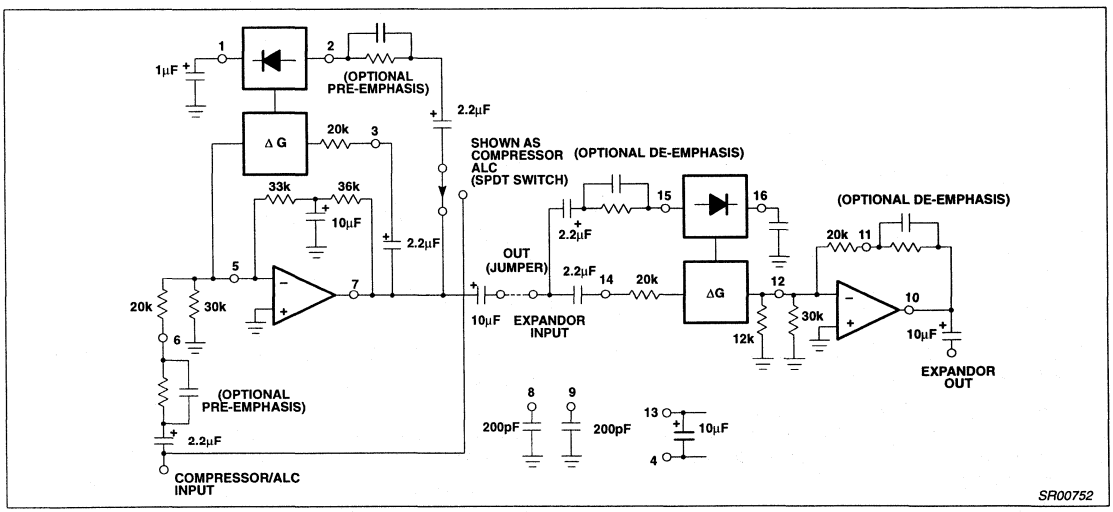


Figure 12.

Evaluation of the SA601/SA606 demoboard AN1000

Author: Randall Yogi

INTRODUCTION

Philips Semiconductors is dedicated to playing a major role in the wireless communication market. Key to this goal is Philips' commitment for design assistance at all levels. This is the purpose of the SA601/SA606 combo-board. The SA601 is a combined RF amplifier and mixer designed for high-performance low-power communication systems from 800-1200MHz. The SA606 is a low-voltage high performance monolithic FM IF system that, when combined with the SA601, results in a high performance double down-conversion FM receiver. To better support this type of application, Philips has combined the SA601 and SA606 ICs onto a single board which highlights how well the SA601 and the SA606 work together. This application note explains how to overcome many of the technical problems that might arise, and shows how to achieve the best possible performance from the SA601 and SA606. Test results are also included.

This application note is divided into four main sections:

I. Overview of the SA601/SA606 combination board
II. Layout
    A. Schematic, Components Specifics and Parts List
    B. Impedance Matching
III. Performance
    A. Test Setup and Procedures
    B. Test Data and Results
IV. Conclusion
    A. Q/A section

I. OVERVIEW

Both the SA601 and the SA606 are designed for portable, low voltage, low power communication applications. For a better understanding of what is involved in combining these boards, or for more information regarding the individual boards, please review application notes AN1777 (for the SA601) and AN1993-AN1996 (for the Second-IF ICs) which can be found in the Philips RF/Wireless Communications Data Handbook, IC17.

The SA601/SA606 demoboard is designed to meet AMPS specifications. Section 2 of the EIA Interim Standard, "Recommended Minimum Standard for 800MHz Cellular Subscriber Units" (EIA/IS-19-B), was consulted as a guide. Specific sections used were:

2.3.1 RF Sensitivity
2.3.2 Adjacent and Alternate Channel Desensitization
2.3.3 Intermodulation Spurious-Response Interference
2.3.4 Protection Against Spurious Response

Measured results demonstrate that the SA601/SA606 demoboard successfully meets and surpasses the specifications listed above.

Although the SA601/SA606 demoboard is designed to meet AMPS cellular specifications, it can be modified for other analog cellular specifications such as TACS, ETACS, and NAMPS. The demoboard could also be configured for ISM band (902MHz – 928MHz) applications.

II. LAYOUT

The layout of any high frequency board is critical and always challenging. As stated previously, understanding each board separately is the key to combining them. Before a single-board layout was attempted, the SA601 and the SA606 individual demoboards were cascaded together, along with an RF SAW filter and a 1st IF SAW filter. The performance with this configuration was satisfactory, thus permitting the next step of combining everything on one board (Figure 2). As with the original SA601 and SA606 individual demoboards, the majority of the components are on one side of the board.

The SA601/SA606 demoboard layout can be configured to provide two different types of matching to the IF SAW filter (Figure 1). It can be configured as a 50 Ω impedance match, or a high impedance match to the 83.161MHz SAW filter. The 50 Ω impedance matching network allows a designer to evaluate or troubleshoot each individual block. For example, a designer can find conversion gain measurements of the SA601 or measure SINAD for only the SA606 block.

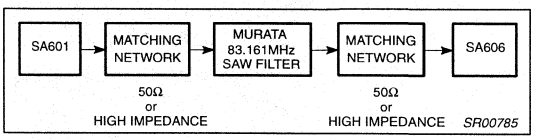


Figure 1. Block Diagram: Matching 1st IF SAW Filter

The 50 Ω impedance match can also be used as a reference for the high impedance match. Because 50 Ω impedance matching requires more components, a high impedance match is preferred. Matching for high impedance can be difficult, but since each block is optimized through a 50 Ω impedance match, the designer has a target/reference. For example, if 12dB SINAD = -120dBm for a 50 Ω impedance matched system, ideally a high impedance match should yield the same results, if not better.

The majority of the single-board layout was adapted from the individual application demoboards, except for the two SAW filters (the image rejection filter centered at 881MHz and the 83.161MHz SAW filter). The layout for the two filters required additional design work. The 881MHz image-rejection SAW filter was placed between the LNA-Out and the Mixer-In of the SA601. Placement of the 881MHz image reject SAW filter, whether it was on the top or bottom of the board, did not have a dramatic impact on performance. This was because isolation between the LNA-Out and the Mixer-In trace had already been considered in the SA601 demoboard. However, because of its high Q, narrowband, and high impedance, the 83.161MHz SAW filter was much more difficult to position. Its placement was critical in passing AMPS specification 2.3.4 Protection Against Spurious-Response Interference. The specification was met with margin to spare by moving the Mixer-Out (Pins 13 and 14) of the SA601 as far away as possible from RF-In (Pin 1) of the SA606.

Schematic, Components Specifics, and Parts List

The schematic shown in Figure 3 is for both 50 Ω impedance matching and high impedance matching to the 83.161MHz SAW filter. The schematic shows the configuration for 50 Ω impedance matching. By making the modifications listed in the box on the bottom right of the schematic (Figure 3), the board can be configured for a high impedance match.

Table 1 lists the basic function of each external component for the schematic shown in Figure 3. This may help answer any questions that arise about the specifics of the board.

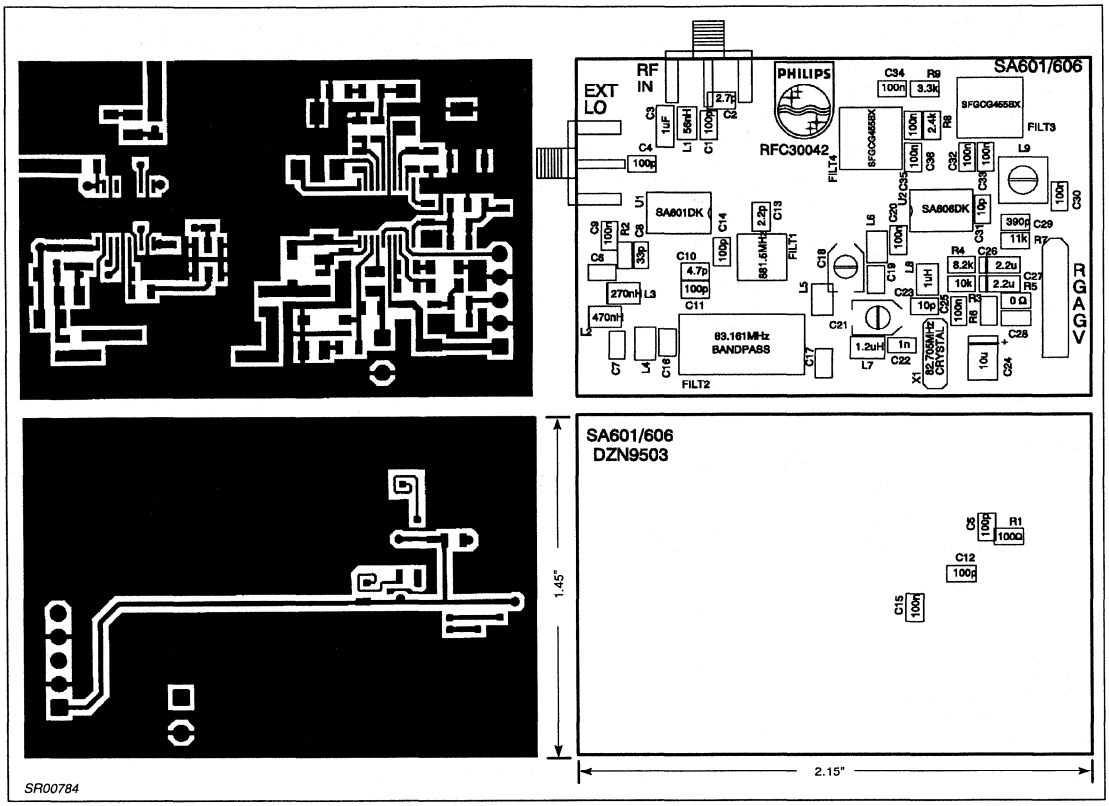


Figure 2. Layout of the SA601/SA606 Demoboard (Not Actual Size)

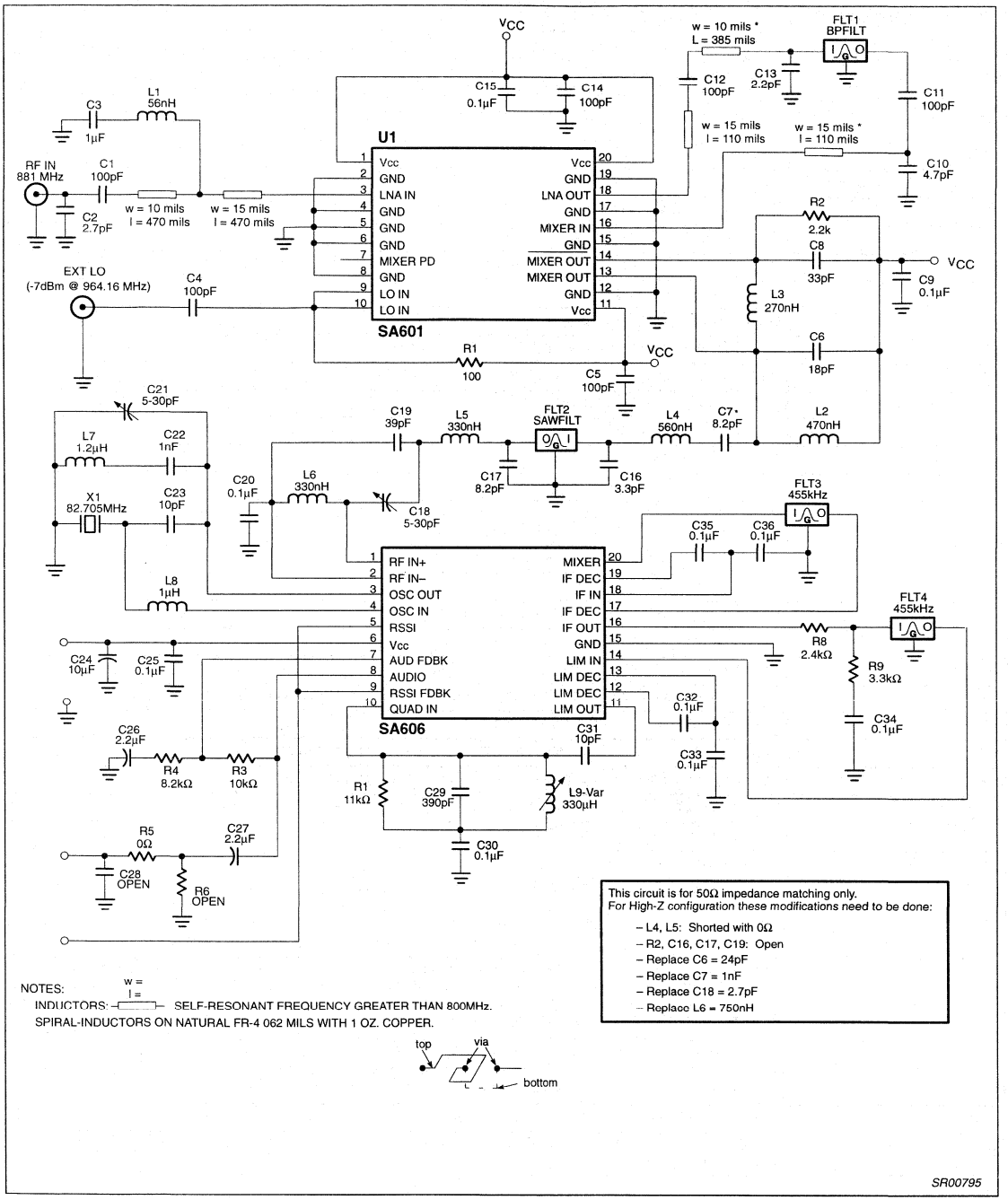


Figure 3. Schematic of the SA601/SA606 Demoboard

Table 1. Components List: Description of Functionality

Part #	Description
C1	LNA Mixer input DC blocking cap
C2	Part of the matching network that optimizes the return loss while minimizing the degradation of the noise figure
C3	Voltage compensation cap for the LNA
C4	LO DC blocking cap
C5, C9, C14, C15, C24, C25	Supply bypassing
C6, C8, L3	Part of the differential to single-ended translation circuit of the mixer out
C7, L2	Part of the matching network of the mixer output
C10, C13	Part of the matching network that optimizes the return loss while minimizing the degradation of the noise figure
C11	Mixer Input DC blocking cap
C12	LNA Output DC blocking cap
C16, C17, L4, L5	Part of the matching network of the 83.161MHz SAW filter
C18, C19, L6	Part of the tapped-C network that matches the RF input of the SA606
C20	AC grounds Pin 2, the RF input of the SA606
C21, C22, C23, L7, L8	Colpitts oscillator network
C26, C34	AC de-coupling cap
C27	DC blocking cap
C28, R5, R6	Part of the filter network that filters 3kHz-15kHz on the SA7025 (Low-voltage 1GHz fractional-N synthesizer). This network is only used on the 7025 IC production tester.
C29, L9	Quad tank component that resonates at 455kHz
C30	AC grounds the quad tank
C31	Provides the 90° phase shift to the phase detector
C32, C33	IF limiter decoupling cap
C35, C36	IF amp decoupling cap
R1	DC pull-up resistor that provides isolation (reduces IF to LO and RF to LO leakage)
R2	Sets output impedance of the Mixer Output
R3	Part of the Audio op-amp that sets a gain of 2dB thus stabilizing distortion
R4	Part of the Audio op-amp that sets a gain of 2dB thus stabilizing distortion
R7	Lowers the Q of the quad tank and thus lowers the S-Curve slope
R8, R9	Part of a network to control linearity of the RSSI
L1	Voltage compensation to LNA
FILT1	Murata SAFC881.5MA70N-TC 881.5MHz bandpass SAW filter: This is a 869MHz to 894MHz bandpass filter. It is used to reject the image frequency (LO + 83.16MHz in our case) and to attenuate the transmit signal (RF-45MHz) leaking through the duplexer so that the SA601 mixer doesn't reach its 1dB compression point from a strong signal leaking through. Some electrical characteristics from Murata are provided (Table 2).
FILT2	Murata SAFC83.161MA51X-TC 83.161MHz SAW filter: 1st-IF filter for attenuating adjacent and alternate channel spurs. The filter plays a larger role in achieving the high performance of the receiver in areas such as dynamic range, spurious performance, and data communication accuracy. The 83.16MHz SAW filter provides a 30kHz bandpass characteristic utilizing electrodes deposited on a piezoelectric substrate. These electrodes form an inter-digitated pattern on the substrate and serve as transducers to launch an acoustic wave. When an RF voltage is applied to one set of transducers, an electric field is generated and causes the acoustic waves to propagate along the surface to an opposite transducer where an output voltage is produced. (See Reference 8, Alan Victor). The Electrical Characteristics for the Murata SAW filter are shown in Table 3.
FILT3, 4	Murata SFGCG455BX-TC 455kHz bandpass filter (30kHz bandwidth).
X1	An 82.705MHz crystal from either HY-Q or Reeves Hoffman is a 3rd overtone crystal used to generate the LO for the SA606

Table 2. Electrical Characteristics of the Murata SAFC881.5MA70N-TC

Tested at 20 ±2°C. Standard condition: Temp = 20 ±2°C. Humidity = 65 ±5%; Applicable condition: Temp = 5 ~ 35°C. Humidity = 45 ~ 85%.

	Item	Requirements	Typical at 20°C (Reference Value in Standard Condition)
6 – 1	Nominal Center Frequency (f_O)	881.5 MHz	–
6 – 2	Insertion Loss I) within 869 ~ 894 MHz (Pass Bandwidth) II) within DC ~ 780 MHz III) within 824 ~ 849 MHz (Duplex Freq. Range) IV) within 970 ~ 2000 MHz	 4.5 dB max. 40 dB max. 20 dB min. 35 dB min.	 3.5 dB 48 dB 30 dB 40 dB
6 – 3	Ripple Deviation (within 869 to 894 MHz)	2.0 dB max.	1.0 dB
6 – 4	V.S.W.R. (within 869 to 894 MHz)	2.5:1 max.	1.7:1
6 – 5	Input / Output Impedance (nominal)	50Ω // 0pF	–

Table 3. Electrical Characteristics of the Murata SAFC83.161MA51X-TC

	Item	Requirements
1.1	Nominal Center Frequency (f_O)	83.161 MHz
1.2	3 dB Bandwidth (from 83.161 MHz)	±15 kHz min.
1.3	Stop Band Attenuation (from Peak Level) 1.3.1 f_O – 1000 kHz to f_O – 930 kHz 1.3.2 f_O – 930 kHz to f_O – 890 kHz 1.3.3 f_O – 890 kHz to f_O – 700 kHz 1.3.4 f_O – 700 kHz to f_O – 400 kHz 1.3.5 f_O – 400 kHz to f_O – 120 kHz 1.3.6 f_O – 120 kHz to f_O – 60 kHz 1.3.7 f_O + 60 kHz to f_O + 120 kHz 1.3.8 f_O + 120 kHz to f_O + 150 kHz 1.3.9 f_O + 150 kHz to f_O + 400 kHz 1.3.10 f_O + 400 kHz to f_O + 1000 kHz	 40 dB min. 70 dB min. 40 dB min. 30 dB min. 40 dB min. 20 dB min. 20 dB min. 40 dB min. 30 dB min. 40 dB min.
1.4	Insertion Loss (at minimum loss point)	5.0 dB max.
1.5	Ripple (within f_O = 15 kHz)	1.5 dB max.
1.6	Group Delay Deviation (within f_O ± 11 kHz)	10 µs max.
1.7	Intermodulation Input Signal : f_O + 60 kHz, f_O + 120 kHz Input Level : –20 dBm	–90 dBm max.

A complete SA601/SA606 demoboard parts list is provided in Table 14 at the end of this document. The parts list includes vendor names and part numbers as a convenience to designers.

Impedance Matching

Matching of the 83.16MHz SAW filter is an involved task. This is because the HP8753C Network Analyzer can only be calibrated for 50 Ω impedance and the 83.16MHz SAW filter has a specified impedance of 850 // -2pF. Refer to Philips application note AN1777 for an explanation of how to setup the calibration for high-impedance. Although calibration at higher impedance is not as accurate as at 50Ω impedance, the results were close enough to get a good impedance match.

Improved impedance matching yields better sensitivity performance because matching of the 83.161MHz SAW filter suppresses unwanted group delay distortion. The response of the 83.161MHz SAW filter is shown in Figure 4. When the filter response is flat, the SAW filter is matched; when it is not, group delay distortion, represented by the hump, is apparent (Figure 4).

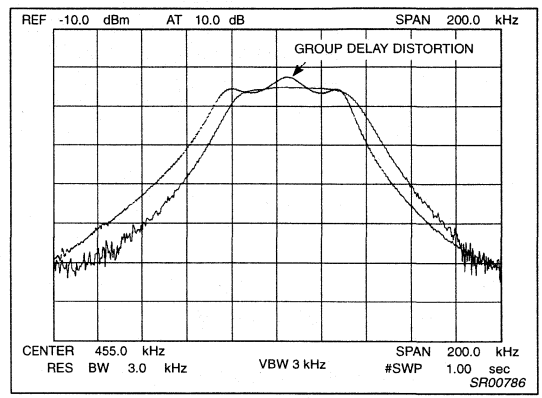


Figure 4. Group Delay Distortion

The steps to match the 83.161MHz SAW filter to a high impedance are as follows:

1. Separate the board into three sections by making two cuts in the trace. Cut 1 is between the Mixer out of the SA601 and the input of the SAW filter. Cut 2 is between the SAW filter output and the RF input of the SA606. (see Figure 5)

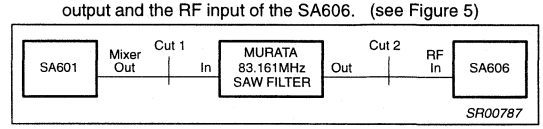


Figure 5. Three Sections of Demoboard

2. Start with SAW filter input of Figure 6 and terminate that side with an 850 Ω resistor.

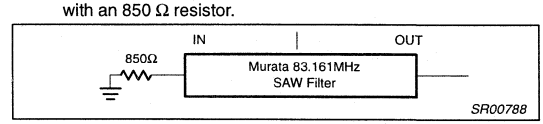


Figure 6. Termination of SAW Filter

3. Measure the impedance of the output of the SAW filter by placing an SMA connector on the trace and marking the corresponding impedance on the Smith Chart.

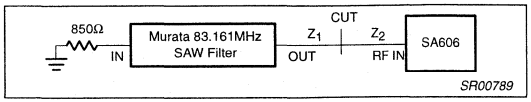


Figure 7. Termination Matching of SAW Filter

4. After identifying the impedance of the SAW filter output indicated by Z_1 in Figure 7, the RF input impedance, Z_2, must be adjusted to provide a conjugate match to Z_1. Z_2 is found on the Smith Chart by reflecting Z_1 about the purely resistive axis represented by the horizontal line running through the center of the Smith Chart.

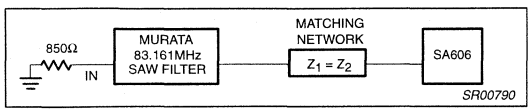


Figure 8. Impedance Matching from SAW Filter to SA606

5. After a conjugate match between Z_1 and Z_2 has been achieved, connect the output of the SAW filter to the matching network. (Figure 8)

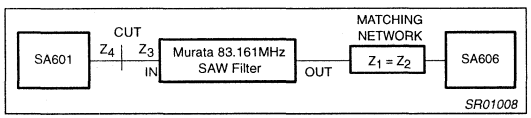


Figure 9. Impedance Matching from SA601 to SAW Filter

6. Remove the 850Ω resistor and measure the impedance at the SAW filter input, Z_3.

7. Obtain a conjugate match to Z_3 at the SA601 mixer output, Z_4, and then connect together (Figure 9).

To double check the matching, remove the 2nd-IF filter from the mixer-out of the SA606 and check the frequency response for any group delay distortion. Figure 4 shows a matched SAW-filter response (flat curve) and a poorly matched response that has group delay distortion.

To make a quick visual check of the frequency response of the board up to the SA606 Mixer output, use the FM modulation of the HP signal generator and spectrum analyzer, as follows:

1. Leave the frequencies (LO and RF) at their respective values. (example: RF = 881MHz and LO = 964.16MHz)

2. Set the FM deviation to 200kHz and the FM modulation to 200Hz on the RF's signal generator.

3. Remove the 2nd-IF filter connected to Pin 20 of the SA606.

4. Set the Spectrum Analyzer sweep time to 1 second, set the center frequency to the 2nd IF frequency (455kHz), and probe Pin 20 with a FET probe. The results should look like the flat response in Figure 4.

III. PERFORMANCE EVALUATION

Procedures

The AMPS specification was used as a guide to test the SA601/SA606 demo board. Sections 2.3.1 through 2.3.4 of the IS-19-B EIA Interim Standard were the procedures used for testing the SA601/SA606 demoboard. These tests were crucial in determining performance of the demoboard.

Figure 10 shows the block diagram of the test setup following the procedures outlined in the AMPS specification.

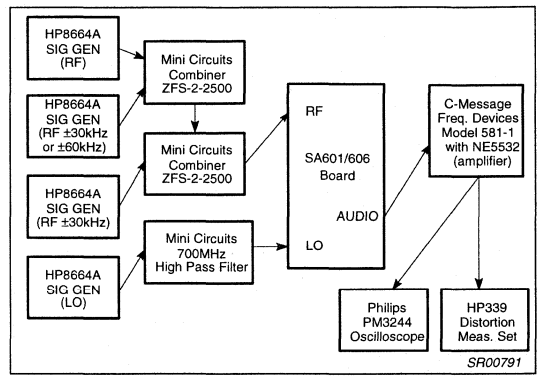


Figure 10. Test Setup for Measuring RF Sensitivity, Adjacent and Alternate Channel Rejection and Spurious Rejection

Transmitter desensitization occurs when the transmit signal from the handset is degrading the performance of the receiver.

To measure transmitter (Tx) desensitization, do the following:

1. Configure the test equipment as shown in Figure 11.

2. Set the Tx signal 45MHz below the RF signal.

3. Measure the Tx power at the Ant of the duplexer on the HP8920A Radio Test Set.

4. Measure 12dB SINAD on the HP8920A Radio Test Set when the Tx signal is on and again when it is off.

5. If there is degradation in sensitivity when the Tx signal is on, the difference of the 12dB SINAD readings is the Tx desensitization.

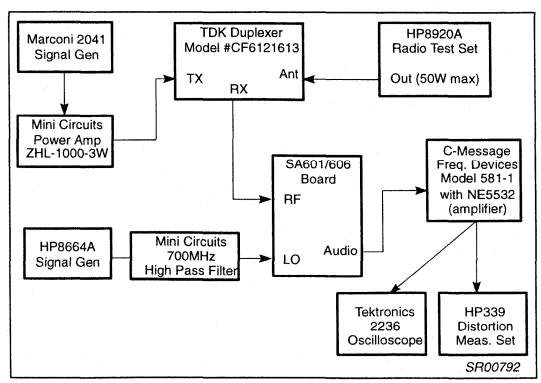


Figure 11. Test Setup for Measuring Transmitter Desensitization

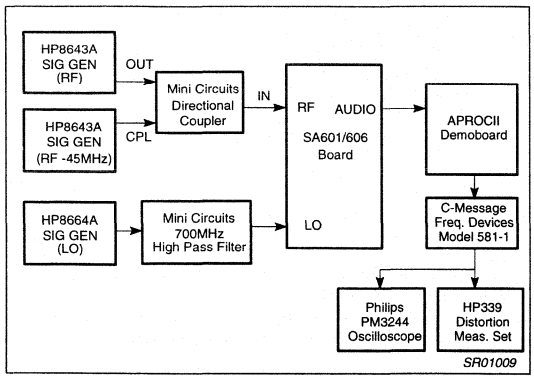


Figure 12. Test Setup for Measuring Transmitter Desensitization Without Duplexer

Because customers' preferences for duplexers vary, Tx desensitization was done another way to evaluate the performance of the SA601/SA606 demoboard.

1. The setup can be configured as shown in Figure 12. Set RF = 869MHz, LO = 957.16MHz and Tx = 824MHz.
2. Set the transmit power to -10dBm because we are assuming that the Tx leakage through the Rx port is that much.
3. Record 12dB SINAD.
4. Reduce the transmit power by 1dB and repeat Step 3.
5. Repeat Step 4 until Tx power reaches -30dBm.
6. Repeat all steps for RF, LO Tx frequencies at mid band (RF = 881MHz, LO = 964.16MHz, Tx = 836MHz) and high band (RF = 894MHz, LO = 977.16MHz, Tx = 849MHz)

Data and Results

Adjacent Channel, Alternate Channel and Intermodulation Spurious Response

The data provided in Tables 4 to 6 shows the sensitivity, adjacent channel, alternate channel, and intermodulation spurious response of the demoboard. The data was taken at V_{CC} = 3V, 4V, and 5V, as well as at three different frequencies.

The data taken was recorded without a duplexer. Adding a duplexer before the RF input will cause sensitivity to decrease by about 3 dB. This board is well within the specified parameters for adjacent channel, alternate channel and intermodulation spurious response rejection in accordance with AMPS specifications.

Protection Against Spurious Response Interference

The next set of data shown is also part of the AMPS specification 2.3.4 Protection Against Spurious Response Interference (Tables 7 to 9). The frequencies tested were the image frequencies that could cause degradation in performance. When using a TDK duplexer (TDK BandPass Filter Model CF6121613), the image frequencies are attenuated, so the image spurs (1047.32MHz) will not degrade the performance of the demoboard. The 2nd IF image frequency is the only frequency that caused problems. This frequency is above the RF by exactly twice the 2nd IF (2 × 455kHz = 910kHz). The problem occurs because, when RF + 910kHz mixes with the 1st LO (964.16MHz), the frequency produced is (RF + 910kHz –1st LO = 82.25MHz). This is equal to the 2nd IF image frequency. When the 2nd IF image frequency is mixed with the crystal oscillator, the frequency produced is the 2nd-IF frequency. The SA606 will demodulate this unwanted frequency, as well as the desired signal.

Example:

RF = 881MHz
LO = 964.16MHz
2nd LO = 82.705MHz
881MHz + 910kHz = 881.91MHz
881.910MHz mixes with the LO (964.16MHz) = 82.25MHz
82.25MHz mixes with the 2nd LO (82.705MHz) = 455kHz

To resolve this problem, the 83.161MHz SAW filter must be isolated. The unwanted frequency was leaking around the SAW filter and into the RF input of the SA606. So the distance between the SA601 mixer out to the RF input of the SA606 was increased by rotating the SAW filter. This solved the problem and the board met the protection against spurious response specification with at least 14dB to spare.

Transmitter desensitization

Another issue was to evaluate how the SA601/SA606 performs with the transmit section of a radio on (transmitter desensitization). Transmitter desensitization will degrade the sensitivity of the receiver if the strong Tx signal is allowed to pass through and cause the SA601 to reach its 1dB compression point in the LNA and the Mixer. Tables 10 to 12 show the results of three test boards for transmitter desensitization as the transmit power is increased from 100mW to 1W.

Using a TDK duplexer (TDK BandPass Filter Model CF6121613), the board performed well. At most, the board degraded by 2dB from the transmitter desensitization.

Since most customers will not want to use the TDK duplexer, Tx desensitization was done another way, as explained in the procedures. Table 13 show the results. The results show that with a duplexer that has Tx leakage of -14dBm or less through the Rx port, the SA601/SA606 will meet the sensitivity requirement according to IS-19-B (-116dBm for 12 dB SINAD), assuming the duplexer has 3dB of loss.

RSSI, AM Rejection, THD, Noise, Audio Output Level

The next set of data shows RSSI performance at 3V, 4V, and 5V (Figure 13) and AM rejection, THD, Noise, and Audio output level (Figure 14).

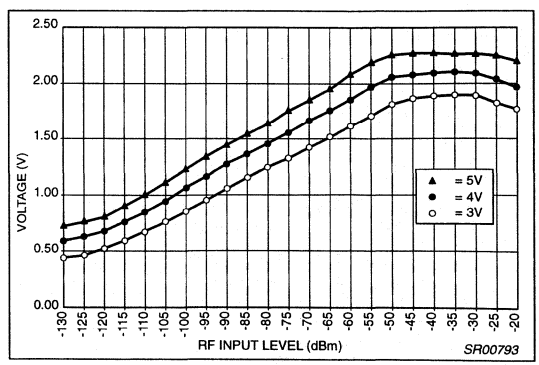


Figure 13. RSSI (Average of Three Boards)

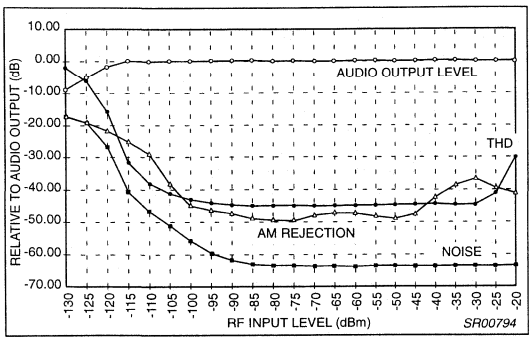


Figure 14. Receiver Performance (Average of Three Boards)

IV. CONCLUSION

The SA601/SA606 application demoboard demonstrates how well the two chips perform together. Meeting the stated AMPS cellular specifications is a good test of a receiver's performance. Not all receivers can meet these stringent requirements. The SA601/SA606 demoboard not only meets, but exceeds, the criteria of sensitivity with 12dB SINAD of about -122dBm, which is 3dB better than AMPS specification, assuming 3dB loss from the duplexer. Adjacent channel exceeds the requirement by 33dB, Alternate channel exceeds the requirement by 7.5dB, Intermodulation Spurious Response exceeds the requirement by 4.5dB, and Protection Against Spurious Response Interference exceeds the requirement by 11dB.

Many key factors such as board layout and impedance matching help the performance exceed the receiver specifications for AMPS. Many issues looked at in this application note will help answer customers' questions as Philips customers design greater and better things.

Questions and Answers

Q. What is the difference between the 50 Ω demoboard and the high-impedance demoboard?

A. Visually, the 50 Ω boards have more components near the 83.161MHz SAW filter. The 50 Ω boards have two 5-30pF trim capacitors. The high-impedance board out performs the 50 Ω board by 1dB on sensitivity. Keep in mind that the 50 Ω board allows troubleshooting of each block.

Q. What do I do if I don't achieve the sensitivity as the data shows?

A. Here is a check list you can follow:

1. Check the solder connections.
2. Make sure the LO drive level is -5dBm to -7dBm to the SA601 mixer.
3. Check for the 700MHz high pass filter (see Figure 10).
4. Check the C-Message filter. (An active C-Message filter with 10dB of gain was used for sensitivity tests.)
5. Probe for signals from the SA601 inputs down to the SA606 limiter-out. Check to see if there are significant losses. The probe points are:
   a. RF input of the SA601
   b. LO input of the SA601
   c. LNA-out of the SA601
   d. Before the 881MHz SAW filter
   e. After the 881MHz SAW filter
   f. Mixer-in of the SA601
   g. Mixer-out of the SA601
   h. Before the 83.161MHz SAW filter
   i. After the 83.161MHz SAW filter
   j. RF input of the SA606
   k. The 82.705MHz crystal
   l. Mixer-out of the SA606
   m. IF-in of the SA606
   n. IF-out of the SA606
   o. Limiter-in of the SA606
   p. Limiter-out of the SA606

Q. What is the difference between the 1008HS and the 1008CS inductors from Coilcraft?

A. There is no difference in performance between the two types of inductors. The only external difference is the packaging.

Q. What should I do if I don't meet the specification for Protection Against Spurious-Response?

A. Make sure that all the grounds of the 83.161MHz SAW filter are connected, especially the grounds closest to the input and output. Shield each section which will isolate each block and improve performance.

Q. Why do you use an IF of 83.16MHz instead of 45MHz?

A. 83.16MHz is used as the IF because, at 45MHz, serious problems may result because of the existence of spurious performance degradation and potential interference due to the half-IF mixer spurious content. The half-IF (RF + 22.5MHz) is only a problem with IF frequencies which are less than twice the receiver bandwidth. An AMPS receiver with 45MHz 1st IF can have a half-IF problem, while at 83.16MHz it will not because the half-IF, at 45MHz for example, will be 891.50MHz (869MHz + 22.5MHz). Since 891.5MHz falls in the pass band, this signal will desensitize the receiver. Also, at 83.16MHz, the image frequency is further away than 45MHz. (See Reference 8)

Q. Will phase noise of the signal generator cause performance degradation when testing Tx desensitization?

A. Yes it will because, when doing the Tx desensitization test without a duplexer, sensitivity dramatically improved as levels on the signal generator were decremented. Also, when cascading two duplexers together, the noise was attenuated and sensitivity improved.
In most handsets, a bandpass filter (center frequency at 836MHz) is placed before the power amplifier; therefore, the out-of-band noise is attenuated before being amplified. This attenuation will lower the phase noise and allow less Tx desensitization.

Q. What spurs will effect the sensitivity of the receiver? How can these spurs be rejected?

A. Consult table below for unwanted spurs:

Spurs	EQ.[1]	Range (MHz)	Rejected by...
1st Image	RF+2(IF1)	1035.32–1060.32	Duplexer
2nd Image	RF+2(IF2)	869.91–894.91	83.16MHz SAW
Half IF	RF+.5(IF1)	910.58–935.58	Duplexer
Tx Intermod[2]	Tx–45MHz	779–804	Duplexer
Tx Isolation[2]	Tx + IF1	907.16–932.16	Duplexer

NOTES:
1. IF1 = 83.16MHz; IF2 = 455kHz
2. Not measured

V. REFERENCES

1. "AN1777: Low Voltage Front-End Circuits", RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
2. "AN1993: High sensitivity application of low-power RF/IF Integrated circuits", RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
3. "AN1994: Reviewing key areas when designing with the SA605", RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
4. "AN1995: Evaluating the SA605 SO and SSOP demoboard, RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
5. "AN1996: Demodulation at 10.7MHz IF with SA605/625", RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
6. "Low-voltage LNA and mixer - 1GHz", (SA601 data sheet), RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
7. "Low-voltage high performance mixer FM IF system", (SA606 data sheet), RF/Wireless Communications, Data Handbook, Philips Semiconductors, 1995.
8. Victor, Alan, "Saw Filters Aid Communications System Performance", Microwaves and RF, Aug. 1991, pg. 104-111.
9. "Recommended Minimum Standards for 800-MHz Cellular Subscriber Units", EIA/IS-19-B. Electronic Industries Association, 1988.

Table 4. RF Sensitivity, Adjacent and Alternate Channel Rejection, and Intermodulation Spurious Response Rejection at V_{CC} = 3V

All data taken without a duplexer.

Frequency	12 dB SINAD	Adjacent Channel Above (+30kHz)	Adjacent Channel Below (-30kHz)	Alternate Channel Above (+60kHz)	Alternate Channel Below (-60kHz)	Intermodulation Spurious Response (+60 & +120 kHz)	Intermodulation Spurious Response (-60 & -120 kHz)
High Impedance Board #1: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	55 dB	53 dB	86 dB	88 dB	71.5 dB	70.5 dB
RF = 869MHz; LO = 952.161MHz	-122 dBm	49 dB	50 dB	88 dB	87 dB	70.5 dB	70.5 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	51 dB	54 dB	88 dB	87 dB	71.5 dB	70 dB
High Impedance Board #2: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122.5 dBm	51.5 dB	52.5 dB	71.5 dB	77.5 dB	71 dB	71 dB
RF = 869MHz; LO = 952.161MHz	-123 dBm	52 dB	51 dB	72 dB	82 dB	70.5 dB	70.5 dB
RF = 894MHz; LO = 977.161MHz	-122.5 dBm	51.5 dB	50.5 dB	72.5 dB	77.5 dB	69.5 dB	69.5 dB
High Impedance Board #3: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	49 dB	54 dB	91 dB	87 dB	73 dB	71 dB
RF = 869MHz; LO = 952.161MHz	-123 dBm	50 dB	56 dB	93 dB	88 dB	73 dB	71 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	50 dB	55 dB	92 dB	89 dB	72 dB	71 dB

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better
2.3.2 Adjacent and Alternate Channel Desensitization: 16dBm min for adjacent channel; 60dB min for alternate channel.
2.3.3 Intermodulation Spurious Response Interference: 65dB min.

Table 5. RF Sensitivity, Adjacent and Alternate Channel Rejection, and Intermodulation Spurious Response Rejection at V_{CC} = 4V

All data taken without a duplexer.

Frequency	12 dB SINAD	Adjacent Channel Above (+30kHz)	Adjacent Channel Below (-30kHz)	Alternate Channel Above (+60kHz)	Alternate Channel Below (-60kHz)	Intermodulation Spurious Response (+60 & +120 kHz)	Intermodulation Spurious Response (-60 & -120 kHz)
High Impedance Board #1: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	51 dB	52 dB	88 dB	86 dB	71.5 dB	69.5 dB
RF = 869MHz; LO = 952.161MHz	-122 dBm	50 dB	51 dB	88 dB	87 dB	72.5 dB	69.5 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	51 dB	51 dB	87 dB	87 dB	72 dB	70 dB
High Impedance Board #2: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122.5 dBm	51.5 dB	51.5 dB	70.5 dB	67.5 dB	70.5 dB	69.5 dB
RF = 869MHz; LO = 952.161MHz	-122.5 dBm	52.5 dB	50.5 dB	71.5 dB	80.5 dB	69 dB	69 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	52 dB	51 dB	72 dB	76 dB	70 dB	76 dB
High Impedance Board #3: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	50 dB	55 dB	91 dB	87 dB	73 dB	71 dB
RF = 869MHz; LO = 952.161MHz	-123 dBm	50 dB	54 dB	93 dB	88 dB	73 dB	70 dB
RF = 894MHz; LO = 977.161MHz	-123 dBm	50 dB	53 dB	91 dB	87 dB	72 dB	70 dB

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better
2.3.2 Adjacent and Alternate Channel Desensitization: 16dBm min for adjacent channel; 60dB min for alternate channel.
2.3.3 Intermodulation Spurious Response Interference: 65dB min.

Table 6. RF Sensitivity, Adjacent and Alternate Channel Rejection, and Intermodulation Spurious Response Rejection at V_{CC} = 5V.

All data taken without a duplexer.

Frequency	12 dB SINAD	Adjacent Channel Above (+30kHz)	Adjacent Channel Below (-30kHz)	Alternate Channel Above (+60kHz)	Alternate Channel Below (-60kHz)	Intermodulation Spurious Response (+60 & +120 kHz)	Intermodulation Spurious Response (-60 & -120 kHz)
High Impedance Board #1: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	50 dB	52 dB	86 dB	85 dB	71.5 dB	69.5 dB
RF = 869MHz; LO = 952.161MHz	-122 dBm	49 dB	52 dB	87 dB	86 dB	71.5 dB	69 dB
RF = 894MHz; LO = 977.161MHz	-122 dBm	52 dB	51 dB	86 dB	86 dB	72 dB	70 dB
High Impedance Board #2: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-122 dBm	52 dB	50 dB	70 dB	76 dB	70.5 dB	69.5 dB
RF = 869MHz; LO = 952.161MHz	-122.5 dBm	52.5 dB	49.5 dB	70.5 dB	78.5 dB	69 dB	69 dB
RF = 894MHz; LO = 977.161MHz	-121.5 dBm	52.5 dB	50.5 dB	71.5 dB	75.5 dB	70 dB	68 dB
High Impedance Board #3: Adjacent and Alternate channel; FM dev = ±8kHz, FM mod = 400Hz							
RF = 881MHz; LO = 964.161MHz	-121.5 dBm	49.5 dB	53.5 dB	90.5 dB	86.5 dB	73 dB	70 dB
RF = 869MHz; LO = 952.161MHz	-122.5 dBm	52.5 dB	49.5 dB	87.5 dB	91.5 dB	73 dB	70 dB
RF = 894MHz; LO = 977.161MHz	-121 dBm	50 dB	53 dB	91 dB	87 dB	72 dB	70 dB

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better
2.3.2 Adjacent and Alternate Channel Desensitization: 16dBm min for adjacent channel; 60dB min for alternate channel.
2.3.3 Intermodulation Spurious Response Interference: 65dB min.

Table 7. Protection Against Spurious Response Interference V_{CC} = 3V

All test measured with TDK duplexer (Model CF6121613D)

Frequency	Interfering Frequency (MHz)	Board #1	Board #2	Board #3
RF = 881MHz; LO = 964.161MHz		**-121 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**
	881.91	82.5 dB	76.5 dB	78.5 dB
	922.58	108.5 dB	108.5 dB	108.5 dB
	1005.74	108.5 dB	108.5 dB	108.5 dB
	1047.32	99.5 dB	97.5 dB	92.5 dB
RF = 869MHz; LO = 952.161MHz		**-119.5 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	869.91	81 dB	73.5 dB	75.5 dB
	910.58	108 dB	108.5 dB	107.5 dB
	993.74	108 dB	108.5 dB	107.5 dB
	1035.32	98 dB	95.5 dB	88.5 dB
RF = 894MHz; LO = 977.161MHz		**-119 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**	**-119.5 dBm for 12 dB SINAD**
	894.91	79.5 dB	82.5 dB	79 dB
	935.58	108.5 dB	110.5 dB	108 dB
	1018.74	108.5 dB	110.5 dB	108 dB
	1060.32	99.5 dB	100.5 dB	96 dB

Requirements per IS-19-B:

2.3.4 Protection Against Spurious Response Interference: 60dB min.

Table 8. Protection Against Spurious Response Interference V_{CC} = 4V

All test measured with TDK duplexer (Model CF6121613D)

Frequency	Interfering Frequency (MHz)	Board #1	Board #2	Board #3
RF = 881MHz; LO = 964.161MHz		**-121 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**	**-121.5 dBm for 12 dB SINAD**
	881.91	84.5 dB	74.5 dB	79 dB
	922.58	108.5 dB	108.5 dB	109 dB
	1005.74	108.5 dB	108.5 dB	109 dB
	1047.32	101.5 dB	98.5 dB	93 dB
RF = 869MHz; LO = 952.161MHz		**-120 dBm for 12 dB SINAD**	**-120.5 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	869.91	80.5 dB	71 dB	73.5 dB
	910.58	107.5 dB	108 dB	107.5 dB
	993.74	107.5 dB	108 dB	107.5 dB
	1035.32	95.5 dB	93 dB	88.5 dB
RF = 894MHz; LO = 977.161MHz		**-119.5 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	894.91	80 dB	78.5 dB	81.5 dB
	935.58	108 dB	108.5 dB	107.5 dB
	1018.74	108 dB	108.5 dB	107.5 dB
	1060.32	100 dB	99.5 dB	95.5 dB

Requirements per IS-19-B:

2.3.4 Protection Against Spurious Response Interference: 60dB min.

Table 9. Protection Against Spurious Response Interference V_{CC} = 5V

All test measured with TDK duplexer (Model CF6121613D)

Frequency	Interfering Frequency (MHz)	Board #1	Board #2	Board #3
RF = 881MHz; LO = 964.161MHz		**-121 dBm for 12 dB SINAD**	**-121 dBm for 12 dB SINAD**	**-121.5 dBm for 12 dB SINAD**
	881.91	84.5 dB	74 dB	77.5 dB
	922.58	108.5 dB	109 dB	108.5 dB
	1005.74	108.5 dB	109 dB	108.5 dB
	1047.32	108.5 dB	97 dB	104.5 dB
RF = 869MHz; LO = 952.161MHz		**-120 dBm for 12 dB SINAD**	**-120.5 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	869.91	79.5 dB	71 dB	71 dB
	910.58	107.5 dB	108 dB	108 dB
	993.74	107.5 dB	108 dB	108 dB
	1035.32	101.5 dB	94 dB	93 dB
RF = 894MHz; LO = 977.161MHz		**-119.5 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**	**-120 dBm for 12 dB SINAD**
	894.91	80.5 dB	77 dB	81.5 dB
	935.58	107.5 dB	108 dB	111.5 dB
	1018.74	107.5 dB	108 dB	111.5 dB
	1060.32	106.5 dB	100 dB	106.5 dB

Requirements per IS-19-B:

2.3.4 Protection Against Spurious Response Interference: 60dB min.

Table 10. Transmit desensitization – Board #1

Frequency	Transmit Power (mW)	12 dB SINAD without Tx (dBm)	12 dB SINAD with Tx (dBm)	Tx desensitization (dB)
RF = 881MHz; LO = 964.161MHz, Tx = 836MHz				
	100	-120	-119.5	0.5
	200	-120	-119.5	0.5
	300	-120	-119	1
	400	-120	-119	1
	500	-120	-119	1
	600	-120	-119	1
	700	-120	-119	1
	800	-120	-118	2
	900	-120	-118	2
	1000	-120	-118	2
RF = 869MHz; LO = 952.161MHz, Tx = 824MHz				
	100	-119.5	-119.5	0
	200	-119.5	-119.5	0
	300	-119.5	-119.5	0
	400	-119.5	-119.5	0
	500	-119.5	-119.5	0
	600	-119.5	-119.5	0
	700	-119.5	-119.5	0
	800	-119.5	-119.5	0
	900	-119.5	-119.5	0
	1000	-119.5	-119.5	0
RF = 894MHz; LO = 977.161MHz, Tx = 849MHz				
	100	-119	-119	0
	200	-119	-119	0
	300	-119	-119	0
	400	-119	-119	0
	500	-119	-119	0
	600	-119	-119	0
	700	-119	-119	0
	800	-119	-119	0
	900	-119	-119	0
	1000	-119	-119	0

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better

Table 11. Transmit desensitization – Board #2

Frequency	Transmit Power (mW)	12 dB SINAD without Tx (dBm)	12 dB SINAD with Tx (dBm)	Tx desensitization (dB)
RF = 881MHz; LO = 964.161MHz, Tx = 836MHz				
	100	-120	-119.5	0.5
	200	-120	-119.5	0.5
	300	-120	-119	1
	400	-120	-119	1
	500	-120	-119	1
	600	-120	-119	1
	700	-120	-119	1
	800	-120	-118	2
	900	-120	-118	2
	1000	-120	-118	2
RF = 869MHz; LO = 952.161MHz, Tx = 824MHz				
	100	-119.5	-119.5	0
	200	-119.5	-119.5	0
	300	-119.5	-119.5	0
	400	-119.5	-119.5	0
	500	-119.5	-119.5	0
	600	-119.5	-119.5	0
	700	-119.5	-119.5	0
	800	-119.5	-119.5	0
	900	-119.5	-119.5	0
	1000	-119.5	-119.5	0
RF = 894MHz; LO = 977.161MHz, Tx = 849MHz				
	100	-119.5	-119.5	0
	200	-119.5	-119.5	0
	300	-119.5	-119.5	0
	400	-119.5	-119.5	0
	500	-119.5	-119.5	0
	600	-119.5	-119	0.5
	700	-119.5	-119	0.5
	800	-119.5	-119	0.5
	900	-119.5	-119	0.5
	1000	-119.5	-119	0.5

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better

Table 12. Transmit desensitization – Board #3

Frequency	Transmit Power (mW)	12 dB SINAD without Tx (dBm)	12 dB SINAD with Tx (dBm)	Tx desensitization (dB)
RF = 881MHz; LO = 964.161MHz, Tx = 836MHz				
	100	-119.8	-119.3	0.5
	200	-119.8	-119.3	0.5
	300	-119.8	-118.8	1
	400	-119.8	-118.8	1
	500	-119.8	-118.8	1
	600	-119.8	-118.8	1
	700	-119.8	-118.8	1
	800	-119.8	-117.8	2
	900	-119.8	-117.8	2
	1000	-119.8	-117.8	2
RF = 869MHz; LO = 952.161MHz, Tx = 824MHz				
	100	-119	-117	0
	200	-119	-117	0
	300	-119	-117	0
	400	-119	-117	0
	500	-119	-117	0
	600	-119	-117	0
	700	-119	-117	0
	800	-119	-117	0
	900	-119	-117	0
	1000	-119	-117	0
RF = 894MHz; LO = 977.161MHz, Tx = 849MHz				
	100	-119	-119	0
	200	-119	-119	0
	300	-119	-119	0
	400	-119	-119	0
	500	-119	-119	0
	600	-119	-118.5	0.5
	700	-119	-118.5	0.5
	800	-119	-118.5	0.5
	900	-119	-118.5	0.5
	1000	-119	-118.5	0.5

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better

Table 13. Transmit desensitization Without Duplexer

Tx Level (dBm)	Board #1			Board #2			Board #3		
	12dB SINAD (dBm)			12dB SINAD (dBm)			12dB SINAD (dBm)		
	824MHz	836MHz	849MHz	824MHz	836MHz	849MHz	824MHz	836MHz	849MHz
-10	-118.5	-117.5	-117	-119	-118.5	-117.5	-119	-118.5	-117.5
-11	-118.5	-118	-117	-119	-118.5	-117.5	-119	-118.5	-117.5
-12	-118.5	-118	-117	-119.5	-118.5	-118	-119.5	-119	-117.5
-13	-119	-118.5	-117.5	-119.5	-119	-118	-119.5	-119	-118
-14	-120	-119.5	-119	-120.5	-120	-119.5	-121	-120.5	-119
-15	-120	-120	-119	-121	-120.5	-119.5	-121	-120.5	-119.5
-16	-120.5	-120	-119.5	-121	-120.5	-120	-121	-121	-120
-17	-120.5	-120	-119.5	-121	-121	-120.5	-121	-121	-120
-18	-120.5	-120.5	-120	-121	-121	-120.5	-121.5	-121	-120.5
-19	-121	-121	-120.5	-122	-121.5	-121.5	-122	-122	-121
-20	-121.5	-121	-121	-122	-122	-121.5	-122	-122	-121.5
-21	-121.5	-121	-121	-122	-122	-121.5	-122.5	-122	-121.5
-22	-121.5	-121.5	-121	-122	-122	-122	-122.5	-122.5	-121.5
-23	-121.5	-121.5	-121.5	-122.5	-122	-122	-122.5	-122.5	-121.5
-24	-122	-122	-121.5	-122.5	-122.5	-122	-122.5	-122.5	-121.5
-25	-122	-122	-121.5	-122.5	-122.5	-122.5	-123	-123	-121.5
-26	-122	-122	-121.5	-122.5	-122.5	-122.5	-123	-123	-122
-27	-122	-122	-122	-123	-122.5	-122.5	-123	-123	-122
-28	-122	-122	-122	-123	-122.5	-122.5	-123	-123	-122
-29	-122.5	-122	-122	-123	-123	-122.5	-123	-123	-122.5
-30	-122.5	-122	-122	-123	-123	-122.5	-123	-123	-122.5
OFF	-122.5	-122	-122	-123	-123	-122.5	-123	-123	-122.5

Requirements per IS-19-B:

2.3.1 RF Sensitivity: -116dBm or better

Table 14. Customer Application Component List for SA601/SA606

Qty.	Part Value	Part Reference	Part Description	Vendor	Mfg	Part Number
****** Surface Mount Capacitors ******						
1	2.2pF	C13	NPO Ceramic 0805 ±.25pF	Garrett	Philips	0805CG229C9BB0
1	2.7pF	C2	NPO Ceramic 0805 ±.25pF	Garrett	Philips	0805CG279C9BB0
1	2.7pF	C18 for Hi Z board	NPO Ceramic 1206 ±.25pF	Garrett	Rohm	1206MCH315A2R7CK
1	3.3pF	C16	NPO Ceramic 0805 ±.25pF	Garrett	Philips	0805CG339C9BB0
1	4.7pF	C10	NPO Ceramic 0805 ±.25pF	Garrett	Philips	0805CG479C9BB0
2	8.2pF	C7, C17	NPO Ceramic 0805 ±5pF	Garrett	Philips	0805CG829C9BB0
2	10pF	C23, C31	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG100J9BB0
1	18pF	C6	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG180J9BB0
1	24pF	C6 for Hi Z board	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG240J9BB0
1	33pF	C8	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG330J9BB0
1	39pF	C19	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG390J9BB0
6	100pF	C1, C4, C5, C11, C12, C14	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG101J9BB0
1	390pF	C29	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG391J9BB0
2	1nF	C22, (C7 for Hi Z board)	NPO Ceramic 0805 ±5%	Garrett	Philips	0805CG102J9BB0
10	100nF	C9, C15, C20, C25, C30, C32, C33, C34, C35, C36	Z5U Ceramic 0805 ±20%	Garrett	Philips	08052E104M9BB0
1	1µF	C3	Tant Chip Cap ±10%	Garrett	Philips	49MC105A016KOAS
2	2.2µF	C26, C27	Tant Chip Cap ±10%	Garrett	Philips	49MC225A010KOAS
1	10µF	C24	Tant Chip Cap ±10%	Garrett	KOA Speer	TMC-M1AB106KLRH
2	5-30pF	C18, C21	SMT Trimmer Cap	Jaco	Kyocera	CTZ3S-30C-B
****** Resistors ******						
1	0Ω	R5	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F000
1	100Ω	R1	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F101
1	2.2kΩ	R2	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F222
1	2.4kΩ	R8	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F242
1	3.3kΩ	R9	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F332
1	8.2kΩ	R4	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F822
1	10kΩ	R3	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F103
1	11kΩ	R7	Res. chip 0805 1/10W ±5%	Garrett	KOA Speer	RM73B2A-F113
****** Inductors ******						
1	56nH	L1	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-560 ±10%
1	270nH	L3	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-271 ±10%
2	330nH	L5, L6	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-331 ±10%
1	470nH	L2	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-471 ±10%
1	560nH	L4	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-561 ±10%
1	750nH	L6 Hi Z board	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-751 ±10%
1	1.2µH	L7	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-122 ±10%
1	330µH	L9	Variable SMT Inductor	Digikey	Toko	TKS2272CT-ND ±3%
1	1µH	L8	Chip Inductor ±10%	Coilcraft	Coilcraft	1008CS-102 ±10%
****** Filters ******						
1	881.5MHz	FILT1	881.5MHz SAW Bandpass	Murata	Murata	SAFC881.5MA70N-TC
1	83.161MHz	FILT2	83.161MHz SAW Bandpass	Murata	Murata	SAFC83.161MA51X-TC
2	455kHz	FILT3, FILT4	455kHz FM IF Filter	Murata	Murata	SFGCG455BX-TC
****** IC ******						
1	SA601	U1	Low Voltage LNA & Mixer	Philips	Philips	SA601DK
1	SA606	U2	Low Voltage FM IF System	Philips	Philips	SA606DK
****** Miscellaneous ******						
1	82.705MHz	X1	82.705MHz crystal	Hy-Q International or Reeves–Hoffman 82.705MHz		
2			SMA Gold Connector	Digikey J502-ND		EF Johnson 142-0701-801
1			5 Pins Gold Test point	Digikey		3M929647-01-36-ND
1			Printed circuit board	RF# 30042		Excel 601/606 #30042

Using the SA5752 and SA5753 for low voltage designs AN1742

Author: Alvin K. Wong

INTRODUCTION

The SA5752 and the SA5753 are two audio processor chips that can be used in designs that require 3 volt operation. This chip set, known as the APROC II (SA5752 and SA5753), is functionally similar to the APROC I (SA5750 and SA5751), but with a number of enhancements which allow more design flexibility for the designer. Additionally, the APROC II offers the same high performance as the APROC I. The SA5752 is the low voltage version of the SA5750, and the SA5753 is the low voltage version of the SA5751. Figures 1 and 2 show the block diagrams of the APROC II and APROC I, respectively. Notice that the differences are subtle and pertain primarily to the amplifier section.

If a designer is not familiar with the APROC I chip set, he/she can refer to AN1741 which discusses the basics of audio processing and the key functions used to meet the strict requirements for cellular specifications. Additionally, it describes how to design with the chip set and how to measure attack and release times for the compandor section.

This application note should be used in conjunction with AN1741 to fully understand audio processing. Experience with the APROC I will help aid the designer in learning the APROC II, but this is not a necessity. This application note will focus on the main differences between the APROCs and highlight key areas of the APROC II.

I. KEY DIFFERENCES BETWEEN APROC I AND APROC II

- Comparing the SA5750 and SA5752
  - Packaging
  - External Amplifier
  - Power Consumption
- Comparing the SA5751 and SA5753
  - Packaging
  - Power Consumption
  - Programmable Gain Attenuators
  - Power Down
  - Programmable Transmit and Receive Mute Polarity Function
  - Non-I²C Operation (Default Mode)
  - Cordless Application
  - VCO Mode
  - NAMPS Mode

II. SA5752

- Preamp
- VOX
- Noise Canceller
- Compressor
- Power Down

III. SA5753

- Non-I²C Operation (Default Mode)
- Programming Without the I²C Protocol
- DTMF
- The Limiter and All-Pass Circuit

IV. EVALUATION SOFTWARE AND DEMOBOARD

- DTMF

V. QUESTIONS AND ANSWERS

I. KEY DIFFERENCES BETWEEN APROC I AND APROC II

Table 2 shows the main differences between the APROC I and II. One noticeable difference is the power consumption and power down currents. Moreover, the SA5753 has three power down modes which will be discussed in detail in the Power Down Mode section of this application note.

Comparing the SA5750 and SA5752

The SA5750 and SA5752 differ in the following ways:

Packaging

There are minimal differences between the SA5750 and the SA5752. Instead of a 24 pin package, the SA5752 is offered in a 20 pin package. This change allows the SA5752 to come in the SSOP package. The SSOP package is smaller in dimension than the standard SO package which saves space.

External Amplifiers

Since many APROC I customers use their own external speaker and ear amplifiers, the SA5752 was designed without them (see Figures 1 and 2). However, the other key blocks are present, like the preamp, VOX, compressor, expandor, and noise canceller circuit.

Since the SA5752 does not supply the ear and speaker amplifiers internally, an external one can be used. The Philips TDA7050T is the recommended choice because of its low voltage operation and high performance capabilities.

Power Consumption

The current consumption and power down mode has been improved in the SA5752. For normal operation, the SA5752 only draws an I_{CC} of 3.1mA for a 3 volt supply compared to the SA5750, where I_{CC} = 8.4mA for V_{CC} = 5V. Additionally, in the power down mode, the SA5752 only draws 0.2mA of current, compared to 1.8mA for the SA5750. Recall that the power down mode is implemented when the chip is not being used to conserve battery life. The power down feature is preferred instead of completely turning off the power to the chip because the turn on time to normal operation is faster.

Comparing the SA5751 and SA5753

The SA5751 and SA5753 differ in the following ways:

Packaging

The SA5751 is available in a 24 pin DIP package or a 28 pin SO package.

Similar to the SA5752, the SA5753 is also offered in the 20 pin SSOP package. The combination of these packages allows all the audio processing functions to be done in a minimal amount of board space.

Power Consumption

The current and voltage specification has also improved for the SA5753. This chip draws 2.1mA at 3V compared to 2.7mA at 5V for the SA5751. There is also additional current economy from the three different power-down modes, PWDN, DENA and IDLE (see Power-Down section). These power-down currents are 0.2mA, 0.6mA and 0.7mA compared to 0.9 for the SA5751.

Programmable gain attenuators

The SA5753 has the same key block functions as the SA5751, but there are additional features. The SA5753 has nine programmable gain attenuators throughout the transmit and receive path. This allows the designer the flexibility to tailor the signal level at different ports. The SA5751 has only one programmable gain attenuator in the receive path which can be used as the volume control. Table 3 shows the programmable gain attenuators' range for the SA5753.

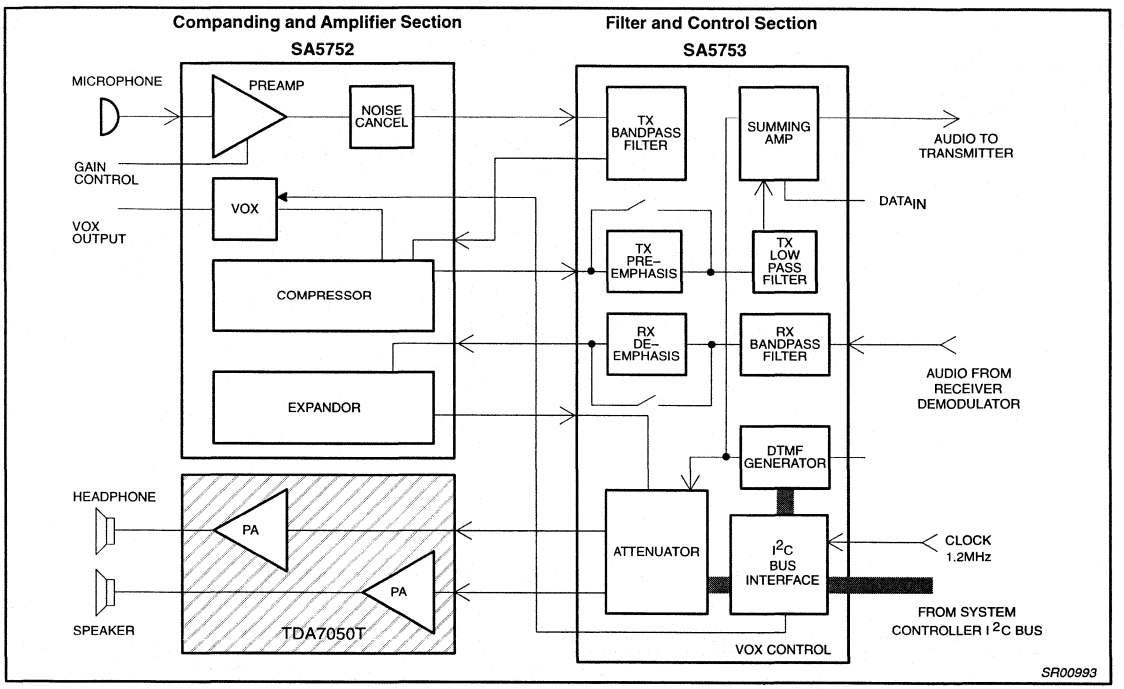


Figure 1. Block Diagram of Audio Processor (APROC II) System Chip Set

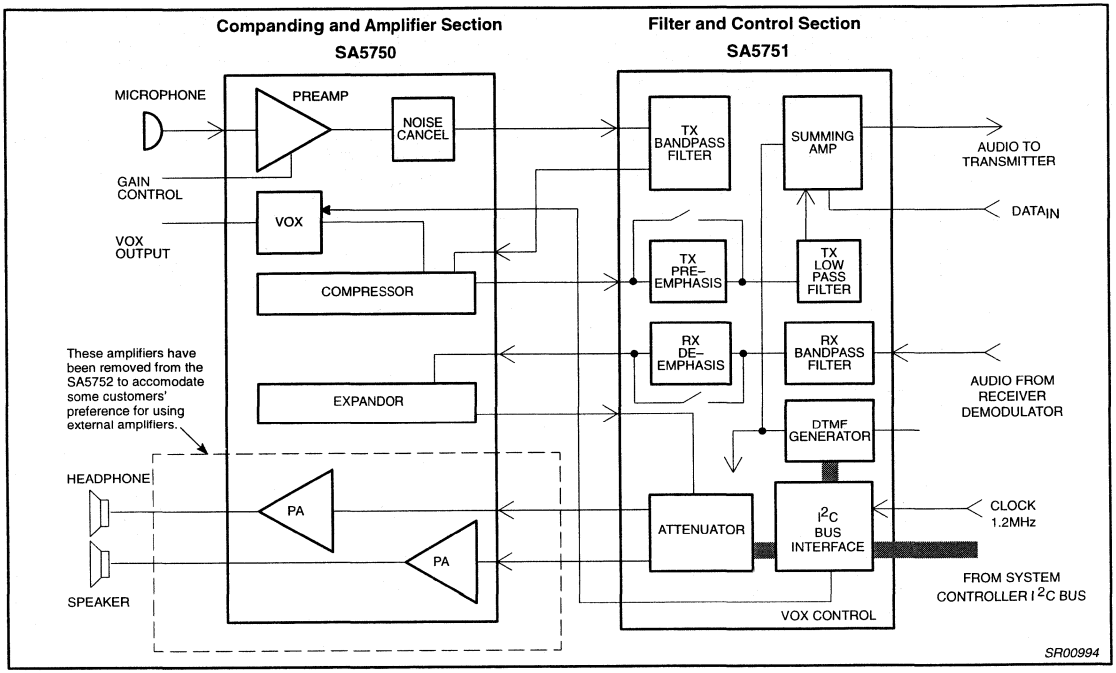


Figure 2. Block Diagram of Audio Processor (APROC I) System Chip Set

Table 2. Key Differences Between APROC I and APROC II (All values are Typical)

	APROC I		APROC II	
	SA5750	**SA5751**	**SA5752**	**SA5753**
V_{CC} (V)	4.5 – 5.5	4.5 – 5.5	2.7 – 5.5	2.7 – 5.5
I_{CC} (mA)	8.4 @ 5V	2.7 @ 5V	3.1 @ 3V	2.1 @ 3V
Total I_{CC} (mA)	11.10		5.4	
Power Down Modes	PWDN		PWDN, IDLE and DENA	
Power Down I_{CC} (mA)	1.8	0.9	0.2	PWDN 0.2 IDLE 0.6 DENA 0.7
Packages:				
NE: 0 to +70°C	SA5750N SA5750D	SA5751N SA5751D		
SA: –40 to +85°C	SA5750N SA5750D	SA5751N SA5751D	SA5752D SA5752DK	SA5753D SA5753DK
No. of Pins	24	24 or 28	20	20
Programmable Gain Attenuators	0	1	0	9
I^2C Protocol	Not required	Required	Not Required	Optional*

Package Codes:
N: Plastic Dual In-Line Package (DIP)
D: Plastic Small Outline (SO)
FE: Ceramic Dual In-Line Package
DK: Shrink Small Outline Package (SSOP)

*Operating the SA5753 without the I^2C protocol means DTMF generator and gain attenuators are no longer functional. See SA5753 section for more details.

Table 3. Attenuator Gain Blocks (SA5753)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB)	
			MIN	MAX
A1	4	-0.8	–12.0	0
A2a	5	±0.25	–3.75	+3.75
A2b	2	–6, (–12 on first)	–24.0	0
A3	4	–1.0	–17.0	–2
A4	4	±0.5	–3.5	+3.5
A6	4	–2.0	–30	0
A7	4	0.5	–3.5	+3.5
NAMPS	1		+1.9 in A2b –7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

Table 4. Power-Down Modes (SA5753)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I^2C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} disabled.
0	0	0	Normal operation.
0	0	1	$DATA_{IN}$ to TX_{OUT} disabled.
X = don't care			

The benefit of having signal amplitude control throughout the signal path is that a designer will no longer have to add an external amplifier to boost signals. Additionally, external resistors are no longer needed to attenuate the signal. The SA5753 programmable gain attenuators make a design more flexible which saves cost and board space from external components.

Power Down

The SA5753 has three different power down modes compared to only one for the SA5751. The three power down modes are PWDN, IDLE, and DENA (see Table 4). All three power down modes have different current consumptions and provide different options to the designer.

In the PWDN mode, the voice and data channels are powered down. This allows for maximum power conservation. In the IDLE mode, both the voice and data channels are also powered down, but are glitch free when going from power down to power up.

The IDLE mode trades a higher standby current against glitch-free power-up. Hence, the IDLE mode is used for power conservation, whereas PWDN mode is mainly used for absolute maximum power conservation.

For the DENA mode, the voice channels are powered down, but the data channel is still fully active. This allows the chip set to transmit on reverse control channel without powering up the whole APROC II.

In the PWDN mode, the SA5753 transmit path from the Tx bandpass filter in to the Tx filter out pin has only 6dB of attenuation. This means that, if a signal is present and a designer does not want this signal through, he/she should use the IDLE (or DENA) mode.

Programmable Transmit and Receive Mute Polarity Function

The SA5753 also has programmable transmit and receive mute polarity functions (TxP and RxP). A designer can mute the transmit or receive path with a logic '1' or '0' on the TxMute or RxMute pin depending on how the SA5753 is programmed by I^2C.

The benefit of having programmable transmit and receive mute polarity functions is that it eliminates the need for an inverter chip which saves on costs, power, and space. If the microcontroller or data processor (DPROC) can only provide a logic '1' to mute the Tx and Rx signal path, then to mute the chip-set the standard way, an inverter gate is needed because the logic '1' needs to be converted to a logic '0'. This logic '0' is then applied to the TxMute and RxMute pin. But with the SA5753, a logic '1' applied to the TxMute and RxMute pins will mute the Tx and Rx path if the SA5753 is programmed to mute for a logic '1'.

Figure 3 shows a diagram of how the inverter gate chip is eliminated. Additionally, a logic '0' applied to the TxMute or RxMute pin can mute the signal path if the SA5753 is programmed to mute when a logic '0' is applied to the TxMute and RxMute pins. Because of this feature the APROC II can now interface directly with the Philips Semiconductors UMA1000 DPROC.

Since the TxMute and RxMute pins are separate, the Tx and Rx path can also be muted separately. For example, if a user wants to mute his/her side of the conversation (such that the other party cannot hear), but still wants to hear the other party, the Tx path needs to be muted while the Rx path is left on. Therefore, a

designer can provide a mute button on the keypad to provide this function to the user.

Since there are separate pins to mute the Tx and Rx paths, a designer is also given full flexibility in programming these pins separately. He/she can define a logic '1' to have the Tx path mute while programming a logic '0' to have the Rx path mute, or vice versa (see Figure 4). However, in most designs a logic '0' is programmed to have the Tx and Rx path muted.

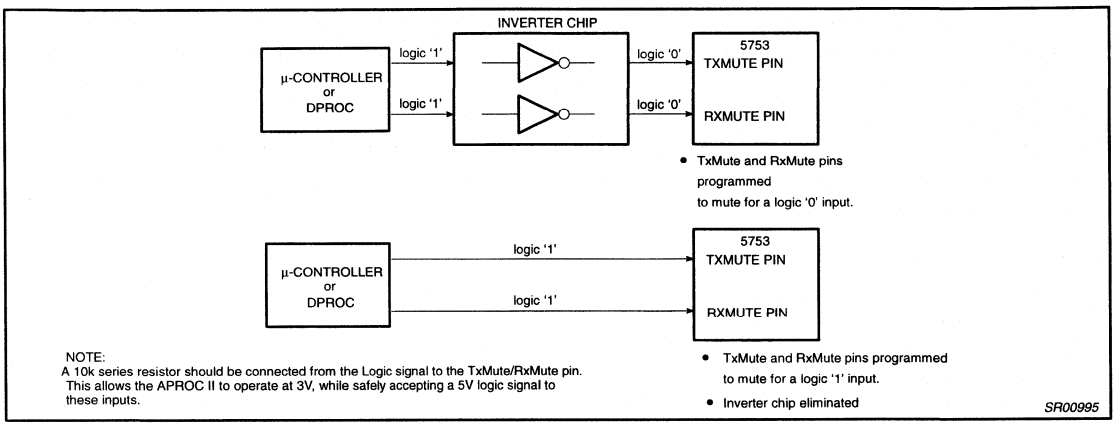


Figure 3. Benefit of Having Programmable Transmit and Receive Mute Pins

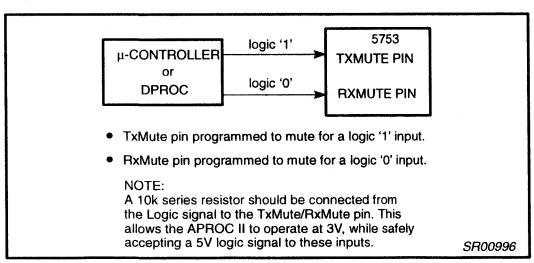


Figure 4. Muting the Tx and Rx Path for Separate Programmable Inputs

Non–I²C Operation (Default Mode)

The SA5753 can also be used without the I²C protocol by pulling the DFT (default pin) and HPDN pin HIGH. This non-I²C operation does not give the designer the flexibility to tailor the signal or use the internal DTMF generator. However, if the SA5753 is loaded serially, the SA5753 can be programmed. More information can be found in any I²C documentation. See the SA5753 section for more detailed information.

Cordless Application

Unlike the SA5751, the SA5753 can be implemented more readily for cordless phone applications. The data path can be routed through the transmit path while inhibiting the voice channel. In the receive path, the EAR_{OUT} and $SPKR_{OUT}$ can be disabled when the data is detected at the $DEMP_{OUT}$ pin.

To allow design flexibility, a designer can attenuate the data signal internally before it is passed through the TX_{OUT} pin. This eliminates the need for external components and allows programmable attenuation steps

such that different data amplitude inputs can be tailored in real-time.

VCO Mode

If the VCO bit on the SA5753 is programmed correctly, the TX_{OUT} provides an extra 6dB of gain through Attenuator 4. Therefore, the new range is 2.5dB to 9.5dB. Normally the TX_{OUT} signal is connected to a VCO (Voltage Controlled Oscillator) with a slope of 10kHz/V. The designer can implement the VCO bit to get a stronger output from the SA5753 to match 5kHz/V VCOs.

NAMPS Mode

Another key difference between the SA5753 and the SA5751 is that the SA5753 can be programmed for NAMPS mode by tailoring the gain attenuator settings.

There are two attenuators that receive the modified gain adjustments. Attenuator 4 is reduced by –7.6dB and Attenuator 2B is boosted by 1.9dB. Therefore, the new ranges are –11.1dB to –4.1dB for Attenuator 4 and –22.1dB to 1.9dB for Attenuator 2B.

The reason the gain settings are reduced is because the signal amplitude needs to be reduced before going to the transmitter. Recall that for the NAMPS mode the frequency deviation is less, so less amplitude is required.

II. SA5752

Figure 5 shows the main blocks of the SA5752: preamp, noise canceller, VOX, compressor, and expandor. This part does not require any programming blocks and therefore, no I²C is needed to operate this part. However, the SA5752 can be powered down via the SA5753 HPDN bit, which is under I²C control.

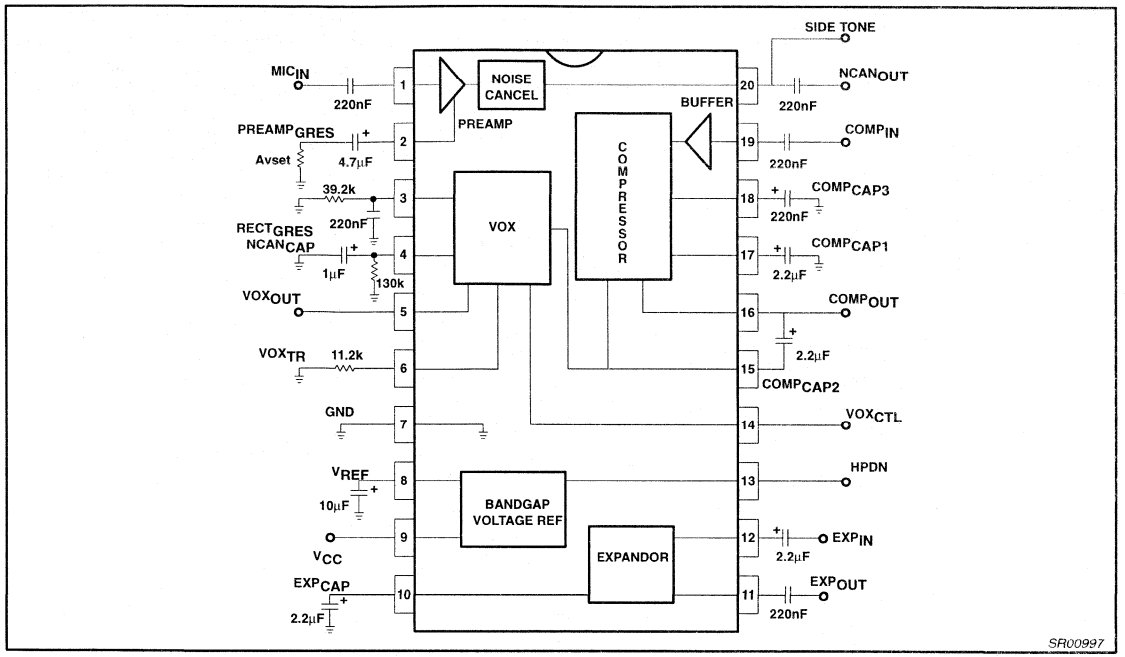


Figure 5. SA5752 Block Diagram

Preamp

The SA5752 provides a preamp which has an adjustable gain range from 0 to 40dB. The gain may be adjusted with an external resistor which connects to Pin 2 (see Equation 1, below). Table 5 shows the resistor values needed to get the appropriate gain. If a designer wants to calculate for a different value, the equation below shows how to do so.

When a designer sets the preamp gain, be sure that the output signal does not clip due to the power supply rails. To prevent this, apply the predicted strongest signal to the preamp input and observe the output while setting the gain.

Additionally, if the VOX is implemented, be sure that the extra 10dB of gain is on from the noise canceller circuit (see VOX section for more details).

$$R1 = \left[\frac{50,000}{10^{\left(\frac{X(dB)}{20}\right)} - 1}\right] - 500 \qquad (1)$$

"X" in dB

where 0 < XdB < 40dB

The preamp input impedance is 50kΩ. The output of the preamp is connected to a noise canceller which can drive a minimum load impedance of 50kΩ.

Table 5. Calculated R1 Values for Different Preamp Gains

X (dB)	R1
0	Leave Pin 2 open (∞)
5	64k
10	22k
15	10k
20	5.1k
25	2.5k
30	1.1k
35	405
40	Pin 2 AC grounded

When measuring the SA5752 preamp gain, be sure to measure the signal from Pin 20 to Pin 1. If the signal is measured from the SA5752 preamp input to the TX_{OUT} of the SA5753, the signal's amplitude will not be the expected value due to the compressor,

pre-emphasis, and attenuator settings. Therefore, remember to measure the preamp gain from the SA5752 preamp out to in.

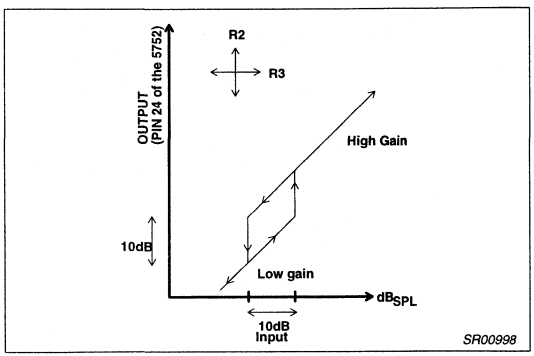


Figure 6. VOX Threshold Points

VOX

The SA5752 VOX circuitry operates like the SA5750 in that it works in conjunction with the noise canceller circuit. With the VOX activated, the noise canceller circuit will provide 10dB of gain when the input signal surpasses the "on" threshold point. When the input signal drops below the "off" threshold point, the noise canceller provides 0dB of gain. Figure 6 illustrates this function.

The VOX circuitry is useful for hands-free operation. This function is normally used in mobile conversation. Because there is road noise present in a moving vehicle, it is desirable to be able to prevent this noise from being heard. If the VOX threshold is set correctly, the noise canceller will provide 10dB of gain when the user speaks and a gain of 0dB when the user stops speaking. The other party will not hear the road noise in the background as loudly. Another feature of the VOX circuitry is that it can be used to save power. The transmitter can be switched off during non-speech periods if voice discontinuous mode (AMP) is enabled.

The VOX_{OUT} and VOX_{CTRL}, Pins 5 and 14 respectively, can be used to determine the status of the noise canceller. Since the VOX_{OUT} pin is an open collector output, a designer should connect a 10k pull up resistor to V_{CC}. This allows the output to read a high or low reading to determine the status of the noise canceller. Table 6 shows how Pins 5 and 14 can be used.

Having a logic '0' on Pin 14 (VOX_{CTRL}) is sufficient in most applications. When the voice is present, the noise canceller kicks on while the VOX_{OUT} pin supplies a logic '1'. When voice is not present, VOX_{OUT} pin supplies a logic '0'.

Supplying a logic '1' on Pin 14 would cause the VOX_{OUT} pin to stay as a logic '1' regardless of any signal input to the preamp

Table 6. VOX Truth Table

Inputs		Outputs	
Voice (Pin 1)	**VOX_{CTRL} (Pin 14 of SA5752)**	**Noise Canceller Gain**	**VOX_{OUT} (Pin 5 of SA5752)**
Not Present	logic '0'	0dB	logic '0'
Present	logic '0'	10dB	logic '1'
Not Present	logic '1'	0dB	logic '1'
Present	logic '1'	10dB	logic '1'

NOTE: If the SA5752 is used alone, be sure that the output of the noise canceller is AC coupled to the input of the compressor. Also, make sure that all of the components for the compressor are connected.

(Pin 1 of SA5752). However, the functionality of the noise canceller will still be signal dependent.

Pins 3, 4, 5, 6, and 14 all deal with the VOX's performance. Resistor R2 and capacitor C3 are connected to Pin 3. These components set the gain of the VOX. The values chosen here are for internal use only and should not be altered.

The following steps are the procedure for setting the VOX threshold. Remember that this setting can be set externally by the user using an external potentiometer or by a microprocessor which can sample the sound in the car and electronically set the "automatic environment VOX function" threshold. This can be done by implementing different resistor settings for different threshold points.

Step 1: Make sure:

a. Pin 6 is left open
b. The VOX attack and recovery components are in place at Pin 4.
c. R2 and C3 are connected to Pin 3.
d. If using the SA5752 alone, be sure to connect the preamp output (Pin 20) to the compressor input (Pin 19) with a DC blocking capacitor.
e. The preamp gain is already set (in this instance the preamp gain is 0dB)
f. Make sure that the compressor's components are also connected; compressor's attack time has to be functional.

Step 2. Apply a constant 1kHz sinewave signal to Pin 1 through a DC blocking cap (if the Philips evaluation board is used, apply the signal to the MIC input pin) with the desired threshold. In this case, $30mV_{P-P}$.

Step 3. Measure the DC voltage on Pin 4: V4=275mV

Step 4. Calculate R5:

$$R5 = \frac{V4(V)}{25\pi A} = \frac{275mV}{25\pi A} = 11k \quad (2)$$

Step 5. Connect R5 to Pin 6 and verify that VOX kicks on at the desired threshold. This set-up has the VOX kicking on at $30mV_{P-P}$ and kicking off at $11mV_{P-P}$ (for better accuracy use a 1% resistor value for R5).

Referring to the above example, if a preamp gain of 10dB was chosen before setting the threshold, the threshold will also change. So it is vital that the preamp gain be set before setting the VOX threshold.

Noise Canceller

The output of the preamp is connected to the input of the noise canceller circuit which is internal to the device. The function of the

noise canceller is to automatically provide a set gain of either 0dB or 10dB when a voice is present or not present. The gain setting can be set by implementing the VOX functions.

Although the noise canceller circuit is really designed to be used with the VOX circuitry, it can be implemented without it. The noise canceller circuit can be set up to provide either 0dB or 10dB of gain at all times, regardless of the presence of a signal. Table 7 shows how to achieve either gain settings when the VOX function is bypassed.

Table 7. Setting Up the Gain of the Noise Canceller

Pin No.	Gain of Noise Canceller	
	0dB	10dB
3	Ground	Ground
4	Ground	V_{CC}
6	10k to GND	Ground

The output of the noise canceller is accessible to the designer at Pin 20.

Compressor

The SA5752 compandor operates with a unity gain level (0dB level) of 77.5mV$_{RMS}$. It operates like the rest of the Philips Compandor family where any signal above the 0dB level in the compressor mode is half in dB, and any signal below the 0dB level is multiplied by 2 (assuming the unit is in dB)

As for the Expandor, the levels above and below the 0dB level are modified by the opposite of what the compressor does. This allows the signal to be restored to its original level with reduction of noise.

To determine the amplitude, the following formula is used.

$$XdB = 20\log\left(\frac{\text{AC level mV}_{RMS}}{77.5\text{mV}_{RMS}}\right) \quad (3)$$

Example:

Determine the compressor's AC voltage output if a 200mV$_{RMS}$ signal is applied to the compressor's input.

1. Convert 200mV$_{RMS}$ to dB as in Equation 3

$$XdB = 20\log\left(\frac{200\text{mV}_{RMS}}{77.5\text{mV}_{RMS}}\right) = 8.23\text{dB}$$

2. Because 8.23dB is above the 0dB level, by definition of the compressor the signal is halved to 4.12dB
3. Now converting back to voltage using Equation 3 the output is 124.5mV$_{RMS}$.

Figure 7 shows the diagram with other numbers for practice.

Power Down

The HPDN (Hardware Power Down) pin on the SA5752 can be left open or connected to V_{CC} for normal operation. For power down, a designer needs to ground this pin.

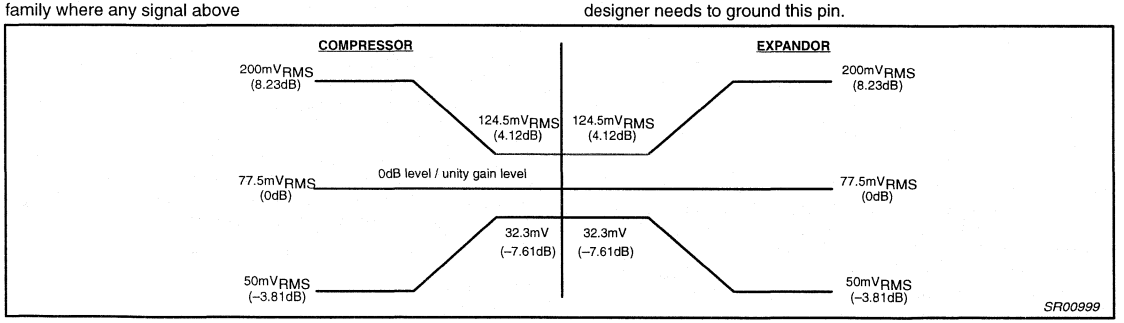


Figure 7. Determining the AC Signal Level Through a Compandor

Table 8. Programmable Divide Ratio Number

Decimal Value	Binary Value	Hi DTMF Frequency	Lo DTMF Frequency
2	0000 0010	OFF	OFF
3	0000 0011	66.66kHz	28.57kHz
4	0000 0100	50kHz	21.43kHz
5	0000 0101	40kHz	17.14kHz
• • •	• • •	• • •	• • •
254	1111 1110	787.40Hz	337.46Hz
555	1111 1111	784.31Hz	336.13Hz
256	0000 0000	781.25Hz	334.82Hz
257	0000 0001	778.21Hz	333.52Hz

III. SA5753

Figure 8 shows the main blocks of the SA5753; the Transmit and Receive Bandpass filters, the Transmit Low Pass Filter, Pre-emphasis and De-emphasis, DTMF generator, attenuators and I^{2}C controls.

Non-I^{2}C Operation (Default Mode)

The SA5753 can be used without the I^{2}C protocol. To implement this feature, the DFT pin (default, Pin 13) and HPDN (Pin 6) must be connected to V_{CC}. In the default mode, a designer has less flexibility in programming the SA5753. The only way to program the SA5753 without the I2C protocol is to load the register serially (see next section).

If a designer decides not to program the SA5753 registers, they can no longer bypass key functions or attenuate/gain the signal. Additionally, they can no longer make use of the DTMF generator.

The TxMute and RxMute pins are also no longer programmable, but are controllable externally.

A designer does not have a choice of programming the mute polarity pins. Muting the transmit and receive path now requires a

designer to supply V_{CC} to the TxMute pin (Pin 18) and RxMute pin (Pin 12). To unmute the paths, a ground connection on these pins is required.

Pin 6 must be grounded for powering down the SA5753 in the default mode. For normal operations without the I²C protocol, Pin 6 must be connected to V_{CC}. Although the SA5753 might be functional with Pin 6 left open, this is not advisable. This pin should either have V_{CC} or ground connected for a defined state. See the SA5753 data sheet for more information on non-I²C operation.

The following is a list of features when the Default Mode is implemented:

1. All previous settings in the registers are ignored except for R8B7 (VOX_{CTL}).
2. VOX_{CTL} = the setting in R8B7 before DFT goes high.
3. All attenuators are set to 0dB.
4. HPDN is now an input, LOW=PWDN Mode.
5. DTMF = OFF
6. DEEMPH = ON
7. PREEMPH = ON
8. AMPS mode
9. Closed = S9, S10, S13
10. Open = S1, S2, S3, S4, S5, S6, S7, S8, S11, S12
11. RX is muted when RXMUTE = HI
12. TX is muted when TXMUTE = HI

NOTE: When the SA5753 is changed from DFT=HIGH (Default Mode) to DFT=LOW, the register settings will have an indeterminate value and all registers will need to be reloaded to avoid undefined states.

Programming Without the I²C Protocol

In the default mode, with DFT (Pin 13) and HPDN (Pin 6) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I²C bus by the negative edge of a shifting clock applied at the SCL pin of the I²C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are, therefore, required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value. Once the registers are loaded, the DFT pin can be pulled low to enable the interface between the control registers and the program functions.

Summary: To use this capability, the DFT pin and the HPDN pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

DTMF

The DTMF generator generates its tones by using the 1.2MHz I²C clock and dividing it down to the desired frequency. There are high and low DTMF tones, so different divide ratios are used. To tailor the exact frequency, a programmable divide ratio number is provided to the designer. Figure 9 shows the basic scheme and the formulas to calculate the desired DTMF frequency.

The programmable divide ratio number ranges from 3 to 257 for both the high and low DTMF functions. This means that the high DTMF frequency range is from 778.21Hz to 66.66kHz. The low DTMF frequency range is from 333.52Hz to 28.57kHz.

The only caution in using the DTMF generator is when the programmable divide ratio decimal number is 256 or 257. For the SA5753, decimal values 256 and 257 are defined as a binary '0' and '1', respectively (see Table 8). The reason the decimal values 256 and 257 were defined this way is because of the actual length of their binary numbers.

Decimal 256 is binary 1 0000 0000 and decimal 257 is binary 1 0000 0001. These binary numbers exceed the 8-bit register, so 256 and 257 were replaced with a decimal '0' and '1' since these values were not previously used.

Other decimal divide ratio numbers can be converted directly to a binary number which is then loaded into the 8-bit register. To turn off the high or low DTMF generator, a decimal 2, converted to a binary 0000 0010, needs to be loaded into the register.

Below are two examples of loading the DTMF generator.

Step 1: Determine what frequency is desired for the High and Low frequencies.

Step 2: Use formulas in Figure 9 to calculate the programmable 'divide ratio number' for both High and Low tones.

Step 3: Convert the calculated 'divide ratio number' to a binary number and load into the proper register. NOTE: If the 'divide ratio number' is 256 or 257, load a binary 0000 0000 or 0000 0001, respectively. To turn off the high or low

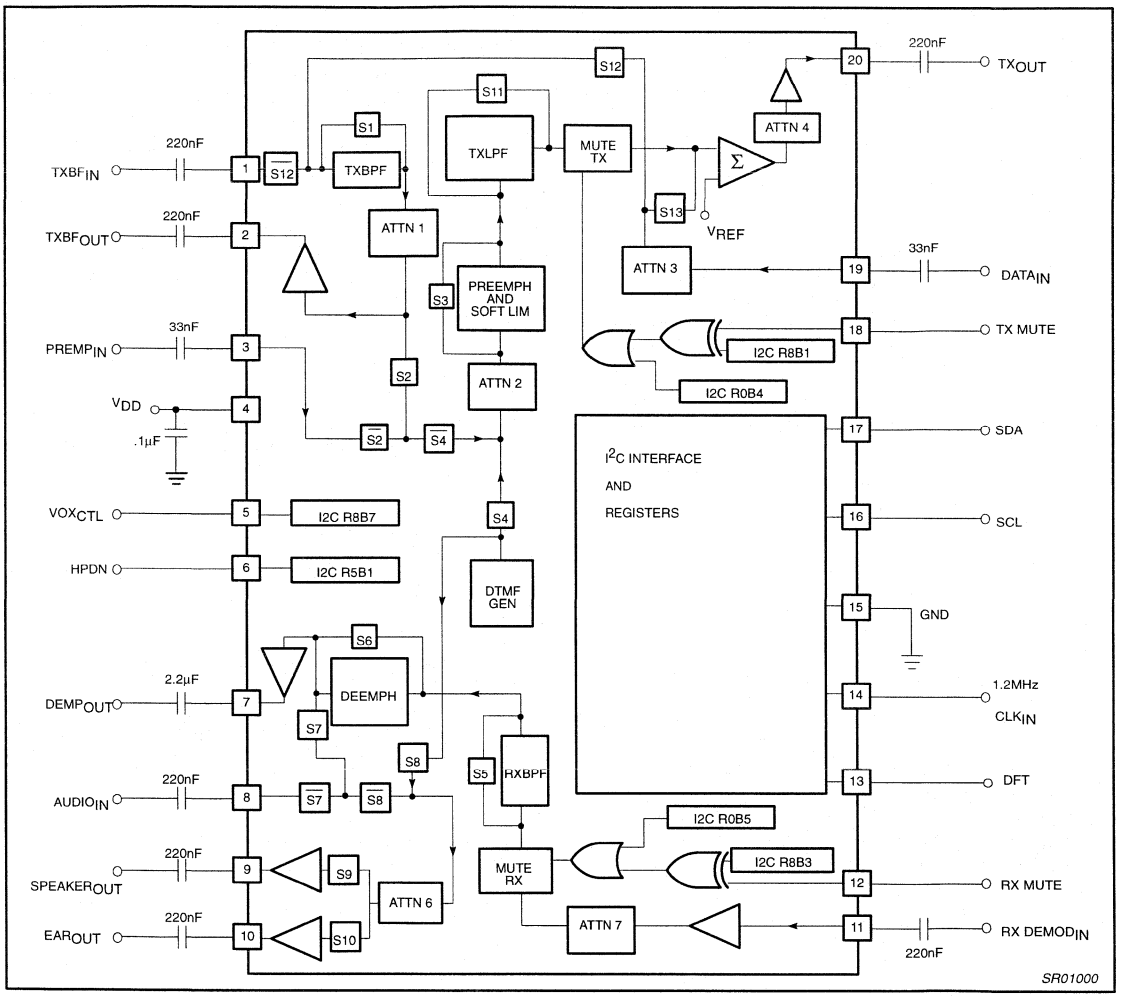


Figure 8. SA/SA5753 Test and Application Circuit

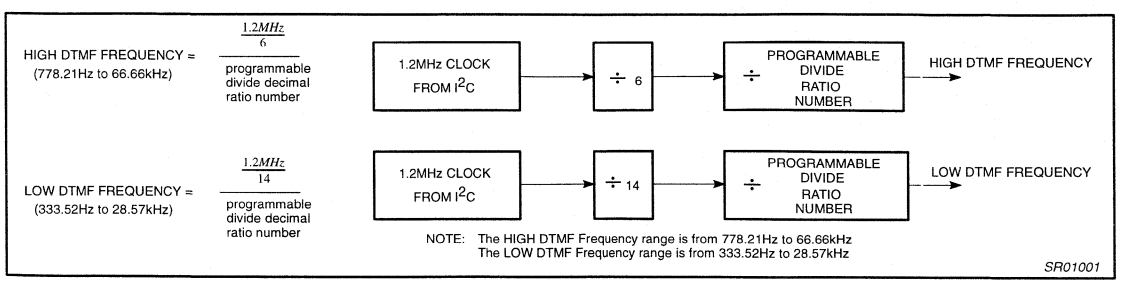


Figure 9. DTMF Formula

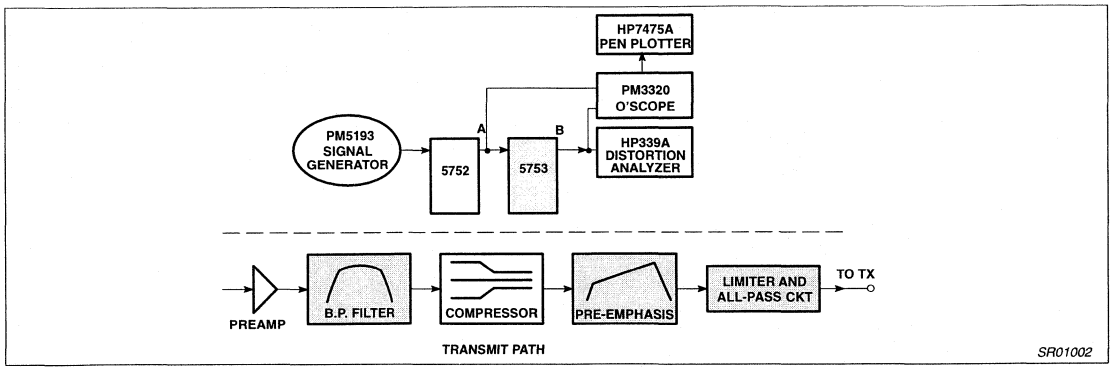


Figure 10. . Test Set-up and Tx Path of Signal

tone DTMF generator, load a binary 2 or 0000 0010 to the register.

Example 1
Program the SA5753 DTMF generator such that High DTMF = 4000Hz and Low DTMF = 3061.22Hz.

1. Using the formula in Figure 9,
   High DTMF 'divide ratio number' = 50
   Low DTMF 'divide ratio number' = 28
2. Convert 'divide ratio number' into a binary number
   High DTMF binary 'divide ratio number' = 0011 0010
   Low DTMF binary 'divide ratio number' = 0001 1100.
3. Load binary numbers into proper registers and observe on a spectrum analyzer.

Example 2
Program the SA5753 DTMF generator such that High DTMF = 778.21Hz and Low DTMF = OFF.

1. Calculate 'divide ratio number' using the formula in Figure 9,
   High DTMF 'divide ratio number' = 257
   Low DTMF 'divide ratio number' = 2, by definition for OFF see Table 8.
2. Converting 'divide ratio numbers'
   High DTMF binary 'divide ratio number' = 0000 0001 (remember the special case that applies here)
   Low DTMF binary 'divide ratio number' = 0000 0010.
3. Load binary numbers into proper registers and observe on a spectrum analyzer.

Programmable Transmit and Receive Mute Polarity Function

If a designer wants to operate the SA5753 at 3V and wants to mute the TxMute and RxMute pins with a 5V logic '1' signal, a series 10k resistor should be used. If the 10k resistor is not used, the SA5753 will draw more current. To eliminate the 10k resistor the designer should make sure that the logic '1' signal never exceeds V_{CC}.

The Limiter and All-Pass Circuit

An important aspect of the AMPS specification is concerned with the 12kHz maximum frequency deviation. The output of the APROC TX_{OUT} should be limited at a level which causes a maximum frequency deviation of 12kHz for the transmitter, regardless of the amplitude of the input signal. Figure 10 shows the equipment used for the test measurements and how the signal was processed. A 1kHz signal was applied to the input of the demo-board until a 5% distorted signal was measured at the limiter output. This waveform's peak-to-peak voltage was recorded as a reference. Then, at various chosen frequencies, the input of the demo-board was overdriven so we could record the distorted peak-to-peak waveform. (See Figure 11)

Formula 4 was used to calculate maximum frequency deviation from the waveforms shown in Figure 11.

$$\text{Max Freq Dev with All-Pass Ckt} = \left(\frac{BW_F}{BW_R}\right) 8\text{kHz} \quad (4)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure 11.

Table 9. Maximum Frequency Deviation Results for the 12kHz Test

Frequency (Hz)	With All-Pass (kHz)
300	3.58
500	5.61
800	10.13
1000	10.01
1200	9.21
2000	10.01
3000	9.61

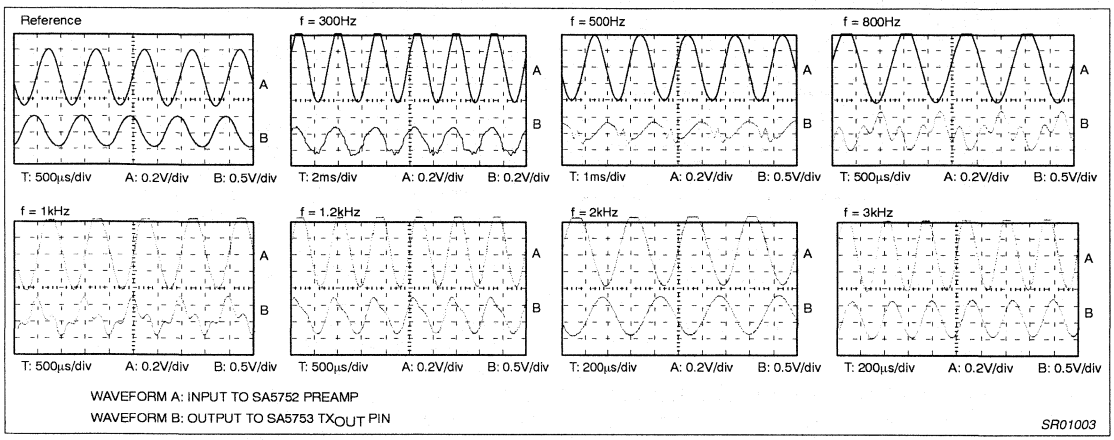


Figure 11. Results from the AMPS 12kHz Maximum Frequency Deviation Test

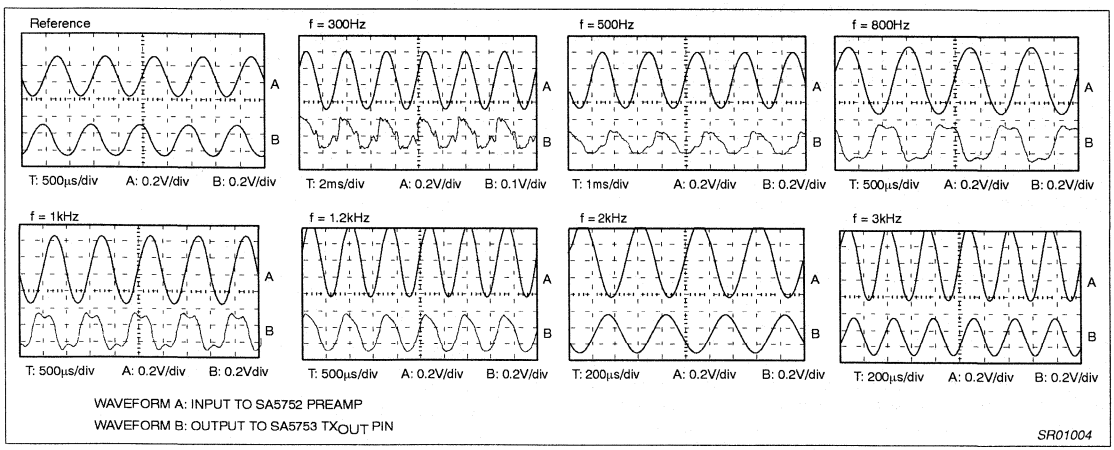


Figure 12. Results from the NAMPS 5kHz Maximum Frequency Deviation Test

Table 9 reveals the calculated results for maximum frequency deviation over the voice band. The test results show that the SA5752 and SA5753 will meet the 12kHz AMPS specification.

The same test set-up was used for the NAMPS measurements, however, the maximum frequency deviation formula changes. The following formula shows how to calculate the maximum frequency deviation for NAMPS:

$$\text{Max Freq Dev with All-Pass Ckt} = \left(\frac{BW_F}{BW_R}\right) 2.9\text{kHz} \quad (5)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure 12.

Table 10. Maximum Frequency Deviation Results for the 5kHz Test

Frequency (Hz)	With All-Pass (kHz)
300	1.48
500	2.11
800	3.27
1000	3.46
1200	3.42
2000	3.65
3000	3.56

Formula 5 was used to calculate the maximum frequency deviation in Table 10 from the waveforms shown in Figure 12. These test results show that the APROC II will meet the 5kHz maximum frequency deviation for NAMPS.

IV. EVALUATION SOFTWARE AND DEMOBOARD

The APROC II demoboard and evaluation software are for evaluation purposes only. It can help a designer understand the hardware and software functionality. The APROC II schematic and layout can be seen in Figures 13 and 14, respectively. The function of each external component is briefly shown in Figure 13.

In this software package, the screen (see Figure 15) only shows the signal path for the SA5753. Recall that for the audio processing chip, the signal is routed between the SA5752 and SA5753. The appropriate pin numbers are labeled to show where the signal enters and leaves the SA5753.

The upper half of the screen is the Tx path and the lower half of the window is the Rx path. To complete the signal path, a designer can use the computer's arrow keys to get to the area of interest. The space bar is used to toggle on and off path switches and key functions (like NAMPS, VCO, HPDN, VOX_{CTRL} etc).

The 'greater than' (>) or 'less than' (<) symbol keys on the key board are used to vary the value of the gain attenuator blocks. The way the gain attenuator blocks are programmed does not follow the logical way where the 'greater than' symbol key means going up in gain and the 'less than' symbol means decreases gain. Instead, the set up is programmed logically by the bits. So a user should use the 'greater than' and 'less than' symbol keys to vary the value, but continue to use the keys until the values stop changing. (See Table 11.)

To power down the chip set the following steps should be taken:

1. To power down the SA5752, move the marker to HPDN and hit the space bar to implement this function.

2. To implement one of the SA5753 three power down modes move the marker to the Power = 000 Bin and program the appropriate mode.

- For PWDN, set Power=1xx Bin; X=don't care
- For IDLE, set Power = 011 Bin
- For the DENA mode, set Power= 010 Bin
- For normal operation, set Power= 000 Bin
- For $DATA_{IN}$ to TX_{OUT} disabled, set Power= 001 Bin. This can be used for cordless applications

To power up the chip set, a designer needs to set the Power=000 Bin (for the SA5753) and toggle the HPDN section (for the SA5752).

DTMF

To implement the DTMF tones, a user can program the high and low tones by typing in the frequencies or programming the I^2C bits.

The high decimal value is from 2 to 257 where the frequency range is from off to 778.21Hz–66.66kHz. The low decimal value is from 2 to 257 where the frequency range is from off to 333.52Hz up to 28.57kHz.

The difference between the SA5753 DTMF generator and the SA5751 is that when the cycle is completed, the DC voltage goes back to 0V, whereas the SA5751 might not return to 0V. Therefore, upon switching back to the Tx voice path, a glitch may be heard from the SA5751, but not from the SA5753.

V. QUESTIONS AND ANSWERS SECTION

Q: I connected your evaluation board and software program but I do not see any output signal on the Transmit path. My input signal is connected to the Mic input of the SA5752. What is the problem?

A: There are several issues to look at. Make sure that the TxMute and RxMute pins are defined. If the registers are programmed such that the TxMute and/or RxMute pins need to be grounded for a signal to flow, please be sure that those pins are grounded.

If the registers are defined such that the TxMute and RxMute pins need V_{CC} connected to them for a completed signal path, please connect V_{CC} to the pins. Although leaving these pins open may work, it defines an open state and is, therefore, not guaranteed.

Q: When I program a DTMF tone, it only stays on for 96ms. How can I make it stay on longer?

A: The DTMF generator is designed to stay on for only 96ms. If a longer tone is desired, the DTMF registers must be re-loaded before the 96ms expires or set DTC = 1. For the evaluation program, the DTMF register can be loaded up automatically to observe the DTMF tone. Just toggle the space bar on the "DTMF frequency DTC" section.

Q: On the evaluation program, there are ADD field and REG values. What are these?

A: These are the registers (ADD = Address field and REG = the register) that must be programmed when using the SA5753 in the I^2C mode. The address field defines which portion of the chip is being accessed (See SA5753 data sheet for a detail look). The register bits control the functions of the block.

If a designer toggles in/out functions, they can see the registers which control that function. The Evaluation software is meant as a learning tool to aid the designer in getting up to speed.

Q: The SA5753 seems to be consuming more current than usual. Is this part damaged?

A: One area to look at is the I^2C clock. If the I^2C clock goes below ground, the SA5753 will draw more current. Therefore, be sure

that the I^2C clock is set at 1.2MHz square wave and it is from ground to V_{CC}.

Q: I have a Philips APROC II demoboard and a 5V I^2C interface board. At the present moment, I use two supplies to run the APROC II board at 3V and the interface board at 5V. Is there a 3V chip available that can be used for the interfacing between the computer's printer port to the I^2C section of the chip?

A: Yes, there is a 3V interface chip; the Philips PC74HC4049T. When a customer purchases an APROC II demoboard, he/she should receive an interface board. Most likely it will be the 3V version.

Q: The APROC II seems to draw more current than usual when I mute the TxMute and RxMute pins with a 5V logic '1' signal. The APROC II is operating at 3V. Is this normal, and if not, what can I do?

A: If you are going to operate the APROC II at 3V and apply 5V to the RxMute and TxMute pins, a series 10k resistor should be used to allow for this configuration.

If the logic '1' input is 3V and the APROC II is operating at 3V, the 10k resistor is not required. In general, it is safe to say that the logic '1' input should be no higher than V_{CC} if the 10k resistor is not used.

Q: I am evaluating your DTMF generator using the Philips evaluation program and demoboard. The frequency calculated and the frequency measured is correct but The evaluation screen, however, sometimes shows a different number, but the number shown is not too far off. Is there a bug in the program?

A: Yes, the program display is not correct. What you calculate and measure is fine. The program is incorrect at this time.

Q: I am evaluating the current consumption of the APROC II demoboard. I read a higher current than what is spec'd in the data sheet. What am I doing wrong?

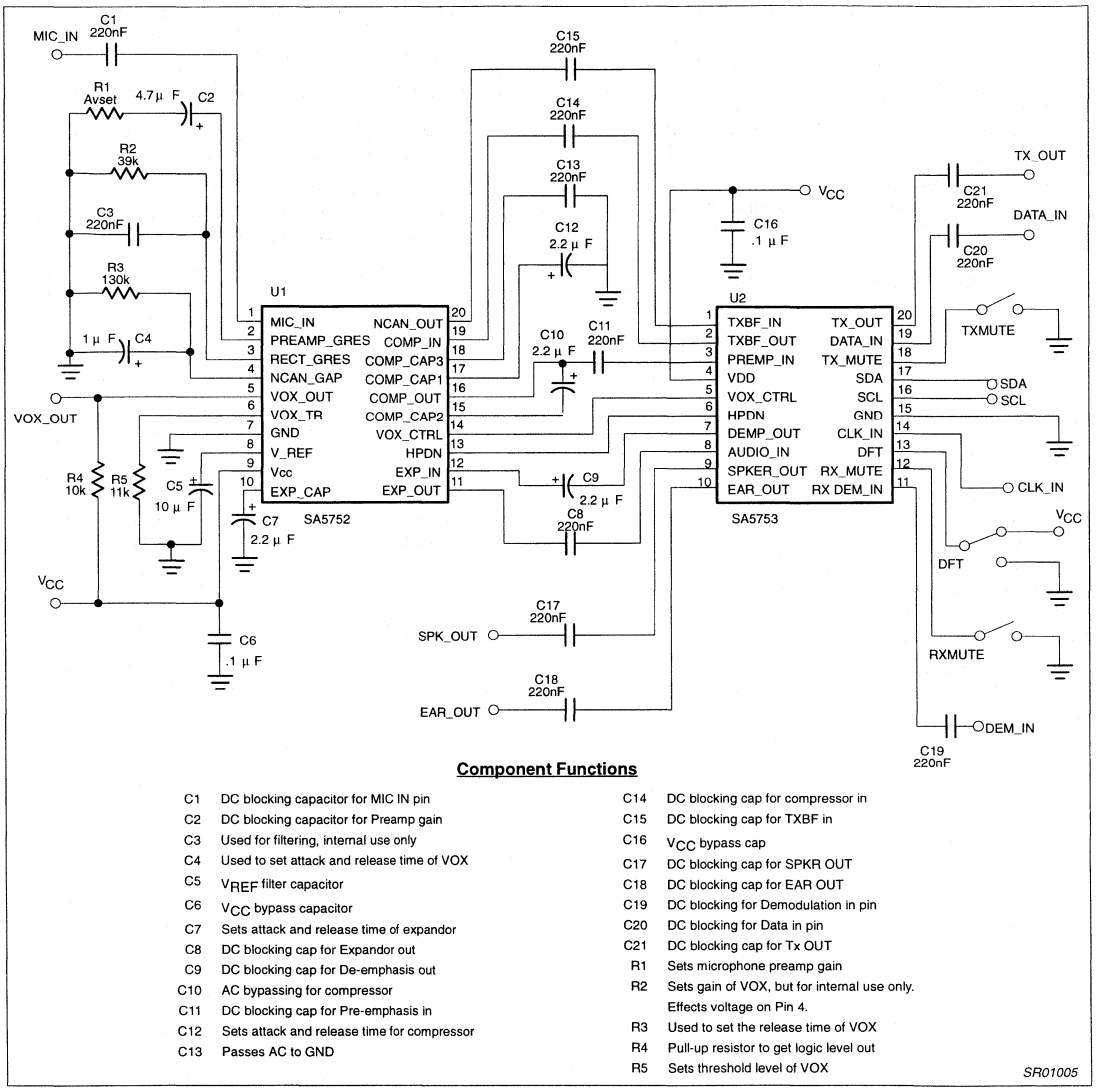
A: Remember that the I^2C interface card will draw some current away from the APROC II board (if it's connected that way). To avoid this problem, operate the I^2C interface card with a separate power supply and then measure the APROC II current.

Q: I have your APROC II evaluation demoboard. I am applying an input signal of 1kHz at $100mV_{RMS}$ to the MIC input and I am not getting any signal output on the TX_{OUT} pin. Any suggestions?

A: Your transmit path is probably open. To close the path you can do one of two things: either ground the TxP Mute pin (Pin 18) or redefine TxP to mute for a different input. You should also make sure that the SA5752 and SA5753 are in the power up state.

Q: I have a very unique situation using the SA5753. I would like to use the Default mode and I^2C mode in different situations. I know that the HPDN pin becomes an output when I^2C mode is implemented; and I know that the HPDN pin becomes an input when the Default mode is implemented. In my application I do not care about current consumption, therefore, the HPDN pin is not important to me. What can I do so that I don't leave the HPDN undefined, but at the same time, I allow myself to switch back and forth between the two modes?

A: For ease of use in the Default Mode without worrying about the function of the HPDN pin, the user can add an external pull-up resistor of 100kΩ between HPDN (Pin 6) and V_{DD}. This will put the SA5753 in Normal (active) Default operation when DFT (Pin 13) is pulled HIGH. For Power Down Mode the user will need to pull the HPDN pin LOW.



Component Functions

C1	DC blocking capacitor for MIC IN pin
C2	DC blocking capacitor for Preamp gain
C3	Used for filtering, internal use only
C4	Used to set attack and release time of VOX
C5	V_{REF} filter capacitor
C6	V_{CC} bypass capacitor
C7	Sets attack and release time of expandor
C8	DC blocking cap for Expandor out
C9	DC blocking cap for De-emphasis out
C10	AC bypassing for compressor
C11	DC blocking cap for Pre-emphasis in
C12	Sets attack and release time for compressor
C13	Passes AC to GND
C14	DC blocking cap for compressor in
C15	DC blocking cap for TXBF in
C16	V_{CC} bypass cap
C17	DC blocking cap for SPKR OUT
C18	DC blocking cap for EAR OUT
C19	DC blocking for Demodulation in pin
C20	DC blocking for Data in pin
C21	DC blocking cap for Tx OUT
R1	Sets microphone preamp gain
R2	Sets gain of VOX, but for internal use only. Effects voltage on Pin 4.
R3	Used to set the release time of VOX
R4	Pull-up resistor to get logic level out
R5	Sets threshold level of VOX

Figure 13. APROC II Evaluation Board Schematic

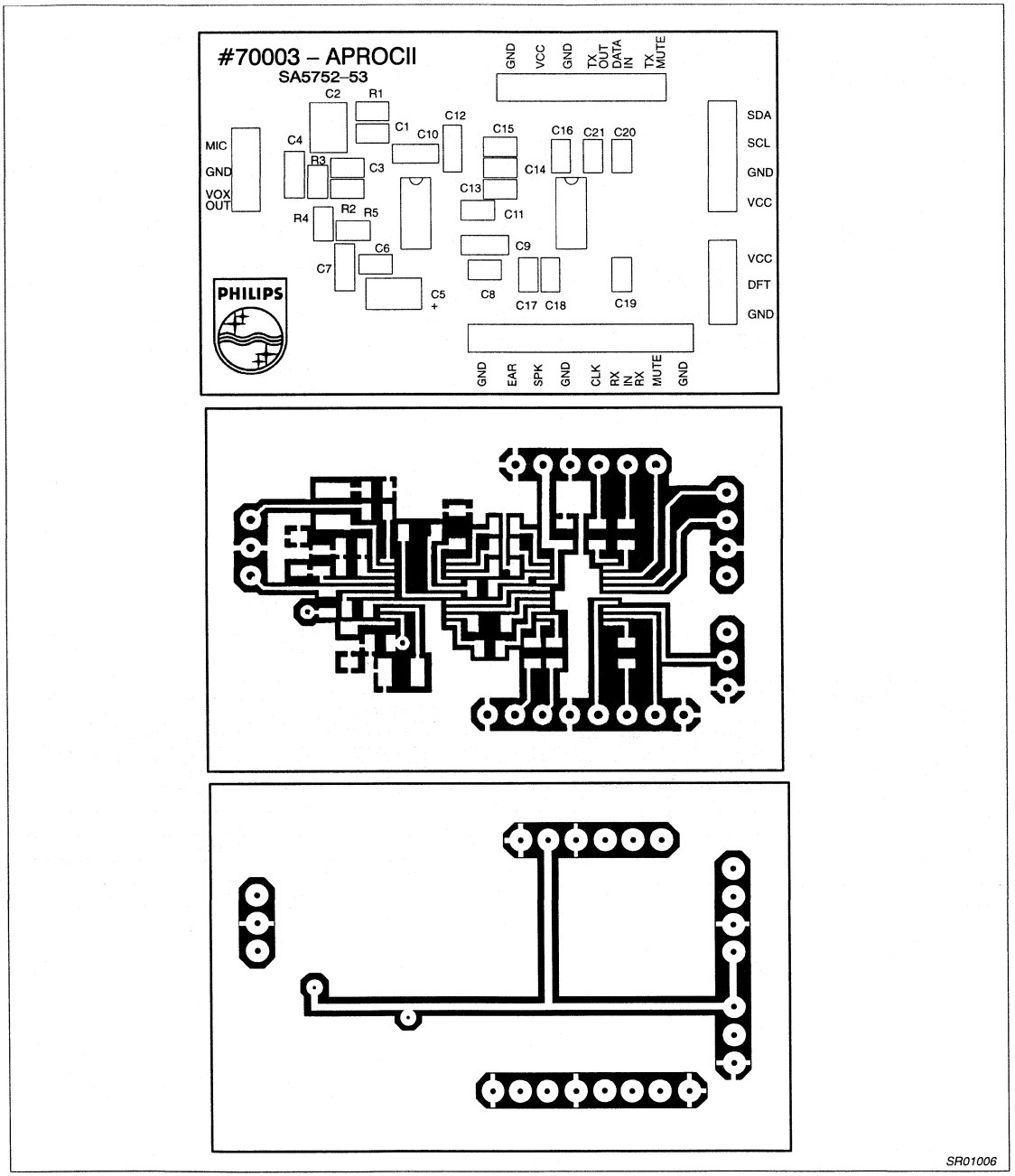


Figure 14. APROC II Evaluation Board Layouts

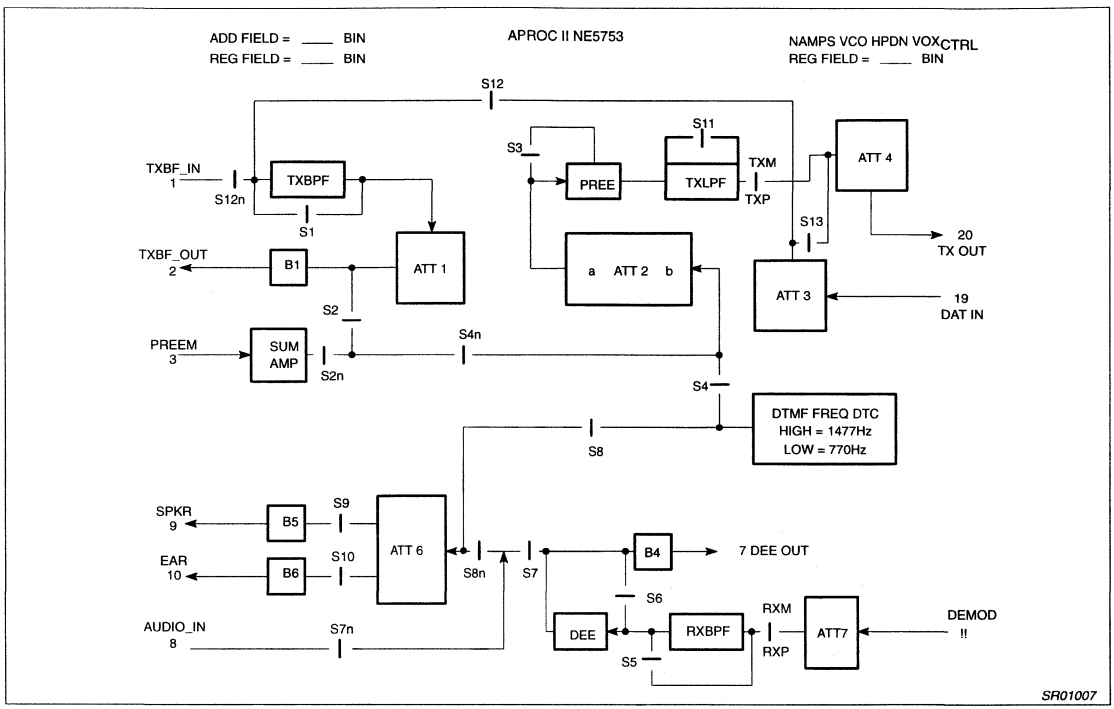


Figure 15. Graphical Display of SA5753 I²C Evaluation Program

Table 11. Gain Attenuator Steps

SYMBOL	Sequence of Gain Attenuator Steps
A1	0, –0.8, –1.6, –2.4, –3.2, –4.0, –4.8, –5.6, –6.4, –7.2, –8.0, –8.8, –9.6, –10.4 –11.2, –12
A2a	0, 0.25, 0.50, 0.75, 1.00, 1.25, 1.50, 1.75, 2.00, 2.25, 2.50, 2.75, 3.00, 3.25, 3.50, 3.75, 0, –0.25, –0.50, –0.75, –1.00, –1.25, –1.50, –1.75, –2.00, –2.25, –2.50, –2.75, –3.00, –3.25, –3.50, –3.75
A2b	0, –12, –18, –24
A3	–2, –3, –4, –5, –6, –7, –8, –9, –10, –11, –12, –13, –14, –15, –16, –17
A4	0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 0, –0.5, –1.0, –1.5, –2.0, –2.5, –3.0, –3.5
A6	0, –2, –4, –6, –8, –10, –12, –14, –16, –18, –20, –22, –24, –26, –28, –30
A7	0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 0, –0.5, –1, –1.5, –2, –2.5, –3, –3.5

Companding with the SA577 and SA578 AN1762

Author: Alvin K. Wong

INTRODUCTION

This application note is written for the designer who understands the basic functions of companding and wants to use the SA577 or SA578. If a designer is not familiar with the functionality of compandors, a good discussion can be found in the earlier Philips Semiconductors compandor data sheets and applications notes.

Key topics discussed in this paper are:

- How to program the unity gain level (0dB)
- How to implement an automatic level control
- How to get the best companding performance under strict design requirements
- How to set the attack and recovery time
- How to operate at 1.8V
- How to sum external signals using the SA578
- How to power-down the SA578
- How to mute the SA578
- How to use the SA577 and SA578 as a dual expandor

But before reviewing these areas, a summary of Philips Semiconductors compandor family will be presented. A system designer can then determine which compandor is best for the design.

SUMMARY OF COMPANDOR FAMILY

In the past, Philips Semiconductors offered four different types of compandors: the SA570, SA571, SA572, and SA575. Each of the four compandors has its own 'claim to fame'. The SA570 and SA571 are known to work well in high performance audio applications. The only real difference between the two is that the SA570 has a slight edge in performance. However when separate attack and recovery times are needed, the SA572 is the compandor to choose. The SA575 becomes useful when there are low voltage requirements.

With the increasing demand for low current consumption, good flexibility, and ease of use in semiconductors, Philips Semiconductors is offering three additional compandors to its family, the SA576, SA577 and SA578. These compandors typically require an I_{CC} of 1.4mA at a V_{CC} of 3.6V, but Philips Semiconductors has demonstrated that these new chips are functional down to 1.8V.

In addition to having low power consumption, the SA578 has a power-down mode. In this mode, the chip consumes only 170µA. This power-down mode is useful when the functionality of the chip is not needed at all times. In the power-down mode , the SA578 maintains all of its pin voltages at all their normal DC operating voltages. Because all of the capacitors remain charged in this mode, the power-up state will occur quickly. Powering down automatically mutes the SA578. Having the mute function internal to the SA578 audio section eliminates the need for an external switch. The SA578 is the only compandor in the family that has power-down and mute functions.

To allow for greater flexibility, the 0dB level is now programmable for the SA577 and SA578. However, for the SA576, the 0dB level is specified and set at $100mV_{RMS}$. The earlier compandors also have a set unity gain (0dB) level. The SA570 and SA571 have a set 0dB level at $775mV_{RMS}$. While the SA572 and the SA575 both have their 0dB levels at $100mV_{RMS}$. If a designer wanted a different 0dB level, two op amps would have to be implemented in the design. One of the op amps would connect to the input of the compandor, while the other op amp would connect to the output. But with the SA577 and SA578, these external op amps are no longer needed. The 0dB level can be programmed from $10mV_{RMS}$ to $1V_{RMS}$ with three external resistors.

Many of the external parts in the previous family of compandors are now internal to the device. Additionally, the left side of the chip is configured as an expandor, and the right side is configured as a compressor. This allows for minimum part count and fewer variations in systems design. The external capacitors are also reduced in value which saves board space and cost. The only trade-off with using smaller capacitors is that there is less filtering. Because of this new approach, the SA576, SA577 and SA578 are easy to implement in any design.

Table 1 shows a brief summary of all the compandors. The seven different compandors offer a wide range of flexibility: different types of packages, power-down capability, programmable or fixed unity gain, different reference voltages, a wide range of operating voltages and currents, different pin outs, etc. From this information, a designer can quickly choose a compandor which best meets the design requirements. After a compandor is chosen from the table, a designer can find additional help from data sheets and application notes.

Since power consumption is important in most designs, it is important to discuss them in this application note. The SA570, SA571, and SA572 have built in voltage regulators, therefore, the current consumption remains roughly the same over the specified supply voltages. This can be especially useful when the power supply is not regulated very well. However with the SA575, SA576, SA577, and SA578, the current consumption will drop as the supply voltage decreases. For this, the power consumption will drop also. This means one can operate the part at a very low power level. This is a good feature for any design having strict power consumption guidelines.

INTRODUCING SA577 AND SA578

Figure 1 and 2 show block diagrams of the SA577 and SA578 respectively. The only substantial difference between the two is that the SA578 has a power-down capability, mute function and summing capabilities (for signals like DTMF tones). In addition the SA578 summing amplifiers are capable of driving 600Ω loads. Listed below are the basic functions of each external component for Figure 1 (SA577).

Table 1. Compandor Family Overview

	SA570	SA571	SA572	SA575	SA576	SA577	SA578
V_{CC}	6–24V	6–18V	6–22V	3–7V	2–7V	2–7V	2–7V
I_{CC}	3.2mA	3.2mA	6mA	3–5.5mA*	1–3mA*	1–2mA*	1–2mA*
Number of Pins	16	16	16	20	14	14	16
Packages SA: 0 to +70°C SA: –40 to +85°C N: Plastic DIP D: Plastic SO F: Ceramic DIP DK: SSOP (Shrink Small Outline Package)	SA570F SA570N SA570D	SA571F SA571N SA571D SA571F SA571N SA571D	SA572N SA572D SA572F SA572N SA572D	SA575N SA575D SA575DJ SA575N SA575D SA575DK	SA576N SA576D SA576N SA576D	SA577N SA577D SA577N SA577D	SA578N SA578D SA578N SA578D
ALC (Automatic Level Control)	Both Channels	Both Channels	Both Channels	Right Channel	Right Channel	Right Channel	Right Channel
Reference Voltage	Fixed 1.8V	Fixed 1.8V	Fixed 2.5V	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2
Unity Gain	775mV_{RMS}	775mV_{RMS}	100mV_{RMS}	100mV_{RMS}	100mV_{RMS}	10mV to 1V_{RMS}	10mV to 1V_{RMS}
Power-Down	NO	NO	NO	NO	NO	NO	YES (170µA)
Key Features	-Excellent Unity Gain Tracking Error -Excellent THD	-Excellent Unity Gain Tracking Error -Excellent THD	-Independent Attack & Recovery Time -Good THD -Needs ext. summing op amp	-2 Uncommited on-chip op amps available -Low voltage	-Low power -Low external component count	-Low power -Programmable unity gain	-Low power -Programmable unity gain -Power down -Mute function -Summing capability (DTMF) -600Ω drive capability
Applications Cordless Phones Cellular Phones Wireless Mics Modems Consumer Audio Two-way Communications	High performance audio circuits "Hi–Fi Commercial Quality"	High performance audio circuits "Hi–Fi Commercial Quality"	High performance audio circuits "Hi–Fi Studio Quality"	Consumer audio circuits "Commercial Quality"	Battery powered systems "Commercial Quality"	Battery powered systems "Commercial Quality"	Battery powered systems "Commercial Quality"

NOTES: SA5750/5751 are also excellent audio processor components for high performance cordless and cellular applications that include the companding function..
*I_{CC} varies with V_{CC}.

R1 – Determines the Unity Gain Level for the Expandor

R2 – Determines What Value the Reference Current (I_{REF}) will be for the Part (Also Affects Unity Gain Level)

R3 – Determines the Unity Gain Level for the Compressor

C1 – DC Blocking Capacitor

C2 – Determines the Attack and Recovery Time for the Expandor

C3 – DC Blocking Capacitor

C4 – Used to AC Ground the V_{REF} Pin

C5 – Provides AC Path from Gain Cell to Output of Summing Amp

C6 – Determines the Attack and Recovery Time for the Compressor

C7 – DC Blocking Capacitor

C8 – Provides AC Ground for the DC Feedback Path

C9 – DC Blocking Capacitor

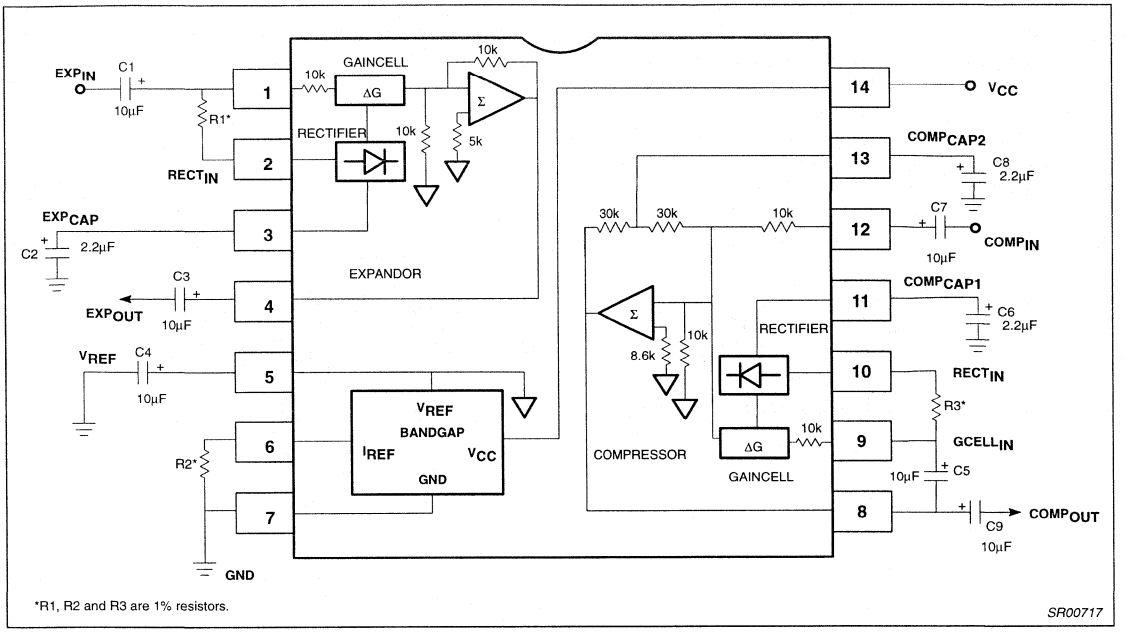


Figure 1 . SA577 Block Diagram

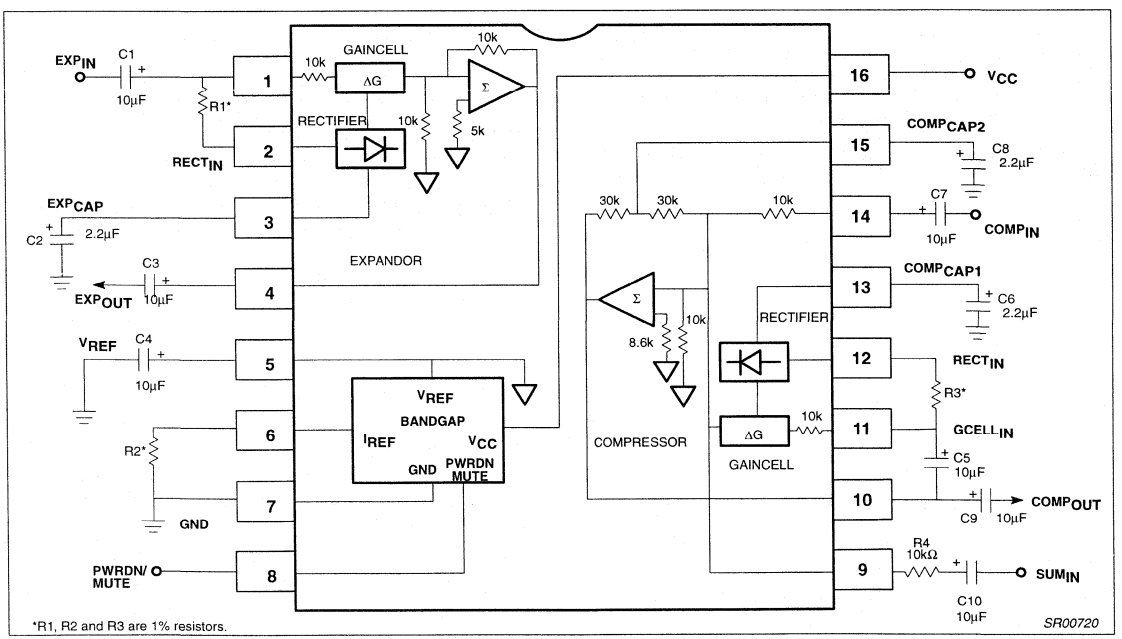


Figure 2 . SA578 Block Diagram

Listed below are the basic functions of each external component for Figure 2 (SA578).

R1 – Determines the Unity Gain Level for the Expandor

R2 – Determines What Value the Reference Current (I_{REF}) will be for the Part (Also Affects Unity Gain Level)

R3 – Determines the Unity Gain Level for the Compressor

R4 – Used to Set the Gain of an External Signal like DTMF Tones and Sum them with the Companded Signal

C1 – DC Blocking Capacitor

C2 – Determines the Attack and Recovery Time for the Expandor

C3 – DC Blocking Capacitor

C4 – Used to AC Ground the V_{REF} Pin

C5 – Provides AC Path from Gain Cell to Output of Summing Amp

C6 – Determines the Attack and Recovery Time for the Compressor

C7 – DC Blocking Capacitor

C8 – Provides AC Ground for the DC Feedback Path

C9 – DC Blocking Capacitor

C10 – DC Blocking Capacitor

HOW TO PROGRAM THE UNITY GAIN LEVEL (0dB)

Three external resistors R1, R2, and R3 define the unity gain level. Both the SA577 and the SA578 0dB levels can vary from $10mV_{RMS}$ to $1.0V_{RMS}$. These limits are used in product characterization, but these parts can function over a wider 0dB level range.

In most applications the 0dB level is equal for both the compressor and expandor side. Therefore, R1 and R3 are equal in value. R3 sets the 0dB level for the compressor side, and R1 sets the 0dB level for the expandor side. However, there could be a situation where a design requires different 0dB levels for compression and expansion. This will not be a problem with the SA577 or SA578, due to the separate 0dB level programming.

Using the formulas below, a designer can calculate the resistor values for a desired unity gain level.

Formula 1: $$R_2 = \frac{V_{BG}}{I_{REF}}$$

where
V_{BG} = Bandgap Voltage
I_{REF} = Reference Current
(V_{BG} is brought out on Pin 6 and R2 determines the I_{REF} value)

Formula 2: $$R_1 = \frac{0.9 \cdot V_{IN_{RMS}}}{I_{REF}}$$

where $V_{IN_{RMS}}$ is the 0dB level
($R_1 = R_3$ in most cases)

Programming the Unity Gain Level for the SA577 also applies for the SA578.

Example:

Program the SA577 or SA578 for a 0dB Level at $100mV_{RMS}$

Step 1: V_{BG}=1.26V.....Typically
I_{REF}=12.6μA.....Good Starting Point

$$R_2 = \frac{1.26V}{12.6\pi A}$$

R_2 = 100k

Step 2:

$$R_1 = R_3 = \frac{0.9V_{IN_{RMS}}}{I_{REF}}$$

$$R_1 = R_3 = \frac{(0.9V)\ (100mV_{RMS})}{12.6\pi A}$$

$\therefore R_1 = R_3 = 7.15k$

Step 3: $R_1 = R_3 = 7.15k$ (1% value)
R_2 = 100k (1% value)

Step 4: Plug in these resistor values and measure for unity gain. Adjust accordingly for accuracy.

NOTE: Rough Limits for Resistors:
$1k \leq R1 \leq 100k$ (1% values)
$20k \leq R2 \leq 200k$ (1% values)
$1k \leq R3 \leq 100k$ (1% values)

Rough Limits for I_{REF}
$6.3\mu A \leq I_{REF} \leq 63\mu A$

The example above gives pretty close results. A designer should use 1% resistors to get the best performance. Below in Table 2 are some recommended values to get started:

Table 2. Recommended Resistor Values for Different 0dB Levels

0dB Level	dBv	R_2	R_1 & R_3
$1.0V_{RMS}$	0	24.3k	18.7k
$316.2mV_{RMS}$	–10	100k	22.6k
$100mV_{RMS}$	–20	100k	7.15k
$10mV_{RMS}$	–40	200k	1.33k

PARAMETERS THAT LIMIT THE DYNAMIC RANGE

The above example is a good place to start, but to get the optimum performance from the SA577 and SA578, a designer needs to understand certain key parameters. I_{REF} is important because it determines the values for all three resistors (R1, R2, and R3). Since I_{REF} is directly related to I_{CC} (see Figure 3), one should be careful in choosing a value. If one chooses a high I_{REF} current, power consumption goes up. However the output signal will have excellent low level distortion (see Figures 4 and 5). If one chooses a low I_{REF} value, distortion at the output will increase slightly. Conversely, the power consumption is reduced, which might be worth the trade-off in battery operated designs.

The dynamic range of the SA577 and SA578 is determined by supply voltage (V_{CC}) and reference current (I_{REF}). I_{REF} determines how well the compandor will perform with low level input signals. The supply voltage determines how high (in level) an input signal can be before clipping appears on the output (in some cases increasing I_{REF} also helps). A designer needs to estimate the input

range going into the compandor so that an appropriate V_{CC} and I_{REF} can be chosen.

The bandgap voltage (V_{BG}) slightly varies over a wide range of I_{REF} currents (Figure 6). Figure 7 shows how I_{REF} varies with R2. The higher R2 is, the lower I_{REF} is. Figure 8 shows how the dynamic range varies over different values of I_{REF} (the higher the supply voltage the better the dynamic range). The graphs in Figures 3 - 8 were taken at V_{CC}=3.6V, F=1kHz and 0dB level=100mV_{RMS}. The I_{REF} current was limited between 5μA and 40μA.

It can be seen that I_{REF} plays an important role in current consumption, THD, and dynamic range. With the aid of these figures, one can determine an I_{REF} which meets the design goals.

Example:
Making use of the graphs in Figures 3 - 8 and formulas 1 and 2, design a compandor with a 0dB level of 100mV_{RMS}. Try to achieve a THD of 0.1 on the compressor side with wide dynamic range. Operate at a supply voltage of 3.6V but with the lowest possible current consumption.

Step 1: According to Figure 5, an I_{REF} of 30μA is required for approximately 0.1% distortion.

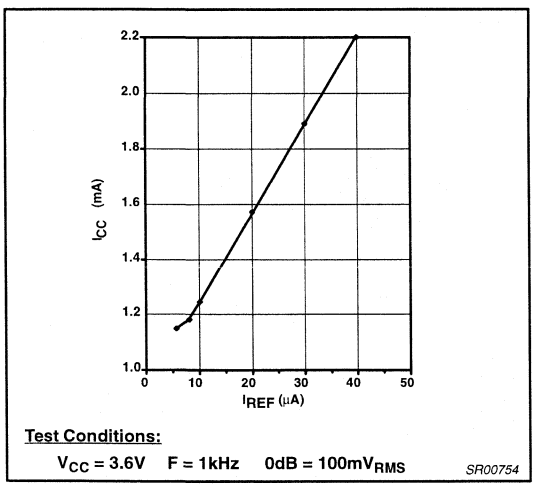


Figure 3 . I_{REF} vs I_{CC}

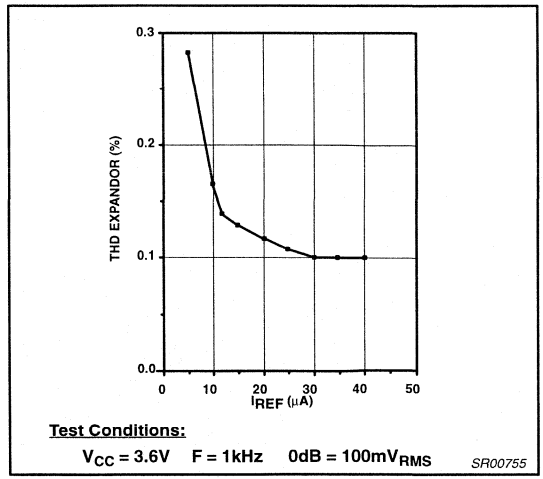


Figure 4 . I_{REF} vs THD, Expandor Side

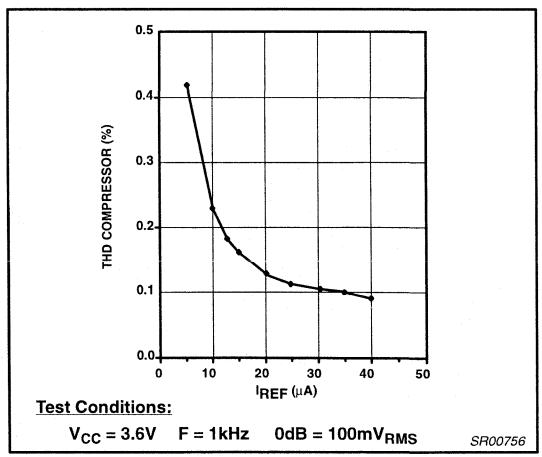


Figure 5 . I_{REF} vs THD, Compressor Side

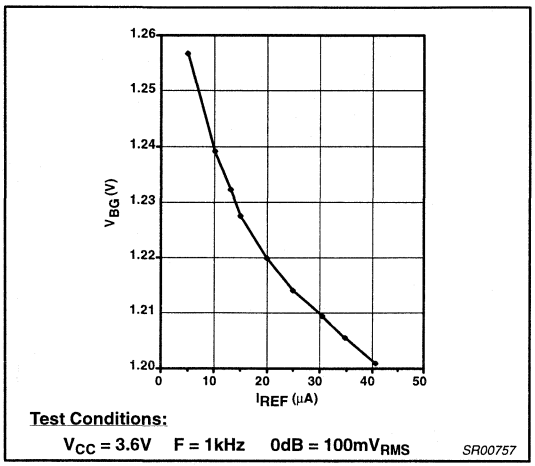


Figure 6 . I_{REF} vs V_{BG}

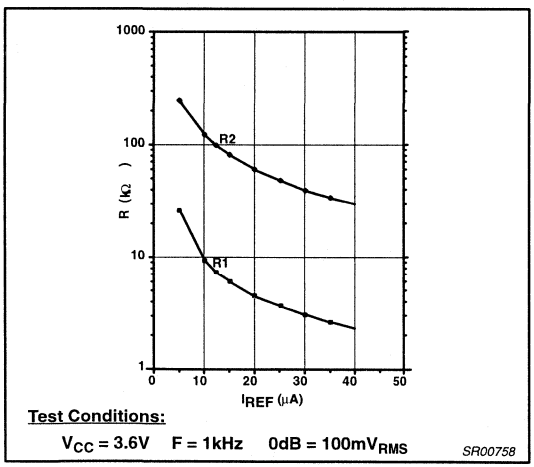


Figure 7 . I_{REF} vs R2, R1

Step 2: From Figure 8, the dynamic range is approximately 92dB. So far the requirements have been met.

Step 3: Figure 3 shows us that I_{CC} is at 1.9mA with no input signal (that's not bad at all!).

Step 4: Calculating R1, R2, and R3

Graphical Method:
From Figure 7: For I_{REF}=30μA and 0dB=100mV_{RMS} R1=R3=3k R2=40k

Actual resistors available: R1=R3=3.01k (1%) R2=40.2k (1%)

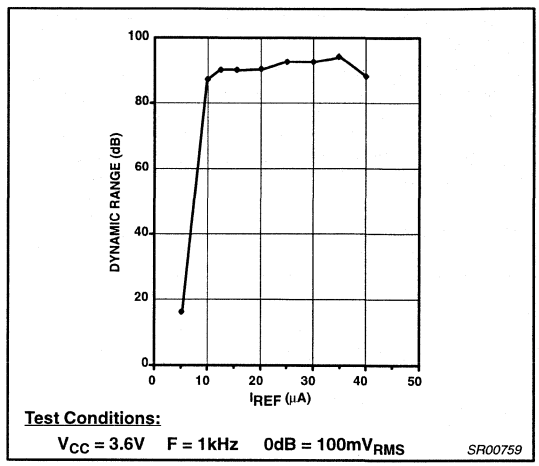


Figure 8 . I_{REF} vs Dynamic Range

Formula Method:
From Figure 6: V_{BG}=1.21V for I_{REF}=30μA therefore, using formula 1:

$$R_2 = \frac{V_{BG}}{I_{REF}}$$

$$R_2 = \frac{1.21V}{30\pi A}$$

R_2 = 40.33k

R_2 = 40.2k (available in 1%)

Recall from formula 2:

$$R_1 = \frac{0.9V_{IN_{RMS}}}{I_{REF}}$$

$$R_1 = \frac{(0.9V)\ (100mV_{RMS})}{30\pi A}$$

R_1 = 3k

R_1 = 3.01k (available in 1%)

Connect these external resistors with the determined values and adjust for optimum performance.

Bench results:
After completing the exercise above, the resistors were connected and the results are given below.

I_{CC} = 1.89mA (with no input signal)
THD = 0.1 (meausured on spectrum analyzer)
0dB = 109mV_{RMS} (off by 0.8dB...good!) Dynamic Range = 92dB

These results are very close to what was predicted and by tweaking R1 and R3, the 0dB error can be further reduced to zero.

BANDWIDTH OF COMPANDOR

Figure 9 shows the typical bandwidth for the SA577 and SA578. The graphs were taken with a V_{CC} of 3.6V and a 0dB level of 100mV_{RMS}. The bandwidth of the expandor, the compressor, and the compandor (where a signal goes through the compressor and the expandor) is shown in this figure. Although the SA577 and SA578 are conservatively specified with a 20kHz bandwidth, Figure 9 reveals that it is actually around 300kHz.

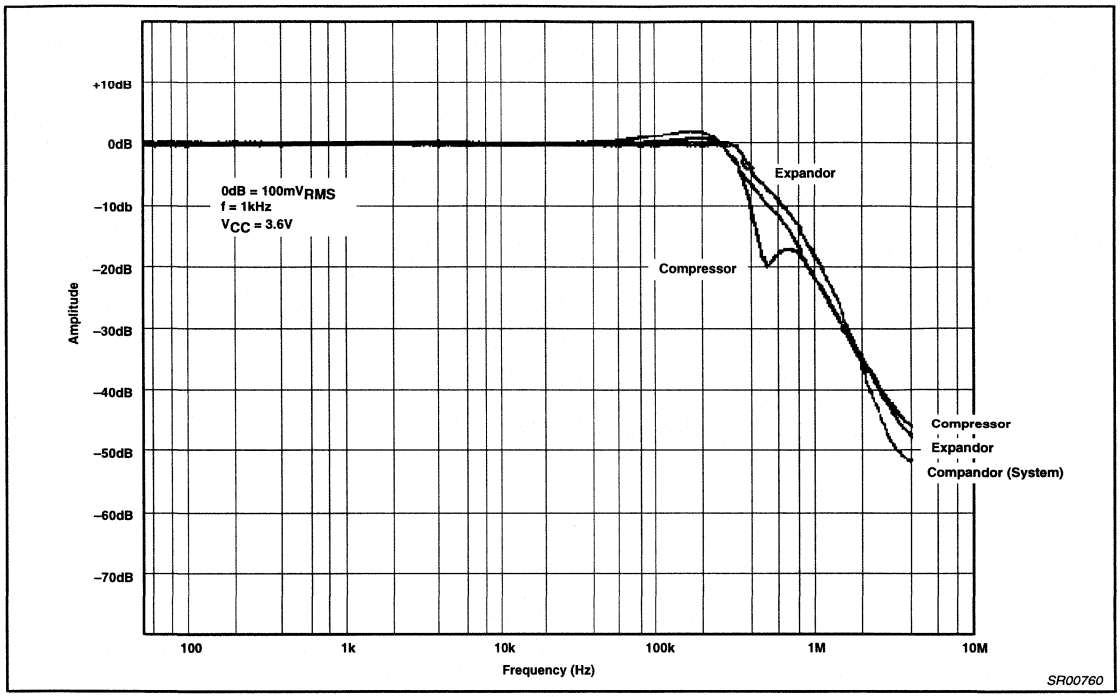


Figure 9 . Bandwidth of SA577 and SA578 Demo Board

HOW TO SET THE ATTACK AND RECOVERY TIMES

C2 and C6, from figures 1 and 2, set the attack and recovery times for the SA577 and SA578. Application Note 174 (AN174) defines A and R times and also describes how they are measured on the bench. Formula 3 shows how the A and R time can be calculated.

Formula 3:

Attack Time [ms] = 10k * C2 or C6
Release Time [ms] = 4 * Attack Time

Although a fast attack time is desirable, one must remember that there is a trade-off with low distortion. As a general rule, a 1µF capacitor for C2 will produce 0.2% THD at 1kHz. Since CCITT recommends an RC time constant of 20ms for the attack time, a 2µF capacitor is recommended for telephony applications because it has only 0.1% THD at 1kHz and 0.33% at 800Hz.

Note: AN174 can be found in the 1989 Linear Data Manual, Volume 1, or the RF Handbook.

IMPLEMENTING A PROGRAMMABLE AUTOMATIC LEVEL CONTROL

The function of an automatic level control (ALC) is to take a given range of input signals and provide a constant AC output level. This type of function is useful in many audio applications. One such application can be found in tape recorders. When a tape recorder with ALC is recording a conversation, a soft spoken person will be heard just as well as a loud spoken person during play back.

Another useful application for ALC could be with telephony. A person who has difficulty hearing, will not have to ask the other party to speak up. If the phone already has a volume control, the user has to adjust the volume for different parties. But with the ALC, the volume only has to be set once.

Different constant AC output levels of an ALC can be 'programmed' with the SA577 and SA578. This allows the designer to choose the output level that is needed in the design, and eliminates the need for an external op amp.

The compressor side of the SA577 and SA578 can be configured to function as an automatic level control (ALC). Figure 10 and 11 show how this can be done. The circuit shown for the SA577/78 ALC is set up to provide a constant output level of $100mV_{RMS}$ with an input range from –34dB to +20dB at 1kHz (see Figure 12).

Below are some design equations for the ALC:

$$\text{AC output level}(V_{RMS}) = \left[\frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a}}\right] \cdot 1.11 \qquad \text{Eq 1.}$$

where $R_{1_a} = R_{2_a} = 10k$ (internal)

$$I_{REF} = \frac{V_{BG}}{R_2}$$

$$\text{Maximum Gain} = \frac{4(R_3 + R_X) \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{CC}} \qquad \text{Eq 2.}$$

$$\text{Gain} = \frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{IN_{RMS}}} \qquad \text{Eq 3.}$$

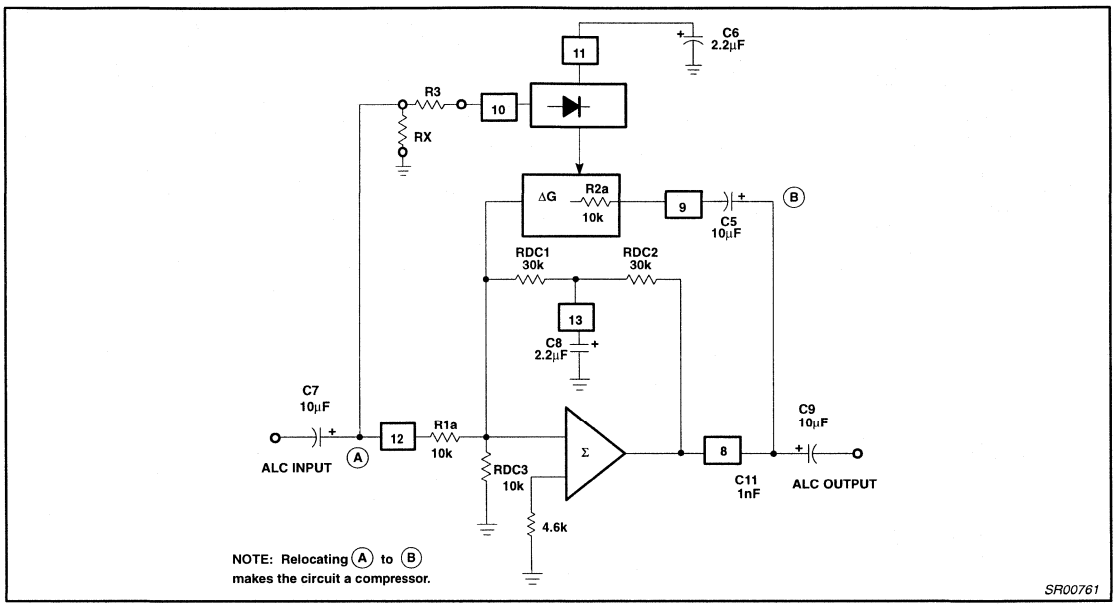


Figure 10 . SA577 ALC Configuration

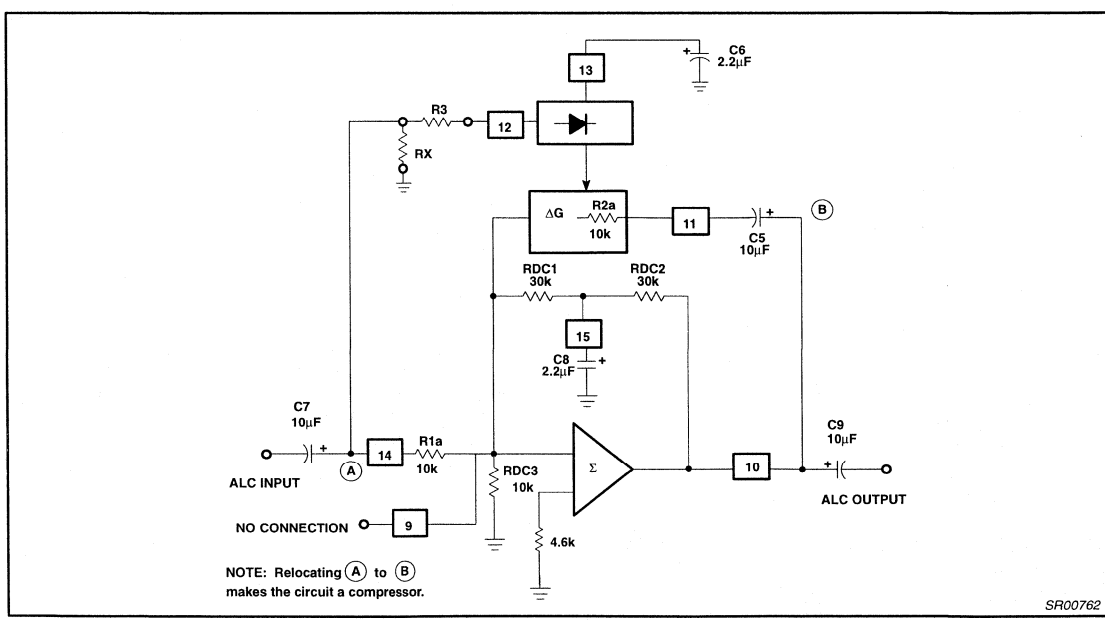


Figure 11 . SA578 ALC Configuration

Example:
Design an ALC with a constant output level of $100mV_{RMS}$ with a maximum gain of 10.

Step 1: From Eq 1

$$\text{AC output level}(V_{RMS}) = \left[\frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a}}\right] \cdot 1.11$$

where $R_{1_a} = R_{2_a} = 10k$ (internal)

$$I_{REF} = \frac{V_{BG}}{R_2}$$

In terms of R_3

$$R_3 = \frac{[\text{AC output level}(V_{RMS})]\ R_{1_a}}{(1.11)\ (R_{2_a})\ I_{REF}}$$

assuming $R_2 = 100k$ and $V_{BG} = 1.26V$.

$$R_3 = \frac{100mV_{RMS} \cdot 10k}{1.11 \cdot 10k \cdot 12.6\pi A}$$

$$R_3 = 7.15k$$

Step 2: From Eq 2

$$\text{Maximum Gain} = \frac{4(R_3 + R_X) \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{CC}}$$

In terms of R_X

$$R_X = \frac{(\text{Max. Gain})\ (V_{CC})\ (R_{1_a})}{4R_{2_a} \cdot I_{REF}} - R_3$$

$$R_X = \frac{(10)\ (3.6V)\ (10k)}{4\ (10k)\ 12.6\pi A} - 7.15k$$

$$R_X = 707.1k$$

$$R_X = 715k \text{ (available)}$$

Step 3:

–connect resistors to circuit
–measure AC output level and adjust R3 for best accuracy
–check maximum gain by applying a low input level and adjust Rx for best results

Figure 12 shows the characteristics of the SA577/578 ALC circuit without Rx. The output stays at a constant $100mV_{RMS}$ level for a wide range of different input AC voltages. Any AC input signal above the cross-over point (unity gain level) is attenuated while any signal below the cross-over point is amplified. The cross-over point is where the input signal is equal to the output signal, where $A_V=1$.

Figure 13 reveals the dynamic range of the SA577 ALC circuit using Rx. The input range of the ALC is reduced. Instead of a $2mV_{RMS}$ input signal to get $100mV_{RMS}$ on the output, a $10mV_{RMS}$ input signal is now required (for Rx=681k). The purpose of limiting the maximum gain of the circuit is to prevent amplification of background noise. To alleviate this problem, Rx is used. Since the ALC was designed with a maximum gain of 10, any input signal below 10mV will not be amplified with a gain greater than 10 ($100mv_{RMS}/10=10mv_{RMS}$). Using Rx can be an advantage because the threshold of the ALC can be set.

Figure 14 shows that as Rx increases so does A_V. In some applications it might be useful to make Rx a potentiometer. This will allow the user to adjust the threshold for different environmental conditions.

Figures 15-18 show the results of using the ALC for different constant output levels. V_{CC} and I_{REF} limit the dynamic range. The upper part of the range can be increased by either increasing V_{CC} and/or I_{REF}. The lower part of the range can be improved by increasing I_{REF}.

EXTRA FEATURES FOR SA578

The SA578 has three extra functions over the SA577. These are power-down, mute and summing capabilities. To implement the power-down/mute mode, Pin 8 should be active low (open collector configuration, see Figure 19). If the power-down/mute feature is not used, Pin 8 should be left open. The SA578 only consumes 170μA of current at 3.6V when Pin 8 is activated. The power-down/mute mode is useful in designs when the function of the chip is not utilized at all times. This feature is a necessity where power conservation is critical.

In cellular and cordless applications, it is common to mix DTMF tones with the audio signal. This usually requires another op amp in which to mix the signals. With the SA578, however, the DTMF tones can be mixed internally on the compressor side. The DTMF signal is also compressed with the audio signal and ready for data transmission. Figure 2 shows that the summing of signals can be done at Pin 9 with R4 and C10. If amplification is not needed, then a 10k resistor is a recommended value for R4. In addition the summing amplifiers are capable of driving 600Ω loads.

THE SA577 AND SA578 AS A DUAL EXPANDOR

The compressor side can actually be configured as an expandor for both the SA577 and SA578. Figure 20 shows how this can be done. Because Pin 9 of the SA578 is available to the designer, the compressor side can not only be configured as an expandor, but as an expandor with summing capabilities.

OPERATING AT 1.8V

The SA577 and SA578 can operate at 1.8V.

SA577 AND SA578 DEMO BOARDS

Figures 21 shows the DIP package layout for the SA577 and SA578 demo boards, respectively. Figures 22 shows the SO layout for the SA577 and SA578 demo boards, respectively. The layouts are configured such that R1, R2, R3, and Rx can be removed and replaced easily. A switch is also available to change the operating mode of the compressor to an ALC configuration and vice versa (position the switch to the right for ALC mode).

When the compressor side is being evaluated, disconnect Rx completely from the socket on the demo boards. Rx should only be used when the compandor is being used for ALC.

For the SA578 demo board, two extra post are available. One is for power-down; the other is for summing external signals. To power-down, simply ground this post. To sum signals, connect the external signal to the proper post.

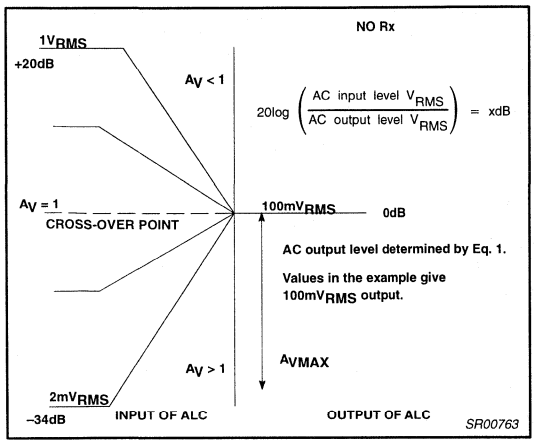


Figure 12 . Dynamic Range of SA577 ALC Demonstration Board Without R_X

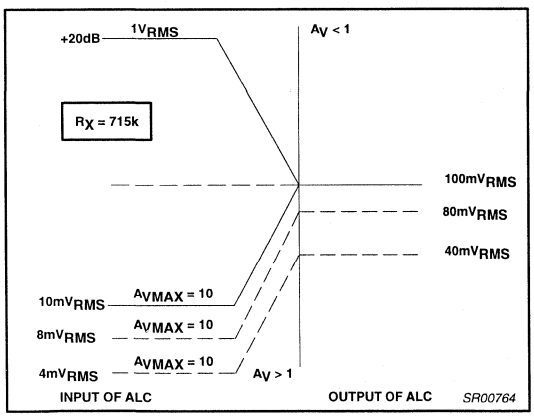


Figure 13 . Dynamic Range of SA577 ALC Demo Board with R_X = 715kΩ

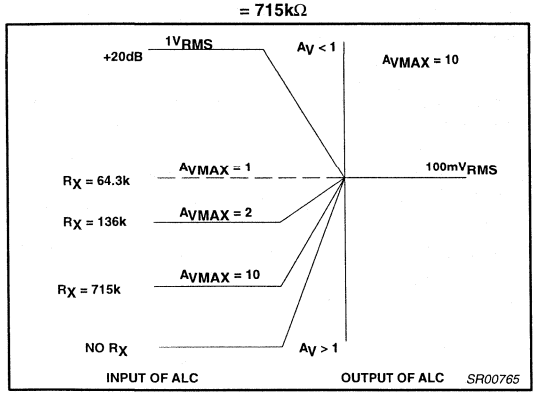


Figure 14 . Dynamic Range of SA577 ALC Demo Board with Different R_X Values

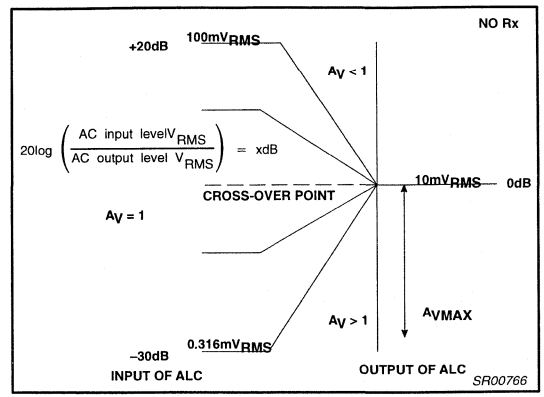


Figure 15 . SA577 ALC: AC Output Level = 10mV$_{RMS}$

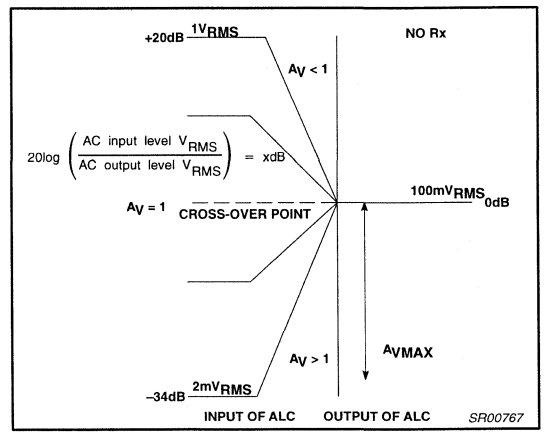


Figure 16 . SA577 ALC: AC Output Level = 100mV$_{RMS}$

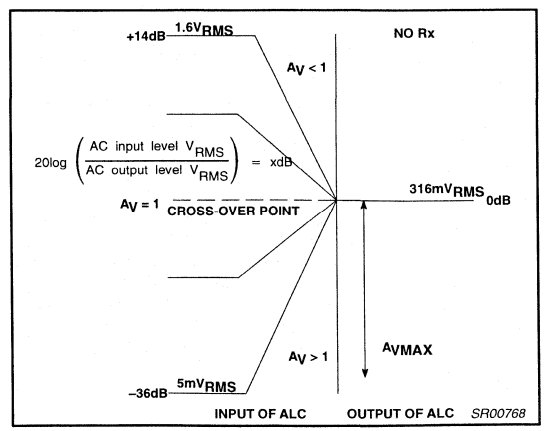


Figure 17 . SA577 ALC: AC Output Level = 316mV$_{RMS}$

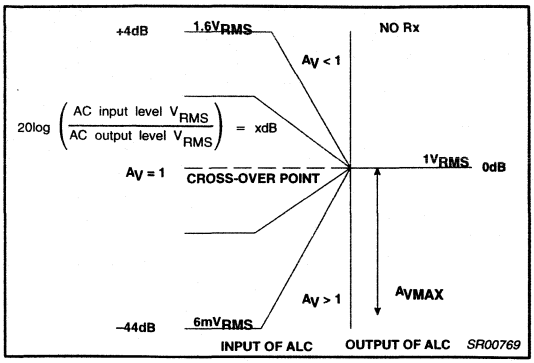


Figure 18 . SA577 ALC: AC Output Level = $1V_{RMS}$

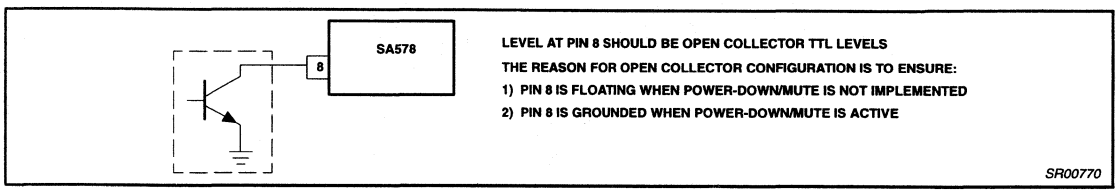


Figure 19 . Proper Use of SA578 Pin 8

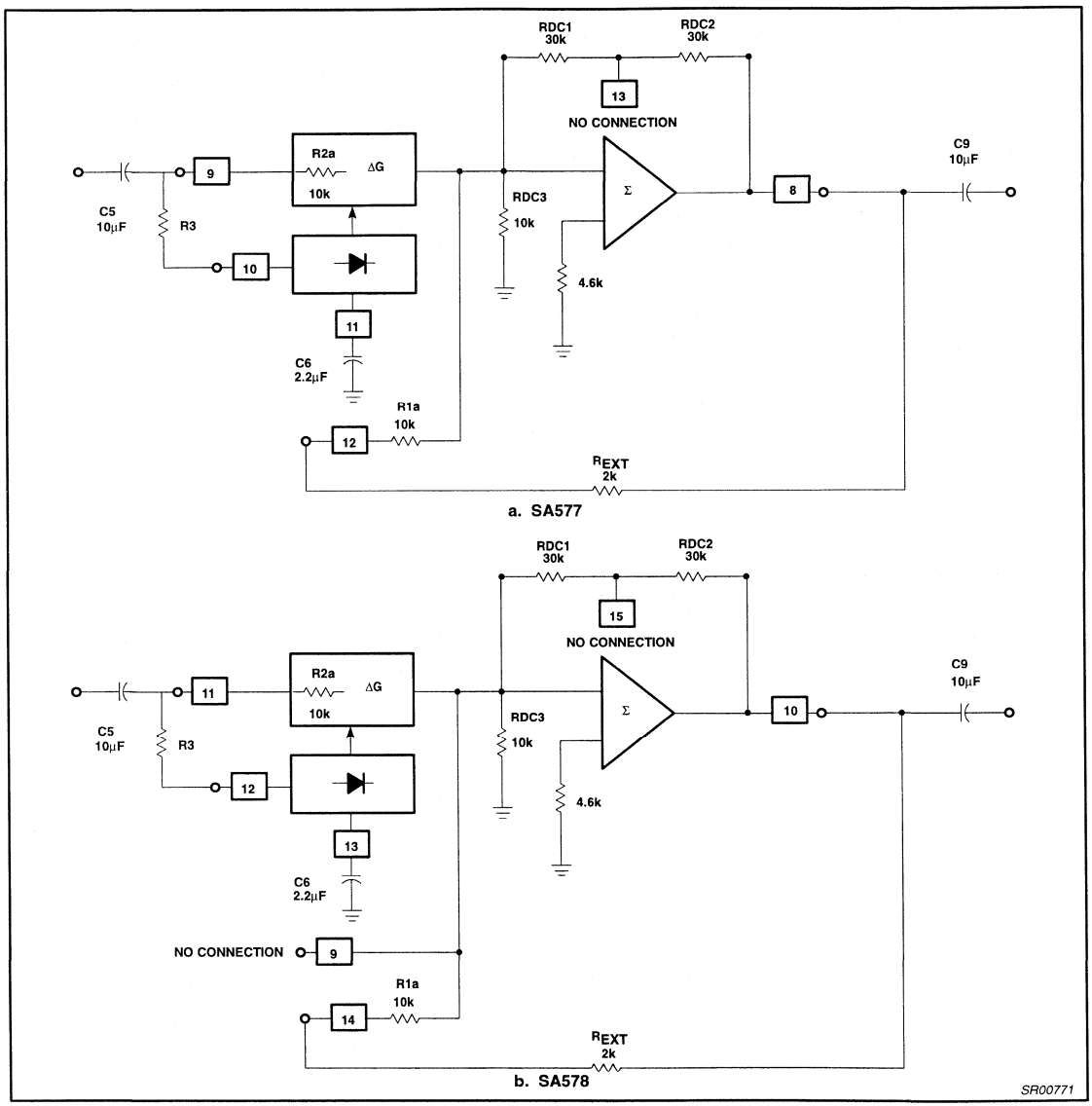
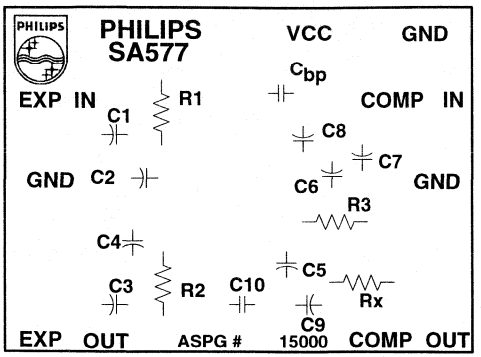
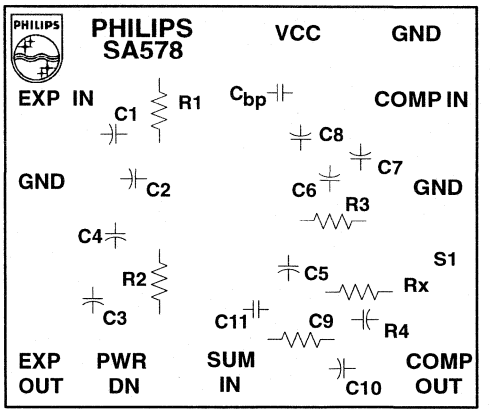


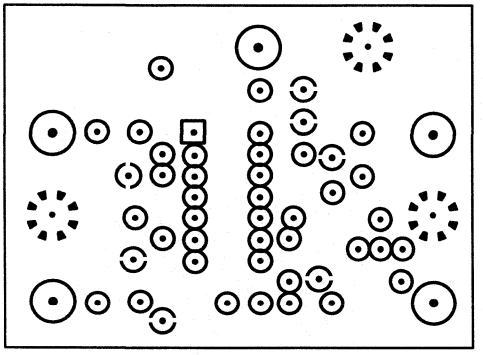
Figure 20 . Expandor Configuration for the Compressor Side



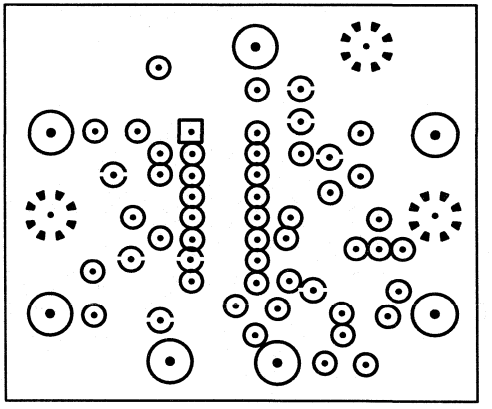
SA577 DIP Top Silk Screen



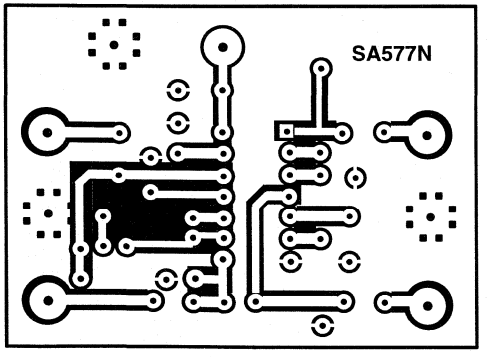
SA578 DIP Top Silk Screen



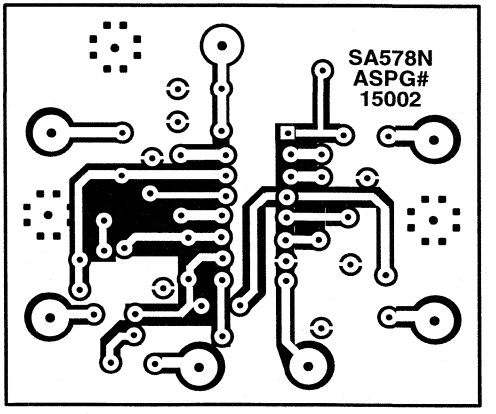
Top View



Top View



Bottom View

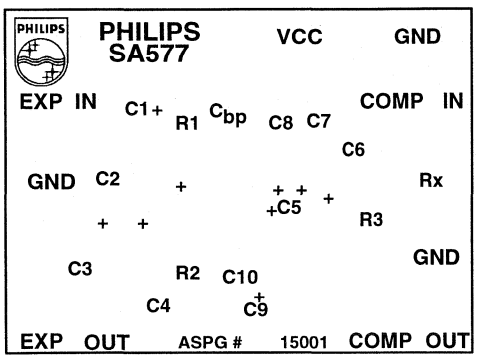


Bottom View

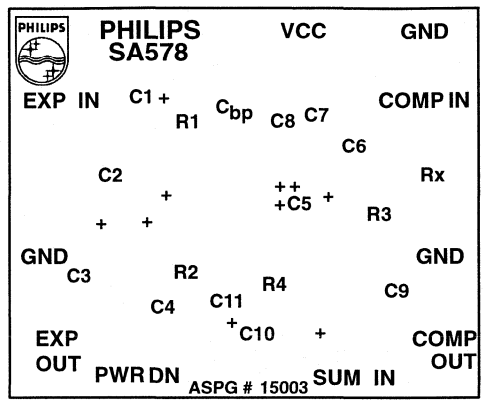
NOTE: C10 eliminated as of 11/30/94.

SR00772

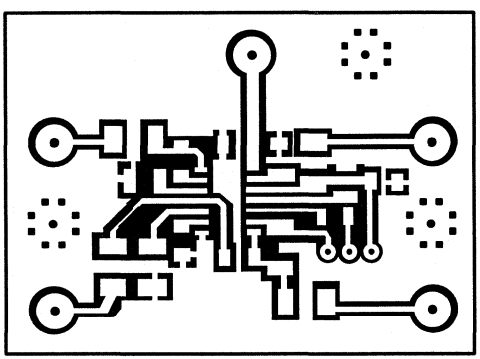
Figure 21 . SA577 and SA578 DIP Application Board Layout



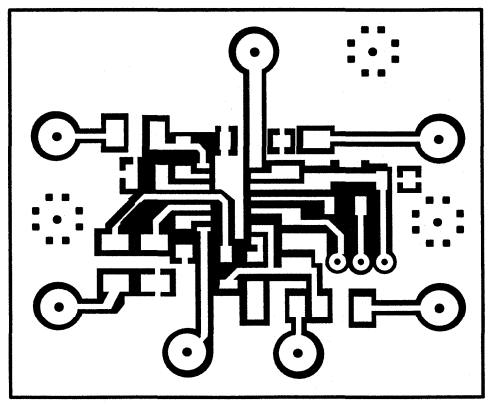
SA577 SO Top Silk Screen



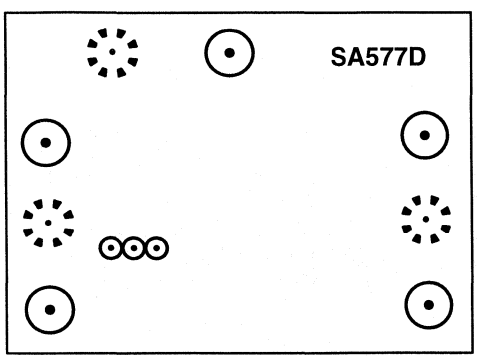
SA578 SO Top Silk Screen



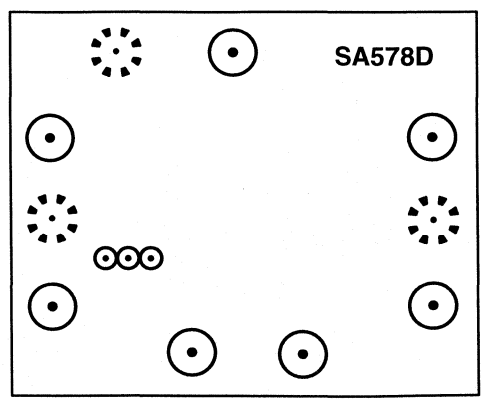
Top View



Top View



Bottom View



Bottom View

NOTE: C11 eliminated as of 11/30/94.

SR00773

Figure 22 . SA577 and SA578 SO Application Board Layout

Low voltage front-end circuits: SA601, SA620

AN1777

Author: M. B. Judson

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I. INTRODUCTION

The objectives of this application note are to highlight key features and distinguish key differences between the SA601 and SA620. The power, gain, noise figure, and third-order intercept point of the LNA and mixer will be characterized. A resonant circuit implementing a high loaded-Q μ-strip inductor and an extensive discussion of open-collector mixer outputs and how to match them will also be presented.

The SA601 and SA620 are products designed for high performance low power RF communication applications from 800 to 1200MHz. These chips offer the system designer an alternative to discrete front-end designs which characteristically introduce a great deal of end-product variation, require external biasing components, and require a substantial amount of LO drive. The SA601 and SA620 contain a low noise amplifier and mixer, offering an increase in manufacturability and a minimum of external biasing components due to integration. The LO drive requirements for active mixers are less stringent than passive mixers, thus minimizing LO isolation problems associated with high LO drive-levels. These chips also contain power down circuitry for turning off all or portions of the chip while not in use. This minimizes the average power consumed by the front-end circuitry. The SA620 features an internal VCO that eliminates additional cost and space needed for an external VCO. The SA601 and SA620 fit within a 20-pin surface mount plastic shrink small outline package (SSOP), thus saving a considerable amount of space.

II. KEY ATTRIBUTES OF THE SA601 AND SA620

The primary differences between the SA601 and SA620 are the LNA power down capability, the implementation of the mixer output circuitry, and the incorporation of an integrated VCO.

Table 1 below summarizes the attributes of both parts.

Table 1. Showing SA601 and SA602 Attributes

Product	Diff. Mixer Output	LNA Thru Mode	Mixer Power Down	Int. VCO and VCO Pwr Down
SA601	Yes	No	Yes	No
SA620	No	Yes	Yes	Yes

III. POWER CONSUMPTION

As mentioned above, the average power consumed by the front-end circuitry can be decreased by selectively turning off circuitry that is not in use. The supply current at a given voltage will decrease more than 3mA for each LNA, mixer, or VCO disabled. When the LNA is disabled on the SA620 it is replaced by a 9dB attenuator. This is useful for extending the dynamic range of the receiver when an overload condition exists. Tables 2 and 3 below contain averaged data taken on the SA601 and SA620 while in an application board environment.

Table 2. Showing SA601 Supply Current

V_{CC}	I_{CC} (mA)	I_{CC} (mA) Mixer Disabled
3.0	8.4	4.9
4.0	8.4	4.7
5.0	8.3	4.5

Table 3. Showing SA620 Supply Current

V_{CC}	I_{CC} (mA)	I_{CC} (mA) LNA Disabled	I_{CC} (mA) Mixer Disabled	I_{CC} (mA) VCO Disabled	I_{CC} (mA) Chip Fully Powered Down
3.0	11.4	8.0	8.1	8.2	1.4
4.0	11.6	8.5	8.0	8.2	1.6
5.0	11.7	8.9	8.0	8.2	1.7

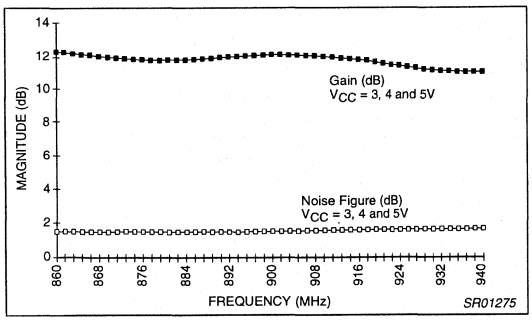


Figure 1. Noise Figure and Gain vs Frequency SA601 LNA

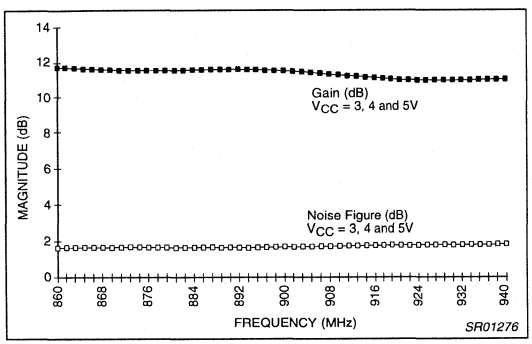


Figure 2. Noise Figure and Gain vs Frequency SA620 LNA

IV. LOW NOISE AMPLIFIERS

The performance of the SA601 and SA620 low noise amplifiers are virtually identical. You can expect an average gain of approximately 11.5 ±1.5dB and a noise figure of approximately 1.6 ±0.3dB. The LNA input and output networks are matched for optimum return loss, gain and best noise figure over the 869 - 894MHz band. They also perform well when utilized in the 902 - 928MHz band without any additional modification to the LNA matching networks. Figures 1 and 2 show gain and noise figure of a typical SA601 and SA620 LNA in the application board environment. Both the gain and the noise figure remain almost constant as V_{CC} is adjusted to 3, 4 and 5V. Therefore, only one curve is shown for clarity.

V. SA620 MIXER

The SA620 mixer is intended for operation with the integrated VCO and employs a single open-collector output structure. The open-collector output structure allows the designer to easily match any high impedance load for maximum power transfer with a minimum of external components. This eliminates the need for elaborate matching networks. The external mixer output circuitry also incorporates a network which distributes the power from the mixer output to two unequal loads. This enables the mixer output to be matched to a high impedance load such as a SAW bandpass filter (typically 1kΩ) while simultaneously providing a 50Ω test point that can be used for production diagnostics. The mixer output circuitry generates the majority of questions for those utilizing this part in their current applications, so some basic concepts regarding open-collector outputs are presented below, as well as a discussion of the network used to provide the 50Ω diagnostic point.

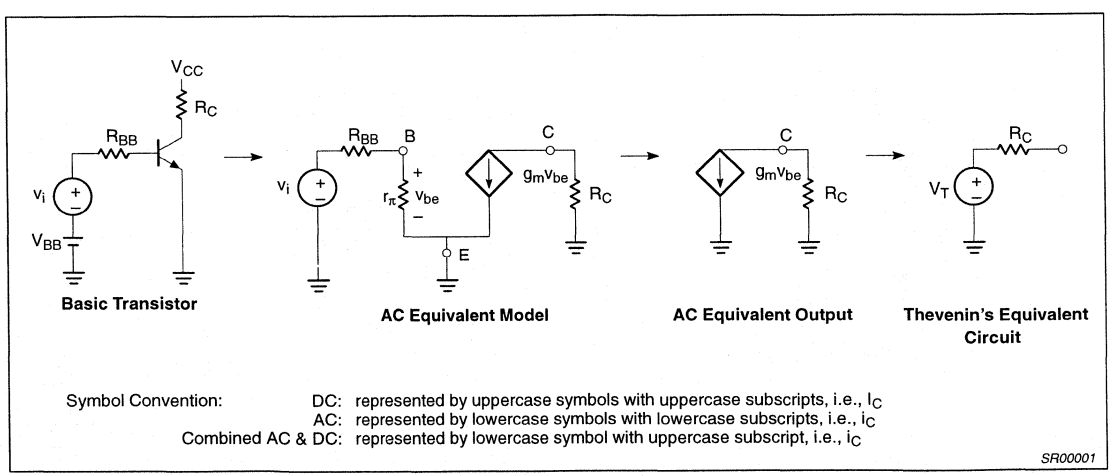


Figure 3. R_C as Source Resistor

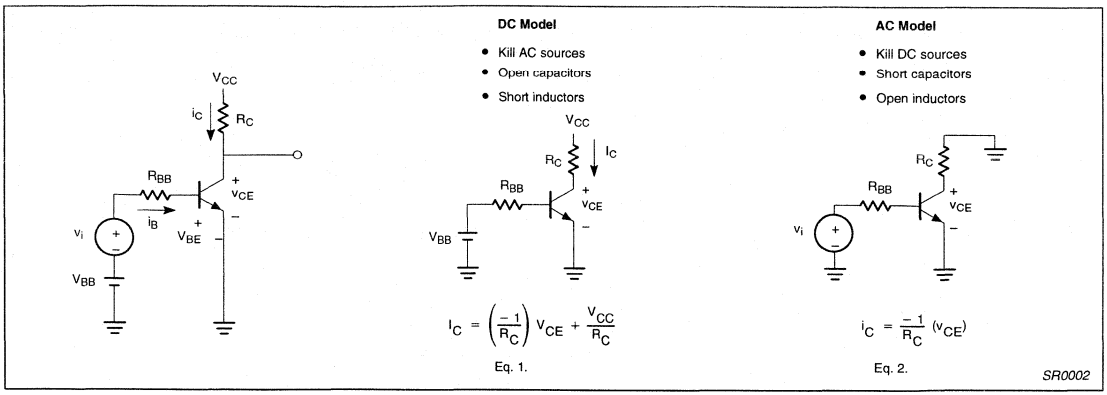


Figure 4. Basic Transistor Analysis

Open-Collector Output Basics [1, 2, 3, 6]

Why R_C Acts Like A Source Resistor

An open-collector output allows a designer the flexibility to choose the value of the R_C resistor. Choosing this resistor value not only sets the DC bias point of the device but also defines the source impedance value. Figure 3 shows the AC model of the transistor. Converting the output structure by applying a Norton and Thevenin transformation, one can conclude that R_C becomes the source resistance. Thus, by choosing R_C to be equal to the load, maximum power transfer will then occur.

Figure 4 shows an active transistor with a collector and base resistor. From basic transistor theory Equation 1 is generated and has the same form as the general equation for a straight line

$$y = mx + b$$

The slope of the DC load line is generated by the value of the collector resistor (m = -1/Rc) and is shown in Figure 5. For a given small signal base current, the collector current is shown by the dotted curve.

The intersection of the dotted curve and the DC load line is called the Quiescent point (Q-point) or DC bias determinant. The location of the Q-point is important because it determines where the transistor is operated; in the cutoff, active, or saturation regions. In most cases, the Q-point should be in the active region because this is where the transistor acts like an amplifier.

Figure 6 shows the ac collector-emitter voltage (V_{CE}) output swing with respect to an AC collector current (i_c). Collector current is determined by the AC voltage presented to the input transistor's base (v_i) because it effects the base current (i_b) which then effects i_c. This is how the v_i is amplified and seen at the output. Recall that this is with no external load (R_{LOAD}) present at the collector. Since no load is present, the AC load line has an identical slope as the DC load line as seen in equation 1 and 2 (m = -1/Rc).

Open-Collector With R_{LOAD}

A filter with some known input impedance is a typical load for the output of the transistor. For simplicity, we will assume a resistive load (R_{LOAD}) and neglect any reactance. Since a resistive load is used (see Figure 7), the AC output swing is measured at V_{OUT} or V_{CE}.

A DC blocking capacitor is used between the R_{LOAD} and the V_{CE} output to assure that the Q-point is not influenced by R_{LOAD}. It is also necessary to avoid passing DC to the load in applications where the load is a SAW filter. However, R_{LOAD} will affect the AC load line which is seen in Equation 4 in Figure 7. Notice that the V_{CE} voltage swing is reduced and thus, the V_{OUT} signal is reduced (see Figure 8).

Since the value of R_C and R_{LOAD} affects the AC load line slope, the value chosen is important. The higher the impedance of R_{LOAD} and Rc, the greater the AC output swing will be at the output, which means more conversion gain in a mixer. This is due to the slope getting flatter, thus allowing for more output swing.

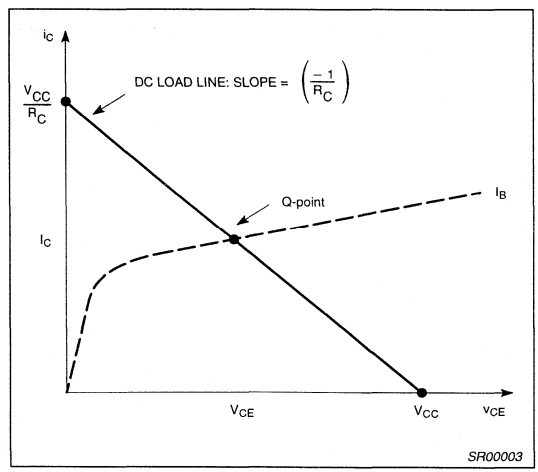


Figure 5. Load Line and Q-Point Graph

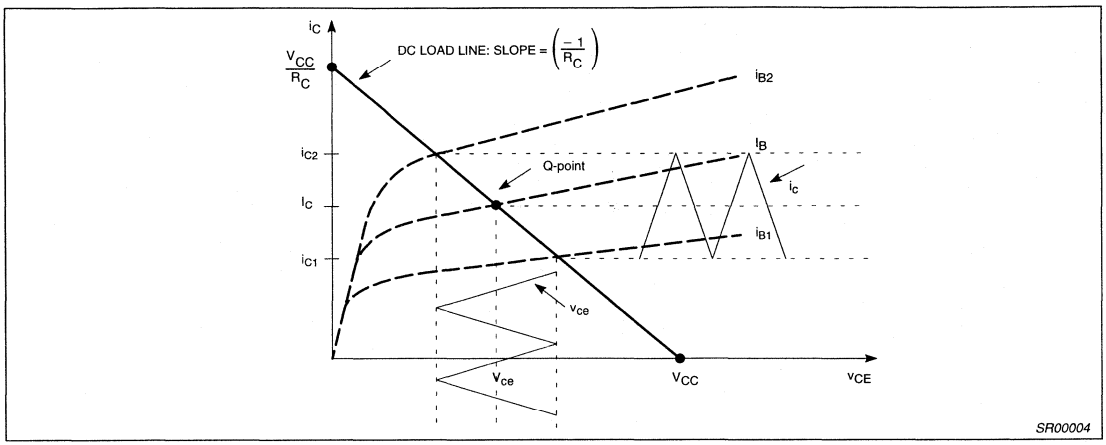


Figure 6. Graphical Analysis for the Circuitry in Figure 4

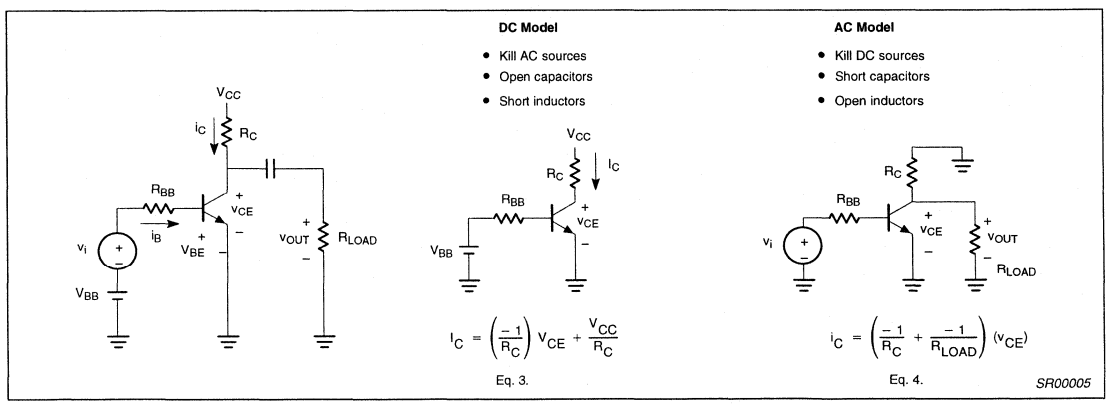


Figure 7. Basic Transistor Analysis with R_{LOAD}

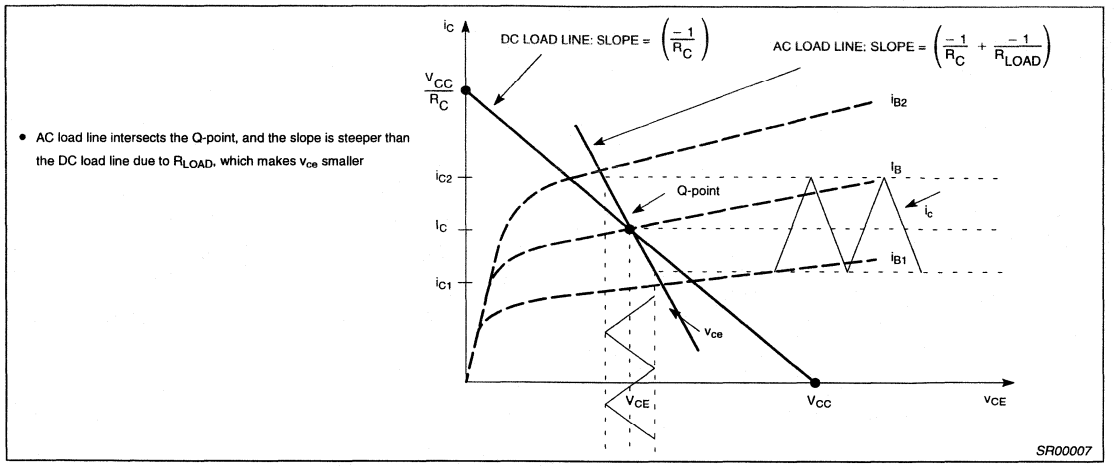


Figure 8. Graphical Analysis for the Circuitry in Figure 7

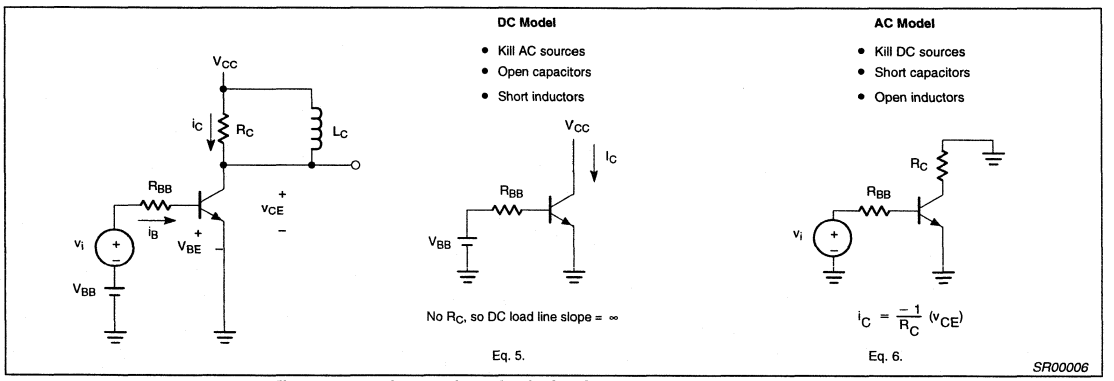


Figure 9. Basic Transistor Analysis with Inductor Added to Collector

Open-Collector With Inductor (L_C)

Adding an inductor in parallel with R_C can increase the AC output signal V_{CE}. Figure 9 shows the DC and AC analysis of this circuit configuration. In Equation 5, there is no R_C influence because the inductor acts like a short in the DC condition. This means the slope of the DC load line is infinite and causes the Q-point to be centered around V_{CC}, thus moving it to the right of the curve. The AC load line slope is set only by R_C because no load is present. Notice that it has the same AC load line slope as the first condition in Figure 4, Equation 2.

Referring to Figure 10, one might notice that the base current (AC and DC) curves spread open as V_{CE} increases. This is caused by a non-infinite early voltage (see Figure 11), which causes the collector current to be dependent on V_{CE}. Taking advantage of this non-ideal condition, the peak-to-peak AC output swing V_{CE}, can thereby be increased by moving the DC Q-point to the right due to the wider spreading between the curves corresponding to different base currents. Figure 12 combines Figures 6 and 10 to show the different AC output signals with different Q-points.

Looking at the AC output level, one might ask how the V_{CE} peak voltage can exceed the supply voltage V_{CC}. Recall that the inductor is an energy storing device (v=Ldi/dt). Therefore, total instantaneous voltage is V_{CC} plus the voltage contribution of the inductor.

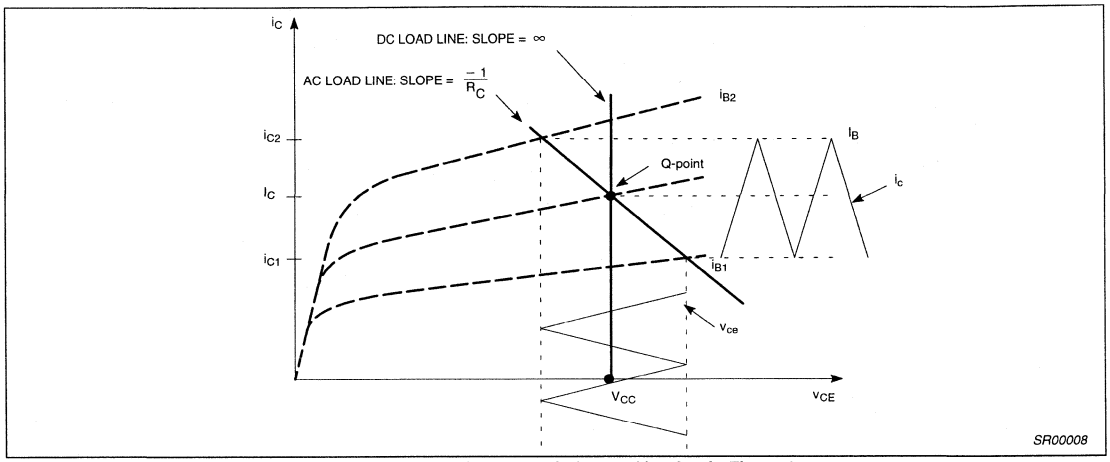


Figure 10. Graphical Analysis for the Circuitry in Figure 9

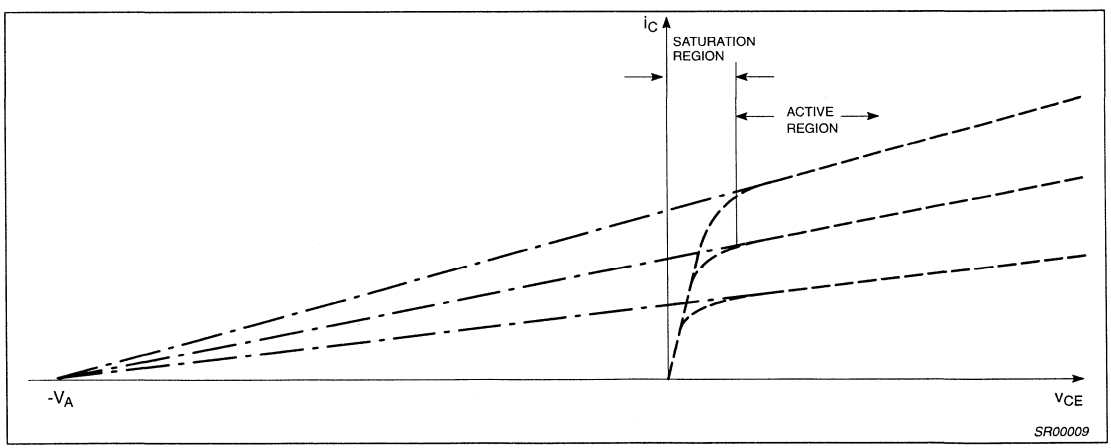


Figure 11. Graphical Representation of Early Voltage Effect

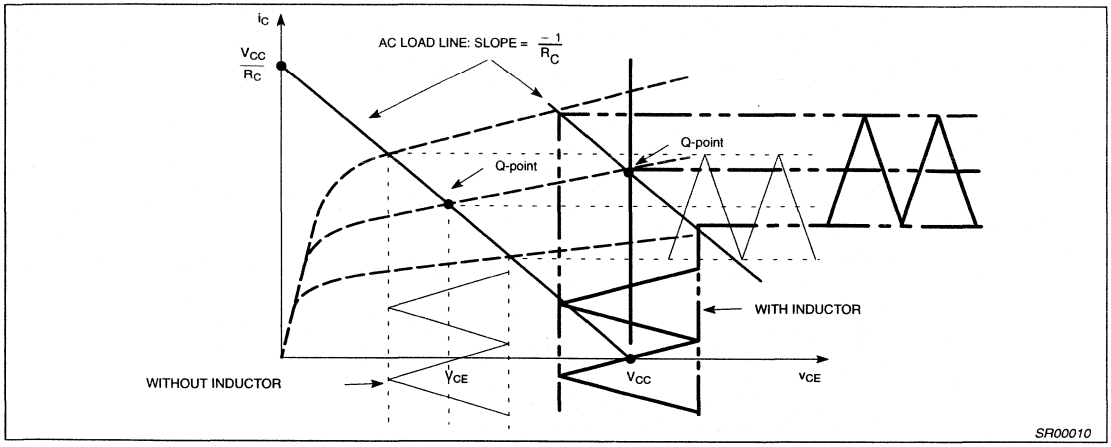


Figure 12. Comparison of Open-Collector Circuit With Inductor vs Without Inductor

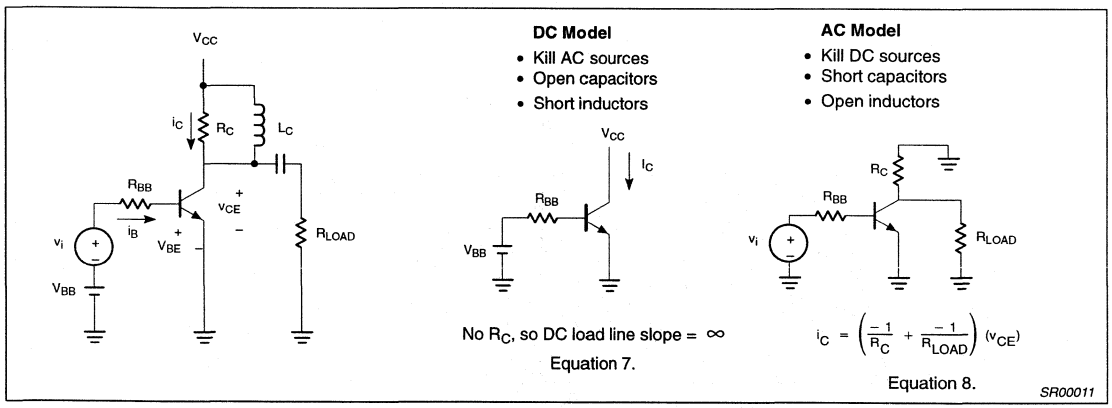


Figure 13. Basic Transistor Analysis with Inductor and R_{LOAD}

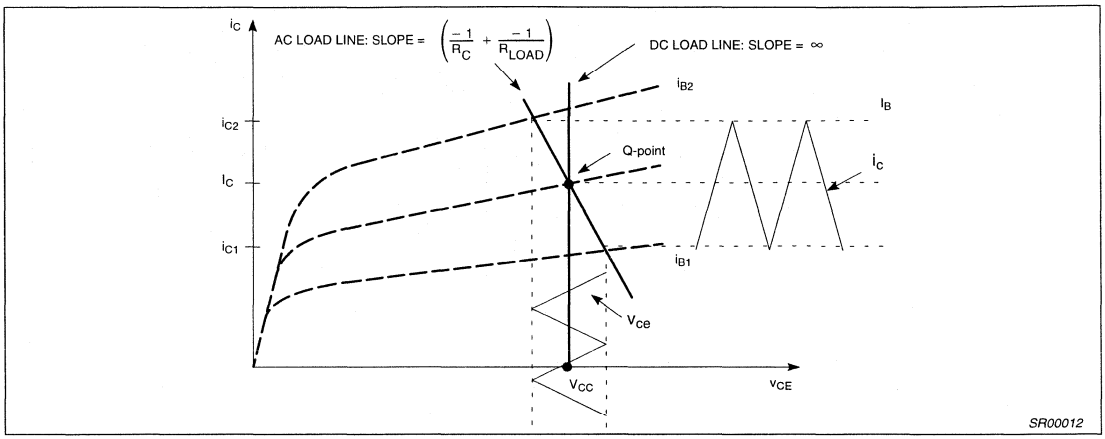


Figure 14. Graphical Analysis for the Circuitry in Figure 13

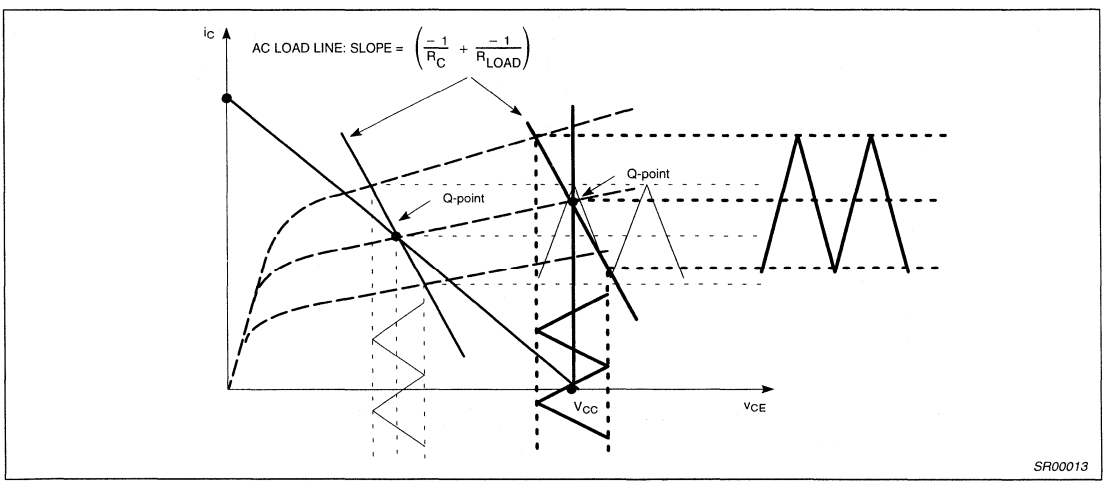


Figure 15. Comparison of Open-Collector R_{LOAD} Circuit With Inductor vs Without Inductor

Open-Collector With Inductor (L_C) and R_{LOAD}

Figure 13 shows the DC and AC analysis with the inductor and load resistor. Again, from the DC analysis, the inductor causes R_C to be non-existent so the DC load line is vertical. In the AC analysis, the AC load line slope is influenced by both R_C and R_{LOAD} resistors (see Equation 8). The AC load line slope is the same as the example of the open-collector without the inductor. Figure 14 shows the response for the open-collector with L_C and R_{LOAD}. Figure 15 combines Figures 8 and 14 showing the increase in AC output swing.

In conclusion, for the load line, R_C plays a role in setting up the bias determined Q-point as well as the AC source impedance. However, when an inductor is placed in parallel with R_C, a different Q-point is set and the AC source impedance is altered. Moving the Q-point takes advantage of the transistor's non-ideal i_c dependence on V_{CE} to get more signal output without having to change the base current. Since R_C is in parallel with R_{LOAD} in the AC condition, it influences the AC load line slope.

VI. FLEXIBLE MATCHING CIRCUIT [6]

A useful variation of the open collector matching concepts previously outlined provides the capability of delivering equal power to two unequal resistive loads. This allows the power delivered to the load to be measured indirectly at another test point in the circuit where the impedance can be arbitrarily defined. If this impedance is defined to be 50Ω, a spectrum analyzer can be easily placed directly into the circuit. This is an excellent troubleshooting technique and a valuable option to have available in high production environments.

Figure 16 shows the schematic for this flexible matching circuit. In this circuit, C_B functions only as a DC blocking capacitor and presents a negligible impedance at the frequency of interest. Recall from the previous open collector matching dicussions that, when R_C

is placed in parallel with an inductor, it has no effect on the Q-point, but does influence the slope of the AC load line as

$$\text{Slope} = \frac{-1}{R_C} + \frac{-1}{R_{LOAD}}.$$

The capacitor C_S functions not only as a DC blocking capacitor, but is also chosen such that the impedance presented by the combination of L, R_C and C_S is equal to R_{LOAD} for optimum power transfer. The analysis is done in the following manner. First, note that inductor L is connected to V_{CC} which is an effective AC ground. So, L can be redrawn to ground. Next, R_C and C_S are converted to their parallel equivalent values as shown in Figure 17.

The resulting parallel LCR circuit is shown in Figure 18. At resonance, the parallel L, C_P combination will be an effective open circuit leaving only R_P. R_P is then simply chosen to be equal to R_{LOAD}.

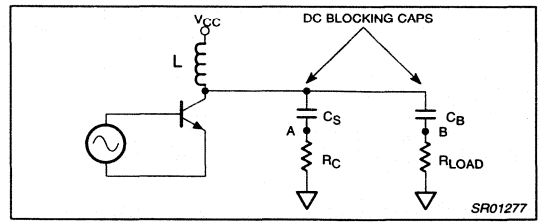


Figure 16. Flexible Matching Circuit

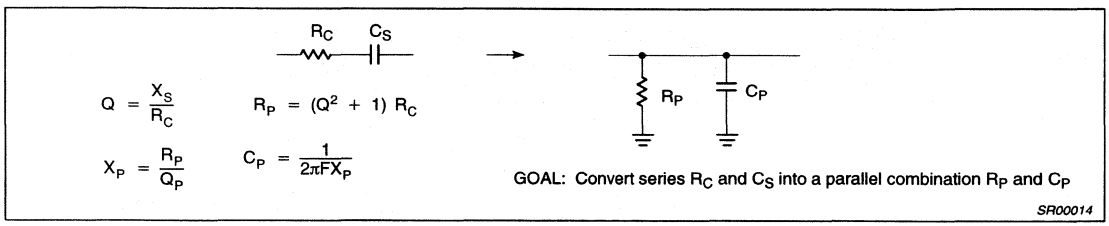


Figure 17. Converting from Series to Parallel Configuration

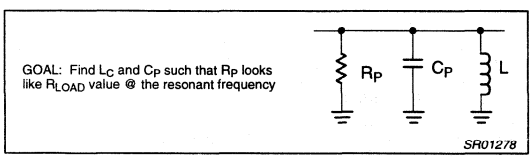


Figure 18. Converting from Series to Parallel Configuration

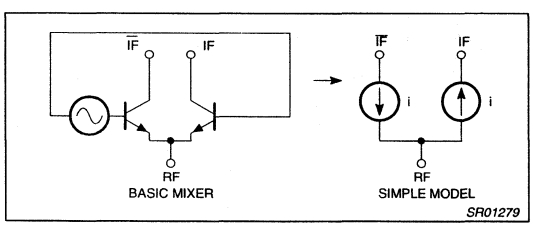


Figure 19. Circuit Model of Differential Open-Collector Output

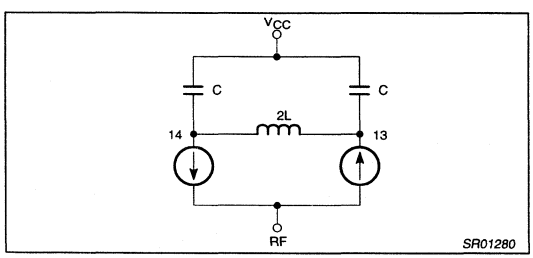


Figure 20. External current-combiner Circuit

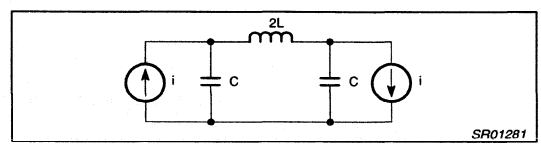


Figure 21. Ideal AC Equivalent Circuit

VII. SA601 MIXER [6]

The SA601 mixer is intended for operation with an external VCO and employs a differential output structure. The current wireless markets demand front-end solutions with low power, and high gain. The differential output offers higher gain than the conventional single-ended open-collector output without an increase in supply current. An equivalent model can be seen in Figure 19. A characteristic of the differential output is that the two output currents are 180° out of phase. This is why the mixer output is labeled IF and $\overline{IF}$.

The current-combiner circuit shown in Figure 20 consists of two capacitors and one inductor. The purpose of the current-combiner is to combine the currents such that they are in phase with one another. By aligning the currents in phase with one another, the output will have a larger AC output swing due to the increased signal current.

Figure 21 shows the ideal AC equivalent model. In the ideal case, it is assumed that all component Q's are high enough to be neglected and the output impedances of the current sources are also high enough to be neglected. By source transformation, the parallel capacitor and current source can be converted to a voltage source and a source capacitor. The inductor, 2L, can be split into two inductors where L becomes the new value (See Step 2 in Figure 22). Since two inductors of equal value in series will be twice that

value, we can split the one inductor into two series inductors each equal to L.

The series capacitor and inductor (L) at resonance will act like a short circuit. Therefore, for this analysis we can redraw the circuit, as seen in Figure 22, step 3.

In Step 4, the voltage source and series inductor (L) is converted back into a current source and parallel inductor. Source transformation, in this simple form, the values of L and C do not change. It is the value of the current and voltage source that changes.

Using Ohm's Law, i=v/z and v = i(1/jωc), while Z =jωL, the imaginary j causes the current to be negative at the resonant frequency specified in Equation 9 of Figure 22. Therefore, by switching the current's direction, the negative sign disappears and the current source is aligned in the same direction as the other one.

VIII. MATCHING THE OPEN-COLLECTOR DIFFERENTIAL OUTPUT

Figure 23 shows the current-combiner and the open-collector matching circuit. The collector current is increased and passes through the load resistor which allows for more AC output swing.

Since the SA601 has differential open-collector outputs, it is possible to implement both a current-combiner and a flexible matching circuit (see Figure 24).

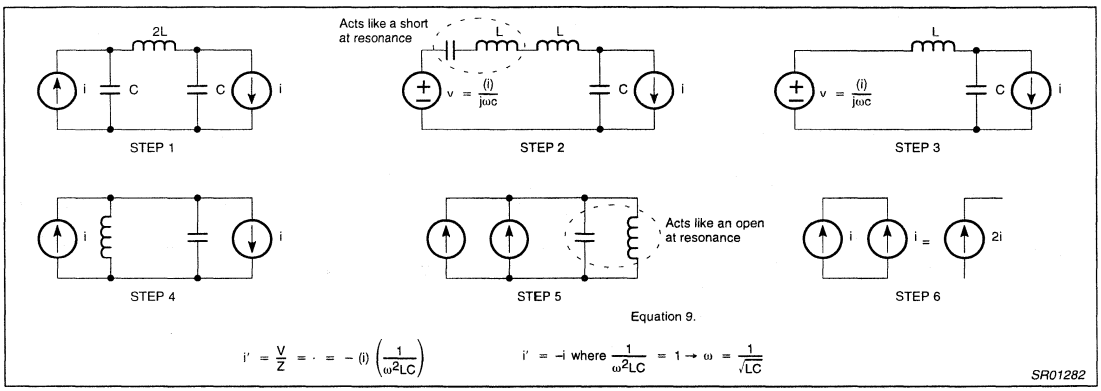


Figure 22. Equivalent Circuit Transformations at Resonance

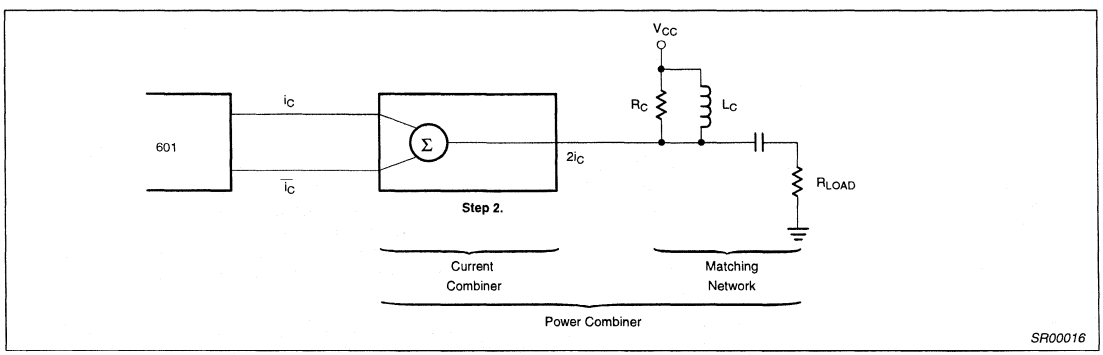


Figure 23. Power Combiner

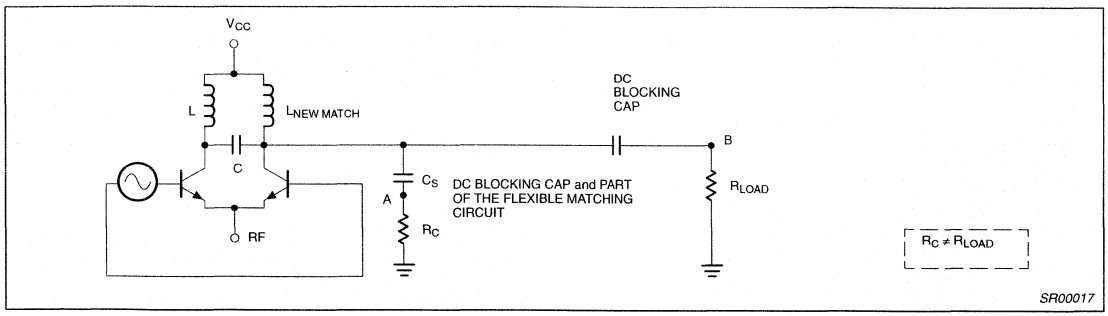


Figure 24. current-combiner with Flexible Matching Circuit

Understanding and implementing the mixer output match is most likely the biggest challenge for those using the SA601. As in most cases, there are many solutions to obtaining the required match for a given circuit. The method selected for the following examples was chosen in order to simply demonstrate some key principles involved in obtaining both high impedance and 50Ω matching while also maintaining some continuity to the previous discussions pertaining to the ideal current-combiner circuit. Each component in the current-combiner/matching circuit will be identified as well as the role each plays in obtaining the required matched condition. In addition, a general procedure for acquiring a good matching circuit along with Smith chart documentation will be provided.

The schematic of the mixer output circuitry utilized on the SA601 demo-board is reproduced here in Figure 25 for convenience.

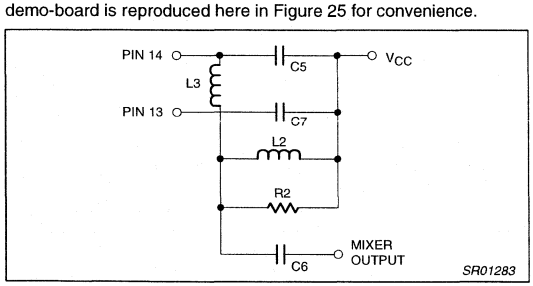


Figure 25. External Mixer Output Circuit

The following is a descriptive summary of the components comprising the external mixer output circuitry.

Inductor L_2
In order to minimize the deviation from the ideal current-combiner circuit, this inductor is chosen to be as large as possible. The inductor will then function only as a choke at the IF frequency and, therefore, should not interact with the current-combiner circuit or effect the matching conditions. This inductor is also necessary to provide the needed DC path from V_{CC} to Pins 13 and 14. In all the examples to follow, a 6.8µH inductor was used for L_2.

Capacitors C_5 and C_7
Also, in order to adhere to the analysis set forth in the ideal current-combiner discussions, these capacitors will be set equal to each other in the examples to follow. The main function of these capacitors is to define the resonant frequency of the current-combiner. They also play a secondary role in defining the output impedance.

Inductor L_3
This inductor also defines the resonant frequency of the current-combiner as well as the output impedance of the current-combiner at resonance.

Capacitor C_6
This capacitor is used to determine the output impedance for 50Ω matches only. For high impedance matches greater than or equal to 1kΩ this capacitor is not very effective. Thus, in this case it is usually replaced with a large capacitance value, adding almost no contribution to the match. A 1000pF is used in the high impedance examples that follow.

Resistor R_2
This resistor is used to simplify the high impedance matching process. In a 50Ω match, the series impedance presented by capacitor C_6 greatly simplifies the process of moving to the 50Ω point on the Smith chart. At high impedance, C_6 is no longer effective and it is often extremely difficult to obtain the proper match by varying just the components associated with the current-combiner circuit. A simple solution to this problem is to obtain the proper resonance condition at a higher impedance than the targeted impedance and then reduce it by placing a resistor of the correct value in parallel with it.

The best way to configure the mixer output circuitry for optimum gain is to optimize the return loss (S_{11}) for this port at the required IF. This, by itself, does not guarantee that optimum gain will occur at this frequency due to the phase relationships of the signals inside the current-combiner, but it is usually very close. The best tool available for this is a network analyzer.

Method of Achieving High Impedance Matching with a Network Analyzer

The network analyzer lends itself very nicely to obtaining 50Ω matches. However, for high impedance matches the Smith chart data will be far to the right of the chart and will be inaccurate, hard to read, and hard to interpret. If the network analyzer were normalized to the impedance value to which you want to match, the data would be in the center of the Smith chart and easy to interpret.

One method of doing this is to disconnect the 'A' port from an HP network analyzer and attach a high impedance probe to this port. Next take an SMA connector (or whatever connector type your analyzer uses) and solder two resistors each equal to the target impedance in the following manner: Solder one end of one of the resistors to the center lead of the connector and leave the other end open. This resistor will define the normalization on the network analyzer during calibration. Next, solder one end of the other resistor to the ground of the connector and leave the other end

open. This resistor will function as a dummy load during calibration. Connect this SMA connector to port '1' on the network analyzer. You are now ready to calibrate. Prior to initiating the open portion of the one-port calibration procedure, contact the open end of the resistor soldered to the center lead of the connector with the high impedance probe (see Figure 26). After this has been completed, contact ground on the connector with the high impedance probe prior to initiating the short portion of the one-port calibration procedure (see Figure 26). Then connect the two open ends of the resistors with solder. Prior to initiating the load portion of the one-port calibration procedure, contact the connection between the resistors with the high impedance probe (see Figure 27). The network analyzer should now be normalized to your target impedance. Thus, the optimum match will once again be in the center of the chart. When making connection to a circuit it is necessary to include a resistor of the same value used during the calibration between the center lead of the connector and its connection to the circuit. Impedance measurements are taken by contacting the high impedance probe at the end of this resistor nearest the circuit (see Figure 28).

Another tip concerning the calibration of the network analyzer should be mentioned. It is often useful to be able to look at a Smith chart over more than one frequency range. A wide frequency range is useful initially when your results are far off the target. Then the narrower range is useful for fine tuning your results. So, it is recommended that you calibrate in both frequency ranges and save the settings in the internal registers of the network analyzer if possible.

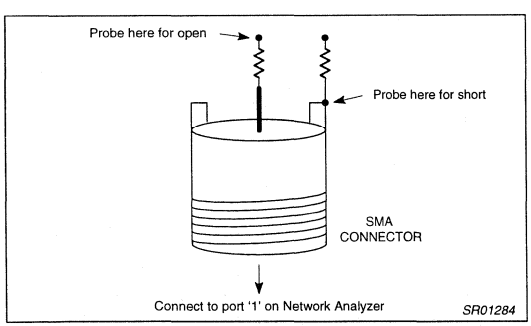


Figure 26. Open- and Short-circuit Calibration Locations

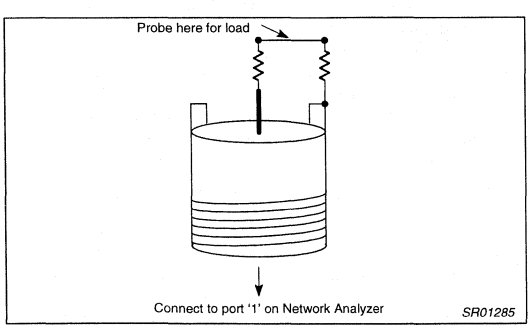


Figure 27. Load Impedance Calibration Location

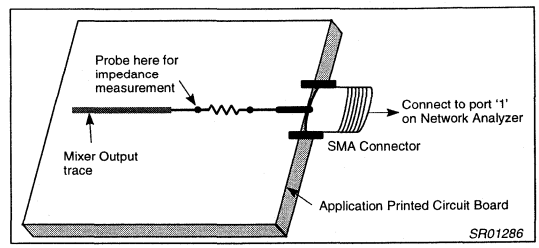


Figure 28. PCB Impedance Measurement Configuration

Non-Ideal Current-Combiner Ckt Considerations

Before we go through some actual impedance matching examples, some key differences between the ideal current-combiner circuit presented earlier and a non-ideal circuit which takes into account the finite Q of inductor L_3 as well as the output impedances of the current sources should be discussed. Through a series of Thevenin/Norton conversions and Series/Parallel equivalent impedance conversions similar to the analysis of the ideal circuit, the mixer output circuit can be modeled by the circuit shown in Figure 29.

The two main things to note in this circuit are the presence of the shunt resistors, R_O and R_Q, and that the current-combiner circuit looks like a simple parallel LRC circuit to capacitor C_6.

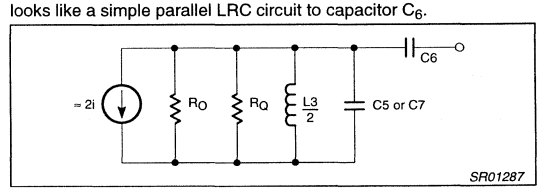


Figure 29. Non-ideal Mixer Output Equivalent Circuit

The significance of the resistors is their role in determining the output impedance of the overall circuit. R_Q is smaller in value than R_O which is the relatively high impedance of the open-collector outputs. Thus, because they are in parallel, R_Q defines the output impedance of the current-combiner circuit at resonance. The value of R_Q is a function of frequency, the component Q of inductor L_3, and the inductance value of inductor L_3. We do not have direct control over component Q or frequency, so the value of R_Q is adjusted by simply changing the value of inductor L_3. A more detailed explanation of this will be shown in the examples to follow.

It is not intuitively obvious why the matching portion of the mixer output circuitry used to obtain the 50Ω matches is composed of a single series capacitance. Many customers using the SA601 have asked why this works because it does not seem to adhere to basic two element matching concepts. To answer this, let's first take a quick look at the general parallel LC circuit shown in Figure 30. This circuit will resonate according to the simple resonance calculation

$$\omega = \frac{1}{\sqrt{LC}}$$

If the capacitor of this circuit is cut in half and the inductor is equivalently represented by two parallel inductors, the circuit in Figure 31 results. At the original resonant frequency $\omega = \frac{1}{\sqrt{LC}}$, the capacitor and one of the inductors will resonate $\omega = [(0.5C)\ (2L)]^{-\frac{1}{2}} = (LC)^{-\frac{1}{2}}$. What is left over is a shunt inductance of 2L presented to the output. Thus, the general

principle is that by decreasing the capacitance of a parallel LC circuit, you will present a shunt inductance to the output of that circuit at the same frequency. This concept when applied to the circuit in Figure 29 offers an explanation of where the missing shunt inductance element is coming from. If capacitors C_5 and C_7 are decreased, this will present a shunt inductance to capacitor C_6. Thus, two element matching concepts would still apply to this circuit. How much inductance is referred to C_6, and what value of C_6 it takes to obtain the matching conditions, is difficult to predict. So, we will rely on the network analyzer to point us in the right direction.

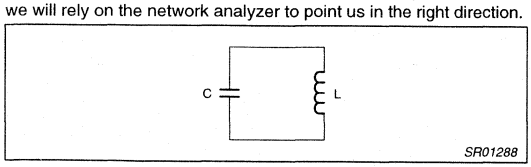


Figure 30. Parallel L_C Network

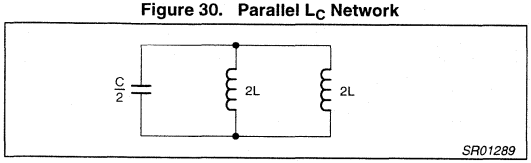


Figure 31. Parallel L_C Network with Decreased Capacitance

One of the most frustrating parts of matching on the network analyzer is it often does not give you very much information until you are at least "in the ball park" of the component values required. The first example will purposely begin with component values to create this condition to give an idea of what might initially be encountered. Additionally, Table 4 at the end of this section contains values for the components required to obtain optimum gain from the mixer at IF frequencies of 45, 83 and 110MHz at both a high impedance of 1kΩ and a low impedance of 50Ω. Using this table you should be able to obtain a good guess for the initial values for your particular application.

IX. MATCHING EXAMPLES

A procedure for acquiring a good high impedance matching circuit for providing optimum gain from the mixer output can be summarized as follows:

1. Normalize the network analyzer to the impedance of interest.
2. Set inductor L_2 to be a large inductance value.
3. Choose "ball park" values for the initial component values based on the simple resonance calculation and /or the tabulated data provided in Table 4.
4. Adjust $C_{5,7}$ to obtain the required match.
5. If the output impedance at resonance is above its target and resonance occurs at the targeted IF, the required match can be obtained with the appropriate value for R_2.
6. If the resonant frequency is above the target IF and the output impedance at resonance is below its target, change inductor L_3 to a higher value and return to step 4.
7. If the resonant frequency is below the target IF and the output impedance at resonance is above its target, change inductor L_3 to a lower value and return to step 4.
8. Design a matching circuit to bring the impedance back down to 50Ω.
9. Make final fine tuning adjustments to $C_{5,7}$ based on the frequency response as observed on a spectrum analyzer.

A procedure for acquiring a good 50Ω impedance matching circuit for providing optimum gain from the mixer output can be summarized as follows:

1. Set inductor L_2 to be a large inductance value.
2. Choose "ball park" values for the initial component values based on the simple resonance calculation and/or the tabulated data provided.
3. If the output impedance at resonance is greater than its target, increase capacitor C_6 until the curve on the Smith chart passes through the center of the chart.
4. If the output impedance at resonance is less than its target, decrease capacitor C_6 until the curve on the Smith chart passes through the center of the chart.
5. If the resonant frequency is greater than the target IF, increase the values of C_5 and C_6 until resonance occurs at the target IF.
6. If the resonant frequency is less than the target IF, decrease the values of C_5 and C_6 until resonance occurs at the target IF.
7. Make final fine tuning adjustments to $C_{5,7}$ based on the frequency response as observed on a spectrum analyzer.

83MHz, 1 kΩ Match

The objective of the first matching circuit we will look at is intended to provide a 1kΩ match at 83MHz. It has inductance values L_2 = 6.8μH and L_3 = 270nH. (These will be the values for these inductors in all the examples unless stated otherwise.) This match is a high impedance 1kΩ match so capacitance C_6 was set to 1000 pF. The simple resonant calculation

$$\omega = [(0.5CL)]^{-\frac{1}{2}} = [(0.5)\ (270nH)\ (C)]^{-\frac{1}{2}} = 2\pi\ (83MHz)$$

suggests that $C_{5,7}$ should be approximately 27pF. The actual value needed to optimize the gain is always less than the value predicted by this equation. Figure 32 shows what an unfavorable Smith Chart might look like when you go in the wrong direction. In this example $C_{5,7}$ was set to 33pF. The chart shows resonance does not occur anywhere between 75 and 95MHz. If you were to continue this curve, it would eventually hit the real axis at a much lower frequency. According to the simple resonance calculation this suggests that our capacitance value is too large. As $C_{5,7}$ is decreased, the plot on the Smith chart starts to resemble a constant admittance circle. Figure 33 shows that a $C_{5,7}$ value of 23pF yields a more favorable curve where resonance occurs at 83MHz as desired. The only problem is the impedance at resonance is not 1kΩ as desired. The Smith chart in Figure 33 has been normalized to 1kΩ. The real part coordinate of 61.984Ω. shown on the Smith chart must be converted in the following manner:

Z_O = (61.984/50) (1kΩ) = 1.24kΩ.

We could at this point choose another value for inductor L_3 and then again find the right value for $C_{5,7}$ to acquire resonance. However, we will take this opportunity to demonstrate how resistor R_2 might be used. The needed shunt resistance R_2 can be calculated from the simple formula for combining parallel resistances.

$$R_2 = \frac{(Z_O)\ (Z_{TARGET})}{(Z_O - Z_{TARGET})} = \frac{(1.24)\ (1)}{(1.24 - 1)} = 5.17k\Omega$$

Figures 34 and 35 show the resulting output match when a 5kΩ resistor is used for R_2.

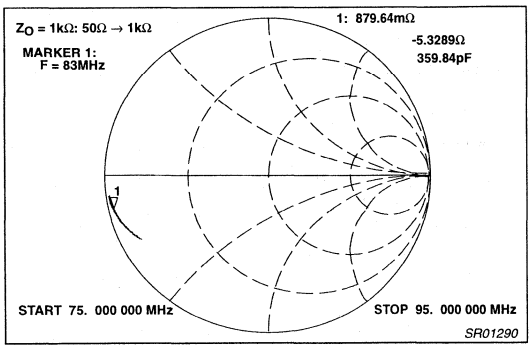


Figure 32. Smith Chart S_{11}: Showing Poor Initial Conditions

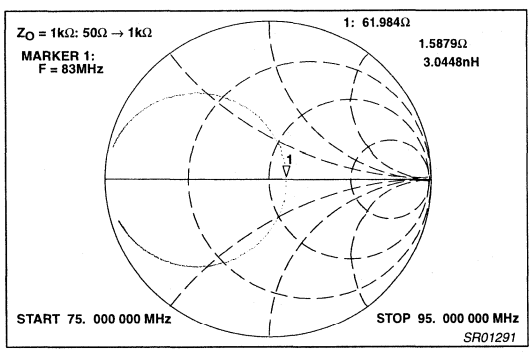


Figure 33. Smith Chart S_{11}: Showing Targeted Resonant Frequency, But Output Impedance Is Too High

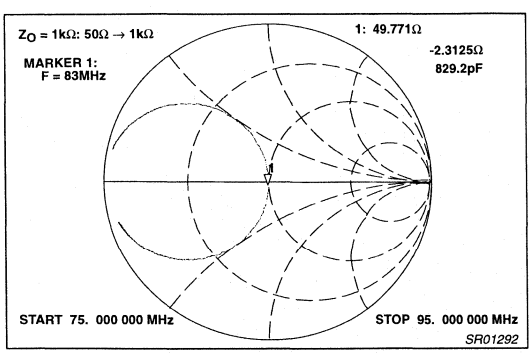


Figure 34. Smith Chart S_{11}: Showing Targeted Resonant Frequency And Output Impedance

In order to verify the high impedance match in the absence of a system in which to test it, a wideband matching circuit was designed to convert the high impedance 1kΩ match back down to 50Ω where it can then be terminated into a standard 50Ω test equipment port. Figures 36, 37 and 38 show the design of such a circuit. A detailed discussion of the design of this type of circuit can be found in [1]. Figure 39 shows the frequency response of the mixer output as the LO was varied to change the IF output. The envelope of this response has been added for clarity. The RF input signal to the mixer was -30dBm. So, the plot shows a very favorable gain of approximately 10.6dB at 81.75MHz. At 83MHz, which is the intended IF, the gain is only about 1dB lower.

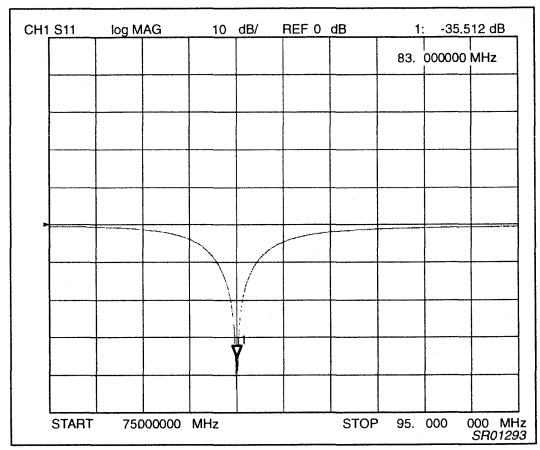


Figure 35. S_{11} Reflection at Mixer Output

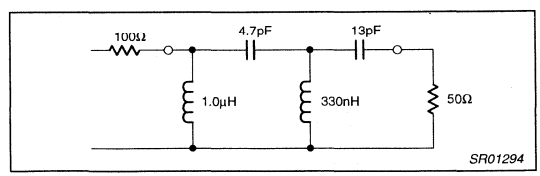


Figure 36. Wideband 1kΩ to 50Ω Matching Network

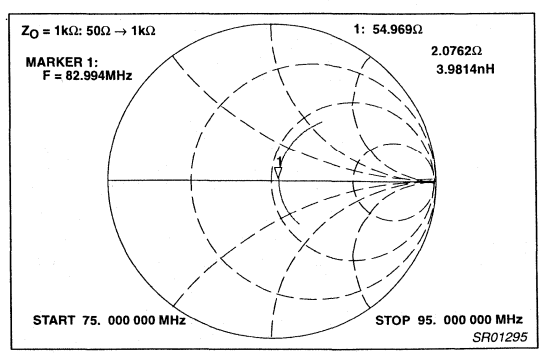


Figure 37. Smith Chart S_{11}: Showing Wideband Matching of Circuit in Figure 36

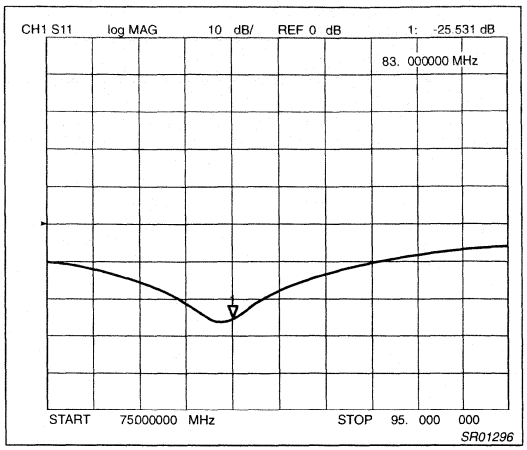


Figure 38. Smith Chart S_{11}: Showing Wideband Matching of Circuit in Figure 36

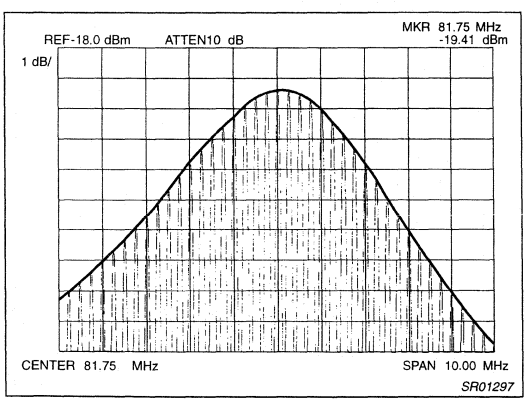


Figure 39. Showing the Frequency Response of the Mixer Output

45MHz, 1 kΩ Match

The next example is designed to show how to determine when inductor L3 is too low or too high to enable you to acquire the proper matching conditions. The objective is to provide a 1kΩ match at the much lower IF of 45MHz. Before we can determine if we have the wrong inductance value for L_3, we must first understand what effect adjusting C_5 and C_7 has on the circuit. The simple resonance calculation suggests that a decrease in $C_{5,7}$ should increase the frequency at which resonance occurs. This also causes a change in the output impedance at resonance. When $C_{5,7}$ is decreased the output impedance at the new higher resonant frequency will also be higher. As $C_{5,7}$ is adjusted the resonant frequency and the output impedance at resonance will change in the same direction. In other words, both will increase as $C_{5,7}$ is decreased or both will decrease as $C_{5,7}$ is increased. This means that if a condition exists where the resonant frequency is greater than the target IF and the impedance at resonance is below its target, the inductance value used for inductor L_3 is too small. Conversely, if the frequency is less than the target IF and the impedance at resonance is greater than its target, the inductance value used for L_3 is too large.

To demonstrate these concepts, inductor L_3 was chosen to be larger than usual (L_3 = 750nH) and $C_{5,7}$ was also chosen to be much larger than usual ($C_{5,7}$ = 82pF). Capacitor C_6 was again set to 1000pF making it negligible during high impedance matching. Again, it should be noted that the following Smith charts have been normalized to 1kΩ. Figure 40 shows that the component values listed above yield a 1kΩ output impedance at a resonant frequency of just 28MHz instead of the 45MHz target IF. In an effort to increase the resonant frequency $C_{5,7}$ was decreased to 33pF. Figure 41 shows that the resonant frequency is close but below the target IF and the impedance is well above 1kΩ. According to the discussions above, this suggests that inductor L3 is too large. Figure 42 shows the results when inductor L3 is decreased to 620nH. This chart shows that both the resonant frequency and the impedance at resonance are greater than their targeted values. This indicates that there is still a chance that the match can be made with some further adjustment of $C_{5,7}$. $C_{5,7}$ was increased to 39pF to lower the resonant frequency. Figure 43 shows that when this was done the condition that suggests that inductor L_3 is too large still exists.

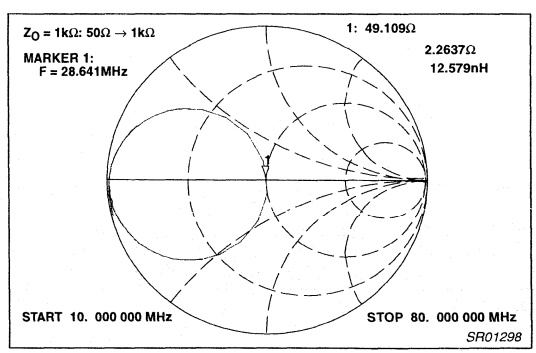


Figure 40. Smith Chart S_{11}: Showing Resonant Frequency Well Below 45MHz Target

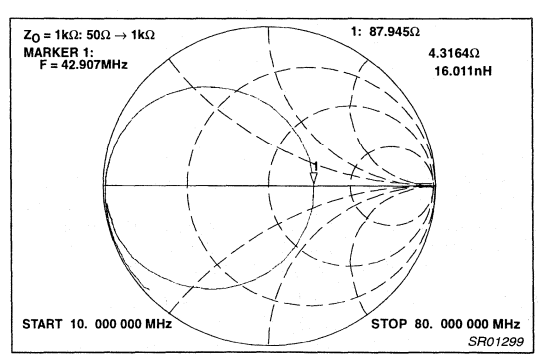


Figure 41. Smith Chart S_{11}: Showing Output Impedance Well Above the 1kΩ Target

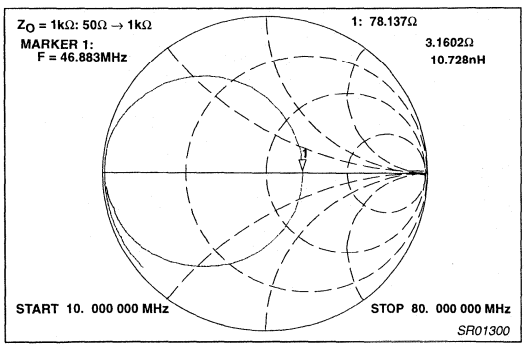


Figure 42. Smith Chart S_{11} , L_3 = 620nH: Showing the Resonant Frequency and the Output Impedance are Both Above the 45MHz, 1kΩ Target Values

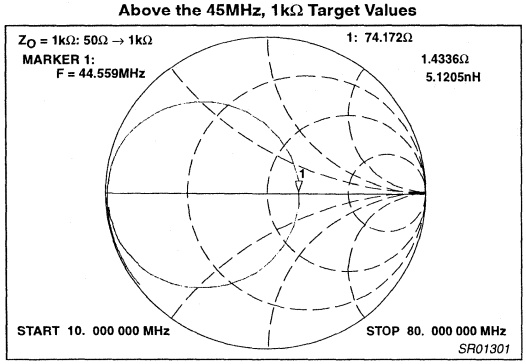


Figure 43. Smith Chart S_{11} , L_3 = 620nH: Showing the Resonant Frequency Below 45MHz Target and Output Impedance Above 1kΩ Target Values

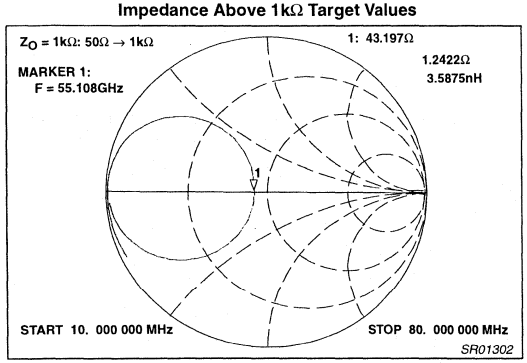


Figure 44. Smith Chart S_{11} , L_3 = 270nH: Showing the Resonant Frequency Above 45MHz Target and the Output Impedance Less than 1kΩ Target Values

Next, in order to demonstrate the other condition, inductance L_3 was changed to 270nH and $C_{5,7}$ was changed to 56pF. Figure 44 shows that the resonant frequency is greater than the target IF and the output impedance at resonance is less than 1kΩ. According to the discussions above, this is the condition which suggests that inductance L_3 is too small. So, inductance L_3 was then increased to 390nH. Figure 45 shows that the 390nH inductance yields a resonant frequency and an output impedance at resonance that are both slightly above their targets. At this point you are close enough to use another wideband matching circuit for dropping the 1kΩ impedance to 50Ω allowing you to check the frequency response directly. It was determined that changing $C_{5,7}$ from 56pF to 62pF yielded optimum gain at exactly the target IF. Figure 46 shows this gain to be approximately 10dB.

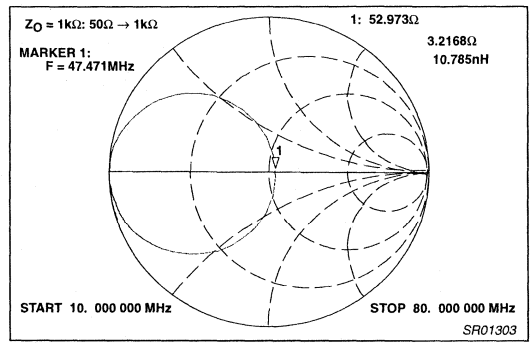


Figure 45. Smith Chart S_{11} , L_3 = 390nH

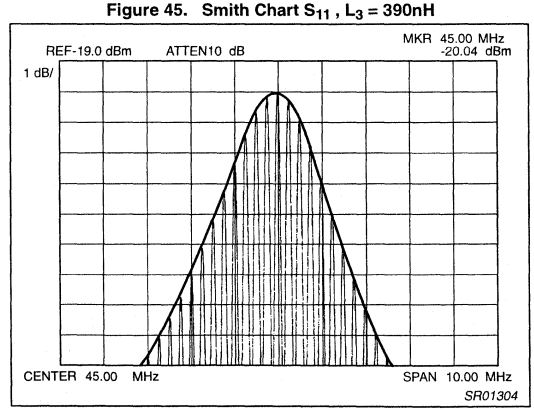


Figure 46. Frequency Response of the Mixer Output

110.592MHz, 50Ω Match

The next example will demonstrate how to obtain a 50Ω match. There are a couple of things to note concerning matching at a higher IF. The first is to expect an increase in the general sensitivity of the matching conditions with relatively small component variations. Secondly, the difference in frequency between the point of optimum gain and the point where the return loss (S_{11}) is minimized greatly increases when matching at a higher IF. To demonstrate these things the objective of the following example will be to provide a 50Ω match at 110.592MHz, which is a relatively high 1st IF.

The initial component values for this matching circuit (see Figure 25 are 6.8uH and 270nH for inductances L_2 and L_3, respectively. Capacitors C_5, C_6 and C_7 were all set to 10pF. It should be noted that C_6 is no longer set at 1000pF and plays a major role in determining the required match at 50Ω as we will see. Figure 47 shows the results of the initial component values. The Smith chart indicates that the resonance frequency is much too low and the impedance at resonance is too high. In our previous high

impedance matching discussions this meant that the inductor L_3 was too Large. In 50Ω matching this is no longer the case. Due to the lower impedance matching condition, the output impedance at resonance can now be significantly altered by varying the series capacitance element C_6. As mentioned previously, the matching circuit is much more sensitive to component variations at a higher IF. Figure 48 shows a small change in $C_{5,7}$ from 10pF to 4.7pF caused the resonant frequency to shift from well above the target IF to well below the target IF with very little change in the output impedance at resonance.

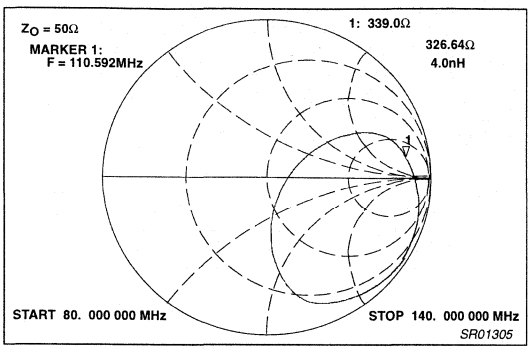


Figure 47. Smith Chart S_{11}: Showing Initial Component Results

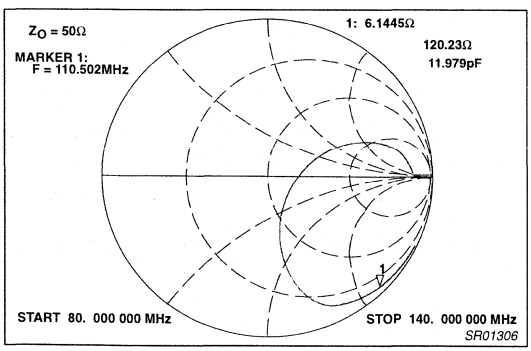


Figure 48. Smith Chart S_{11}: Showing Sensitivity to Small Changes in $C_{5,7}$

These observations suggest a general method of attack for obtaining the output impedance at 50Ω. When the series capacitance element C_6 is increased/decreased it will cause the somewhat circular curve on the Smith chart to increase/decrease in diameter. An effective method for obtaining the required match would be to adjust C_6 such that this curve passes through the center of the Smith chart and then make the necessary adjustments to $C_{5,7}$ to set the resonant frequency at the target IF. Looking at Figure 48 again, we see that the output impedance at resonance is too high. We should be able to decrease this by increasing the series capacitance element C6. In addition, from Figures 47 and 48 we know that the correct value for $C_{5,7}$ to obtain resonance at 110.592MHz is between 4.7pF and 10pF. So, we will increase C_6 to 12pF and set $C_{5,7}$ to 6pF and see what happens. Figure 49 shows the output impedance at resonance is very close to the target but the resonant frequency is still a bit too high. Figures 50 and 51 show that by adding 1pF to $C_{5,7}$ the required match is obtained. An additional matching network is not needed to evaluate the circuit because we are already at 50Ω.

In previous discussions, it was mentioned that the frequency at which the return loss is obtained does not guarantee optimum gain at this same frequency due to the phase relationships of the signals within the current-combiner circuitry. Figure 52 shows that approximately 12dB of gain is obtained but at a frequency of 115MHz, which is approximately 5MHz away from the targeted IF. To correct this we simply adjusted $C_{5,7}$ to 8.5pF to obtain a similar condition 5MHz lower than the previous result as shown in Figures 53, 54 and 55.

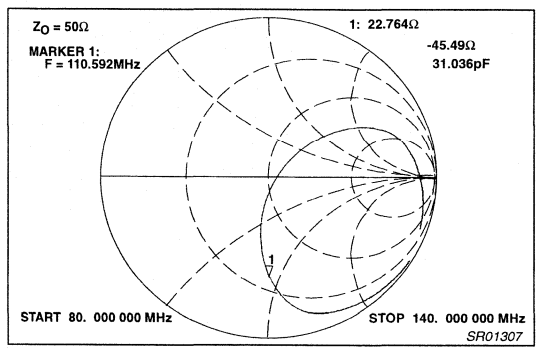


Figure 49. Smith Chart S_{11}: Showing Results of Adjustment to Capacitor $C_{5,6,7}$

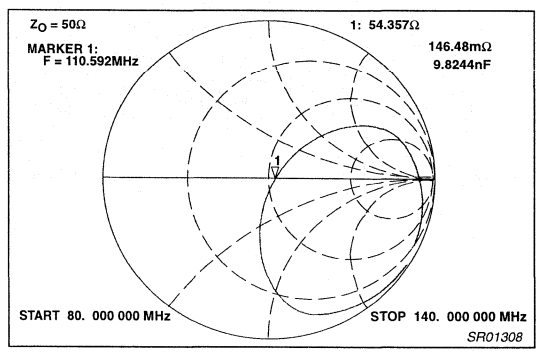


Figure 50. Smith Chart S_{11}: Showing Final 110.592MHz, 50Ω Results

Table 4. Mixer Output Component Values

	50Ω Match			1kΩ Match		
	MHz			MHz		
	45	83	110	45	83	110
L_1	6.8µH			6.8µH		
L_3	270nH			390nH	270nH	
$C_{3,7}$	80pF	18pF	8.5pF	62pF	22pF	10pF
C_6	22pF	15pF	12pF	1000pF		
R_2	———			—	5k	—

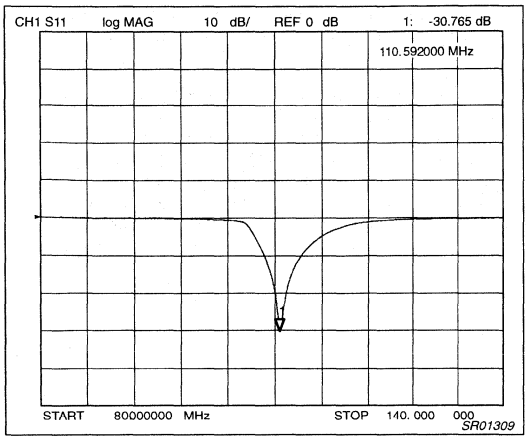


Figure 51. Final 110.592MHz, 50Ω Results

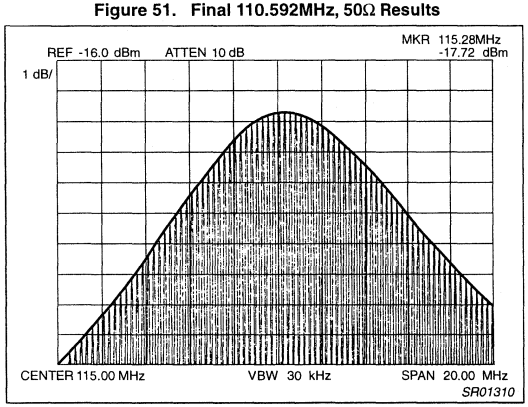


Figure 52. Mixer Output Freq. Resp. Peak is 5MHz Too High

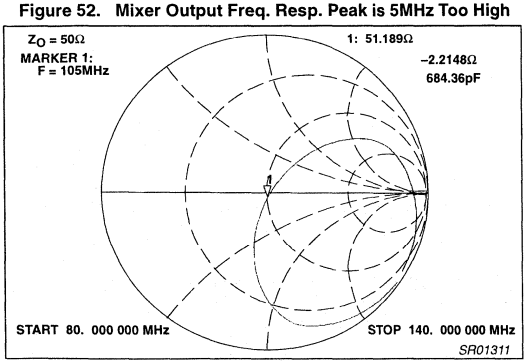


Figure 53. Smith Chart S_{11}: Showing Match With $C_{5,7}$ = 8.5pF

SA601 $IP3_{IN}$ Considerations

It should be noted that it is often necessary to give up some mixer gain of the device in order to obtain acceptable IP3in performance. The previous examples and procedures demonstrated how to optimize the gain. To meet the IP3in specifications of your particular application, it may be necessary to make some changes. The demoboard schematic for the SA601 in Figure 67 shows these changes. One difference between the previous discussions and this schematic is that C_5 and C_7 are not of equal value. It has been found that loading the differential output in an asymmetrical fashion by making C_5 less than C_7 is beneficial to $IP3_{IN}$ performance. So, your frequency adjustments would then be made by keeping C_7 constant and varying C_5. Also, inductor L_2 can no longer be chosen arbitrarily large. It must be chosen such that a high impedance parallel resonance condition occurs with C_7 at the frequency of interest. Resistance R_2 can then be used to obtain the required high impedance match. C_6 is used to acquire the 50Ω match exactly as before. The IP3in and gain performance for this configuration at 83MHz is shown in Figures 56 and 57. Notice the gain is approximately 8dB which is approximately 2dB less than that obtained in the previous examples. This was the trade-off for obtaining the better $IP3_{IN}$ performance (see Figure 57).

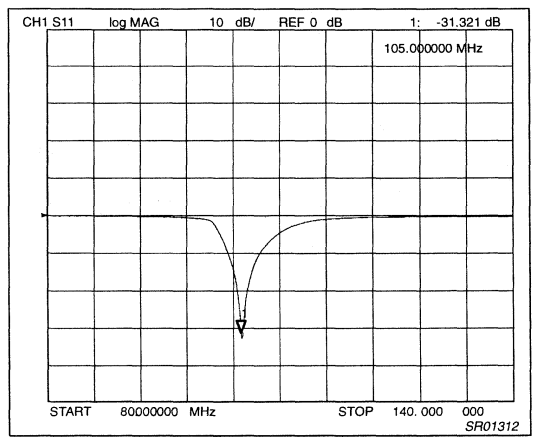


Figure 54. Mixer Output Set 5MHz Below Target to Get Final Result at 110.592MHz

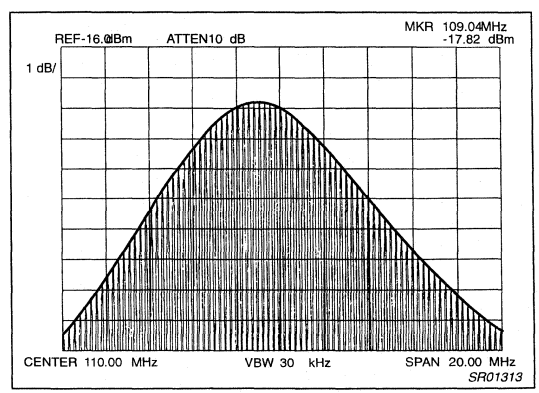


Figure 55. Mixer Output Set 5MHz Frequency Response Peak Very Near 110.592MHz Target

Summary of Mixer Open-Collector Output Concepts

The open-collector of a transistor offers a designer using the SA601 and SA620 the flexibility to provide impedance matching with minimal external components. Additionally, when an inductor is strategically located in the circuit, more AC output swing will occur due to the Early-Voltage effect of the device without adding any additional current.

When using the SA601 differential open-collector output, a designer can use the current-combiner circuit to combine the currents such that additional output signal swing is achieved. This preserves the RF signal and thus eliminates the need for interstage amplifiers. The current-combiner differential mixer output is not available on the SA620.

A flexible matching circuit can be used to deliver an equal amount of power to unequal resistive loads. The flexible matching circuit is ideal for trouble-shooting.

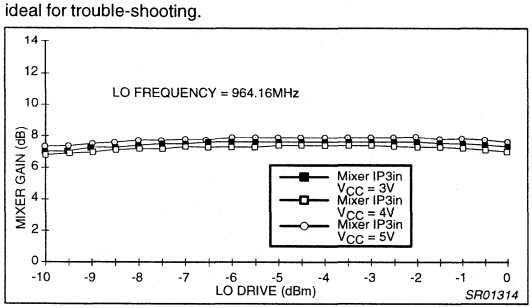


Figure 56. Mixer Gain vs LO Drive SA601

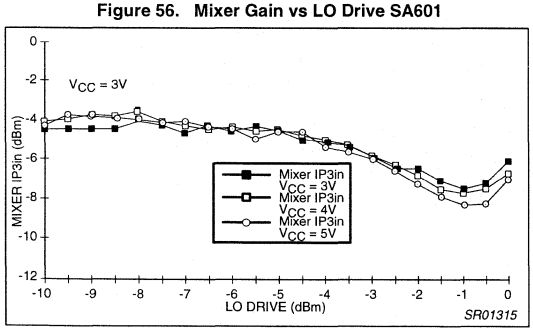


Figure 57. Mixer $IP3_{IN}$ vs LO Drive SA601

X. SA601 MIXER CHARACTERIZATION

Figure 56 shows a mixer gain vs. LO drive curve for a SA601 utilizing the current-combiner circuit in an application board environment. It shows that over an LO drive-level range of -10dBm to 0dBm the mixer gain deviates from an average value of 7.5dB by less than 0.5dB. It also shows that the gain will change by less than 0.5dB when V_{CC} is varied from 3V to 5V.

The noise figure of the SA601 generally increases with decreasing LO drive. Over the LO drive-level range of -10dBm to 0dBm the noise figure varied from approximately -12dB to approximately -8dB, respectively. The noise figure at - 5dBm LO drive is approximately 10dB.

Figure 57 shows the mixer's 60kHz $IP3_{IN}$ vs. LO drive curve for the SA601 in an application board environment. It should be noted that the $IP3_{IN}$ was measured with a -35dBm RF input at 881MHz and an offset of just 60kHz. 881MHz is the center of the 869 to 894 IS-54 Rx band, -35dBm was selected to ensure P_{IN} vs P_{OUT} linearity, and 60kHz was chosen as a suitable representation of current application alternate-channel constraints. The figure shows $IP3_{IN}$ to be constant at approximately -4.3dB over an LO drive-level range from -10dBm to approximately -5dBm. For LO drive-levels greater than -5dBm, $IP3_{IN}$ will decrease by approximately 1dB for every 1dB increase in LO drive. It is for this reason, that even though the mixer noise figure continues to decrease with larger LO drives, *the LO drive-level which optimizes gain, noise figure and $IP3_{IN}$ for current IS-54 applications is approximately -5dBm.*

SA601 System 12dB SINAD Performance

Figure 59 shows the 12dB SINAD vs RF input frequency of a receiver system composed of the SA601 utilizing the differential mixer output and the SA606 low-voltage FM-IF as shown in Figure 58. Data was taken over an input frequency range covering the 869 - 894MHz IS-54/AMPS Rx band as well as the 902 - 928 ISM band. *The 12dB SINAD performance in both bands was approximately -121 to -122dBm without a duplexer.* The system 12dB SINAD with a duplexer present will typically increase by approximately 3dB.

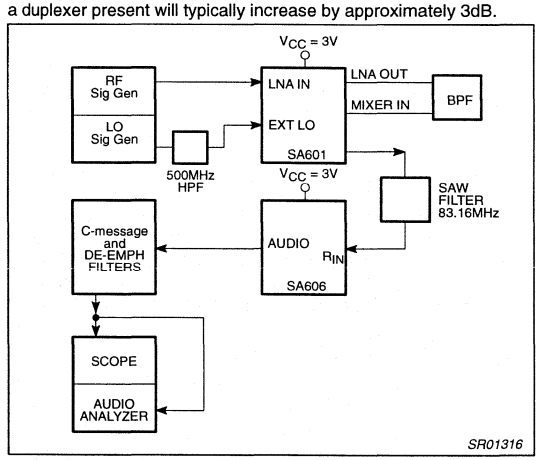


Figure 58. SA601 12dB SINAD System Test Configuration

XI. SA620 VCO

The SA620 features a low-power integrated VCO for providing an LO to the mixer. Thus, the additional cost and space associated with the use of an external VCO are eliminated. In the Philips SA620 application board environment shown in Figure 71, the VCO can be operated from 900MHz to approximately 1200MHz with the frequency range (using a 5V control voltage) increasing from 20MHz to 70MHz, respectively. Figure 60 shows the LO frequency vs. control voltage for two LO ranges centered at 960 and 995 MHz.

Figure 61 shows the VCO output power for the same LO ranges shown in Figure 60. The average VCO output power is approximately -20dBm and varies less than 0.5dB over the 5V control voltage range.

Figure 62 shows the VCO phase noise at a 60kHz offset for the same LO ranges shown in Figures 60 and 61. *The average phase noise (60kHz offset) is approximately -103dBc/Hz on*

non-silver-plated application boards and varies approximately 1dB across the 5V control voltage range. Phase noise performance may be improved another 1 – 2 dBc/Hz in with silver plating (see discussion below). It should be noted that a significant degradation of the phase noise performance was observed in the application board environment when the VCO was operated at frequencies above 1100MHz.

XII. μ-STRIP INDUCTOR OSCILLATOR RESONANT CIRCUIT [4, 5, 8]

The SA620 application board utilizes a high Q, μ-strip inductor in its oscillator resonant circuit to improve phase noise performance. Information concerning phase noise, μ-strips, and their implementation on the SA620 applications board is presented below

General Theoretical Background

Phase noise $S_\theta(fm)$ is a performance parameter of an oscillator circuit's spectral purity describing the energy it produces at frequencies fm on either side of the wanted carrier frequency f_c. To express how this works, an oscillator can be modeled as a feedback loop employing a phase modulator and noise-free amplifier to show how the resonator effects the phase characteristics of the resulting output. (A complete analysis of this model can be found in [4].)

In Figure 63, the phase spectral-density noise factor $S_{\theta IN}$ models internal phase noise produced by the oscillator's active components (e.g. BJT, FET etc.). Essentially, this factor is filtered by an external resonator that accepts energy from the noiseless amplifier which has sufficient gain G_O to sustain closed loop oscillations. Active circuitry with low internal phase noise will produce cleaner outputs for a given degree of filtering. Similarly, increasing the filtering will produce a cleaner output for a given internal spectral phase noise. Note that because of the feedback arrangement, the output spectral phase noise can never be less than that produced internally. These relations are summarized in the following equations, assuming the external resonator to be a simple parallel resonant LC tank circuit.

$$S\theta_{OUT}(fm) = |H(j\theta)|^2\, S\theta_{IN}(fm) \qquad (10)$$

$$S\theta_{OUT}(fm) = \left[1 + \left(\frac{f_o}{2Q_L\, fm}\right)^2\right] S\theta_{IN}(fm)\ ;\ (fm) > 0 \qquad (11)$$

In practice, a spectrum analyzer is commonly used to obtain an indirect measure of phase noise by measuring power vs. frequency, or the power spectrum on some specified bandwidth at various carrier offset frequencies m and then normalizing each reading to the equivalent power in a bandwidth of 1Hz. This technique of measuring SSB phase noise L(m) usually takes the peak carrier power as the 0dB reference. Thus, Equation 11 can be expressed as

$$L_{OUT}(fm) = \frac{1}{2}\left[1 + \left(\frac{f_o}{2Q_L\, fm}\right)^2\right] S\theta_{IN}(fm)\ ;\ (fm) > 0 \qquad (12)$$

SSB Phase Noise

and

$$L(fm) \equiv \frac{\text{noise power (in 1 Hz) with instrument corrections at } fm \text{ offset from the carrier } f_c}{\text{carrier power}} = \frac{N}{C} \qquad (13)$$

Equation 12 shows two possible ways to decrease an oscillators output phase noise $L_{OUT}(fm)$. Basically, we can decrease $S_{\theta IN}(fm)$ or increase the loaded-Q, Q_L of the tank circuit. In the case of the SA620, only the latter is feasibly controllable since $S_{\theta IN}(fm)$ is a property of the internal circuitry and, as already noted, places a lower attainable bound on $L_{OUT}(fm)$ as $Q_L \Rightarrow \infty$.

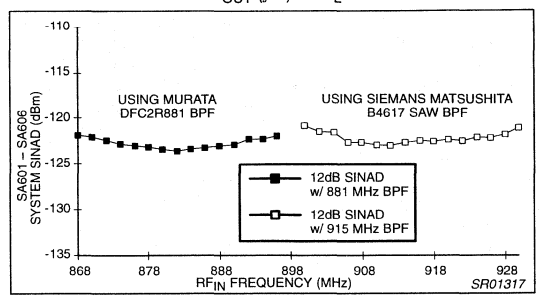


Figure 59. SA601 - SA606 System 12dB SINAD vs RF_{IN} Frequency

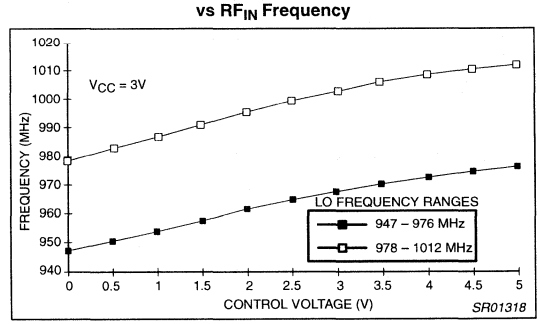


Figure 60. LO Frequency vs Control Voltage SA620 VCO

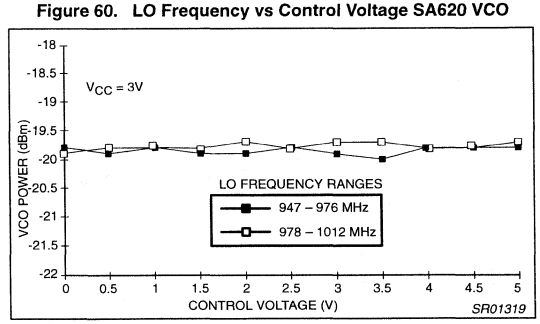


Figure 61. VCO Power vs Control Voltage SA620 VCO

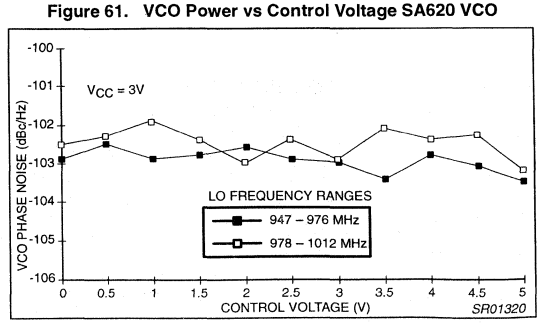


Figure 62. VCO Phase Noise vs Control Voltage SA620 VCO

Increasing Loaded-Q

Figure 64 shows the oscillator section of the SA620 with a conventional 2nd order parallel tuned tank circuit configured as the external resonator.

From the basic equations for parallel resonance, the resonator's loaded-Q is given by

$$Q_L = R_P \left[\frac{C_T}{L_T}\right]^{(1/2)} \quad (14)$$

where

$$R_P = R_T \;||\; R_C = \left[\left(\frac{1}{R_T}\right) + \left(\frac{1}{R_C}\right)\right]^{-1} \quad (15)$$

represents the net shunt tank resistance appearing across the network at resonance. R_T represents losses in the inductance L_T and capacitance C_T (almost always dominated by inductor losses), and R_C is the active circuits load impedance at resonance. Improving the quality (i.e., their Q) of the tank components, L_T and C_T will increase R_T, but since R_C is low in the case of the SA620, the resulting increase in R_P is relatively small. We can increase R_P by decoupling Z_C from the tank circuit (note that R_C is the real part of Z_C at resonance). Decoupling this impedance by using either tapped-L or tapped-C tank configurations is possible. Inspection of the circuit shows that DC biasing is necessary for Pins 9 and 10 (osc1 and osc2, respectively), so a tapped-C approach would require shunt-feeding these pins to V_{CC}. Thus, the most practical way is to employ a tapped-L network.

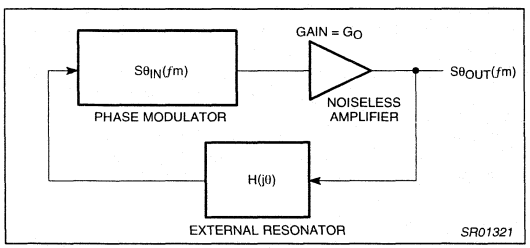


Figure 63. Oscillator Phase Noise Model

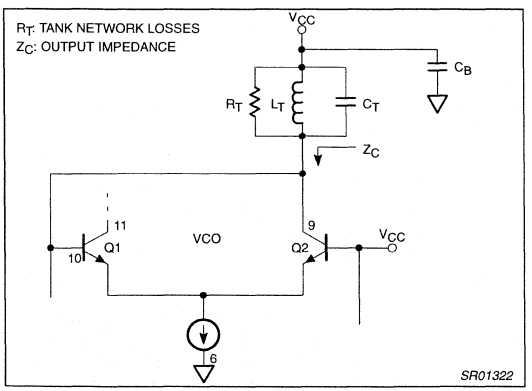


Figure 64. SA620 With External Resonator

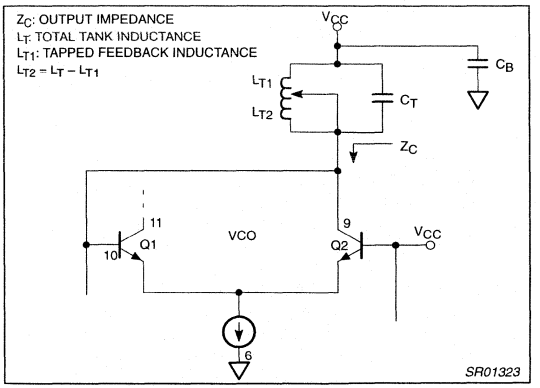


Figure 65. SA620 With Tapped-L Resonator

Figure 65 shows the basic tapped-L circuit. The effective multiplied shunt impedance at resonance across C_T is given by

$$\hat{R}_P = R_P \left[\left(\frac{L_{T2}}{L_{T1}}\right) + 1\right]^{1/2} \quad (16)$$

with a corresponding increase in loaded Q

$$\hat{Q}_L = Q_L \left[\left(\frac{L_{T2}}{L_{T1}}\right) + 1\right]^{1/2} \quad (17)$$

Feedback is caused by an RF voltage appearing across L_T, coupled through bypass capacitor C_B and its ground return to the cold end of the current source at Pin 6. The significance of this path increases with frequency. At 900MHz it becomes very critical to obtaining stable oscillations and must be kept as short as possible. Attention to layout detail cannot be overlooked here!

High-Q Short μ-Strip Inductor

Realizing a stable tapped-L network using lumped surface-mount inductors is impractical due to their low unloaded-Q and finite physical size. Another approach utilizes a high-Q short microstrip inductor. The conventional approach to microstrip resonators treats them as a length of transmission line terminated with a short which reflects back an inductive impedance which simulates a lumped inductor. The approach presented here deviates from this technique by specifically exploiting the very high unloaded-Q attainable with short microstrip inductors where we design for a large C/L ratio by making the microstrip a specific but short length. Resonance is achieved by replacing the short with whatever capacitance is needed for proper resonance. One equation for the inductance of a strip of metal having length l (mil) and width w (mil) is

$$L = [5.08E - 3]\ell\ [\ln(\ell/w) + 1.193 + 0.224(w/\ell)]\ \ [nH/mil] \quad [4]\ (18)$$

This technique results in a much shorter strip of metal for a given inductance. One intriguing property of microstrip inductors is that they are capable of very high unloaded-Q's. An equation describing the quality factor for a "wide" microstrip line is

$$Q_C = 0.63h\ [\sigma f_{GHz}]^{1/2} \quad [5]\ (19)$$

where h is the dielectric thickness in centimeters, σ is the conductivity in [S/m] and f is frequency in GHz. This equation predicts an unloaded-Q exceeding 700 when silver-coated copper is used. Also, wide microstrip lines are defined as those whose strip width w to height h ratio is approximately or greater than 1, i.e. w/h > 1. The parallel capacitor formed by the metal strip over the

ground plane should also be included and may be calculated by the classic formula and included in the total needed to resonate with the inductance result found from equation (18). This "strip" capacitance is given by

$$C_S = K\varepsilon_0\varepsilon_r \text{ [wl/h] [Farad]} \quad (20)$$

where ε_O= 8.86E-12 [F/cm] is the permitivity of free space, r is the relative dielectric constant of the substrate. A "fringe factor" K is included to account for necessary fringing (est 2% to 15%). These equations are meant to provide insight into circuit behavior and should, therefore, be applied cautiously to specific applications.

UHF VCO Using the SA620 at 900MHz

The basic electrical circuit involving the SA620 is shown in Figure 66. Feedback occurs when sufficient RF voltage develops across the tap inductances L_{T1} and L_{T2} (due to tap-1 and tap-2 respectively); note that inductance is reckoned from the cold end of the tank at node A. Taps 1 and 2 should be as close as possible to Pins 10 and 9, respectively. Also, nodes A (cold end of tank) and B (Pin 6) must be as physically close together and exhibit as low an impedance as possible to discourage parasitic oscillations. This "inner-loop" composed of L_{T2}, inductance of taps 1 and 2 connecting to Pins 10 and 9, and stray low Q inductance between nodes A and B create a parasitic loop that will favor oscillations that no longer depend on the full tapped-L tank circuit. This low-Q loop will exhibit very poor phase noise and typically oscillate well above 1200MHz; it has been observed as high as 1600MHz.

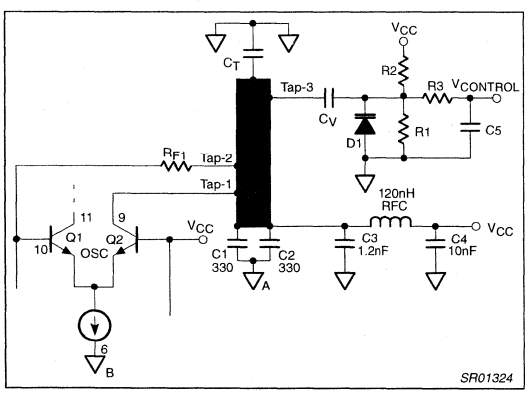


Figure 66. SA620 with Tapped-L μ-Strip Resonator

Another factor also affects this unwanted parasitic oscillation. As the loaded-Q of the tapped tank circuit decreases, the circuit becomes conditionally stable and will eventually favor the parasitic loop exclusively. This occurs because tapped-L loaded-Q affects the magnitude of the RF voltage appearing across the entire microstrip tank. Thus, feedback at taps 1 and 2 is reduced as the Q decreases. This increases the likelihood of the inner-loop parasitic controlling the oscillator, since its feedback voltage is largely independent of the μ-strip tank Q.

Equation 19 shows that microstrip inductors are capable of very high unloaded-Q's. This depends on a number of physical factors: frequency, dielectric thickness and its quality, and the skin depth conductance of the metal strip itself. For example, at 900MHz, when coated with silver, unloaded-Q is somewhere about 750; when coated with lead (or sloppy soldering!) it drops to less than 230. If the unloaded-Q is too low, the loaded-Q also drops and the circuit becomes conditionally stable, and now will either oscillate at the higher parasitic inner-loop or the wanted tapped-L lower complete tank circuit frequency. Components should be connected by narrow traces closely connected to component pads to avoid soldering on the microstrip layer.

The addition of R_{F1} introduces necessary losses to control the inner-loop parasitic oscillation. Its size should be made as small as possible consistent with stability, startup and good phase noise performance. Since it also decreases feedback, LO injection falls off as it increases. Typically, experimental values from 4Ω to 30Ω have proved sufficient. Stability as a function of V_{CC} is a good way to assess conditional stability. Provided the microstrip tank has a high loaded-Q, stability should be independent of V_{CC} down to less than 2.5V, or so. When loaded-Q decreases, so as to favor the inner-loop parasitic, conditional stability will occur. This can readily be observed by increasing V_{CC} beginning at about 1.0V and noting whether the VCO jumps back and forth unpredictably. Mixer and LO port loading also affect this condition and should be considered.

Dimensions for the microstrip resonator are based on several criteria. The strip must be "wide": its width to height must be on the order of 1 or greater. Minimum strip length seems to be about 200 mils for a 62 mil thick board. L/C ratios somewhere about 500 have yielded quite good results. Note that we usually specify the "L/C" ratio because it is always greater than 1, even though in a parallel resonant circuit it appears in the Q equation as C/L. Thus, decreasing the "L/C ratio" by making the microstrip shorter helps the loaded inductor Q, and the circuit loaded-Q_L, increase (see Equation 14). However, the effect of the lower Q of C_T, even when using a "hi-Q" SM type, decreased the expected larger increase in the net loaded circuit Q. Thus, the expected increase in Q_L may not be fully realizable. Assuming a 62 mil thick board with FR5 dielectric, a strip 50 by 300 mils gave very good experimental results where C_T was about 4.3pF with oscillations occurring from about 950 to 1000MHz for various test boards. A shorter inductor designed to increase the C/L ratio requiring 7.5pF experimentally resulted in only about 1–2dB improvement at 950MHz.

Tap-1 may be anywhere between the cold end of the tank (where C_1 and C_2 are located) and tap-2. Tap-2 yields good results at about 1/3 the strip length. Making it too close to the cold end in an effort to increase Q_L will result in loss of control over the inner-loop parasitic. To keep Q_L as large as possible, C_T should be a Hi-Q SM type. Differences greater than 5dB in SSB phase noise have been observed between a generic NPO SM and Hi-Q NPO SM capacitor.

Tap-3 can be at the end of the microstrip where C_T is connected. However, the varactor inevitably will cause a decrease in overall loaded-Q, typically by as much as 5dB. Moving it back some distance from the high end of the tank will decrease this effect and yield better results. A good starting point is about 1/4 back or 3/4 of the length from the cold end. C_1 and C_2 are paralleled lower value capacitors to yield a better low-impedance ground return to Pin 6 (node B) since relatively large RF currents flow through them. Note that as Q_L increases the peak circulating RF current will also increase, as will the RF voltage at the high end of the microstrip. At 900MHz good results have been obtained when both are about 330pF. RFC was chosen to be approximately series-resonant around 900MHz and constitutes the series feed path for DC biasing. It may be possible to neglect this component entirely, provided the PCB connection to the cold end of the tank is very close to RF ground. Finally, note that shielding of the entire microstrip may be necessary to meet part 15 emission limitations (where applicable).

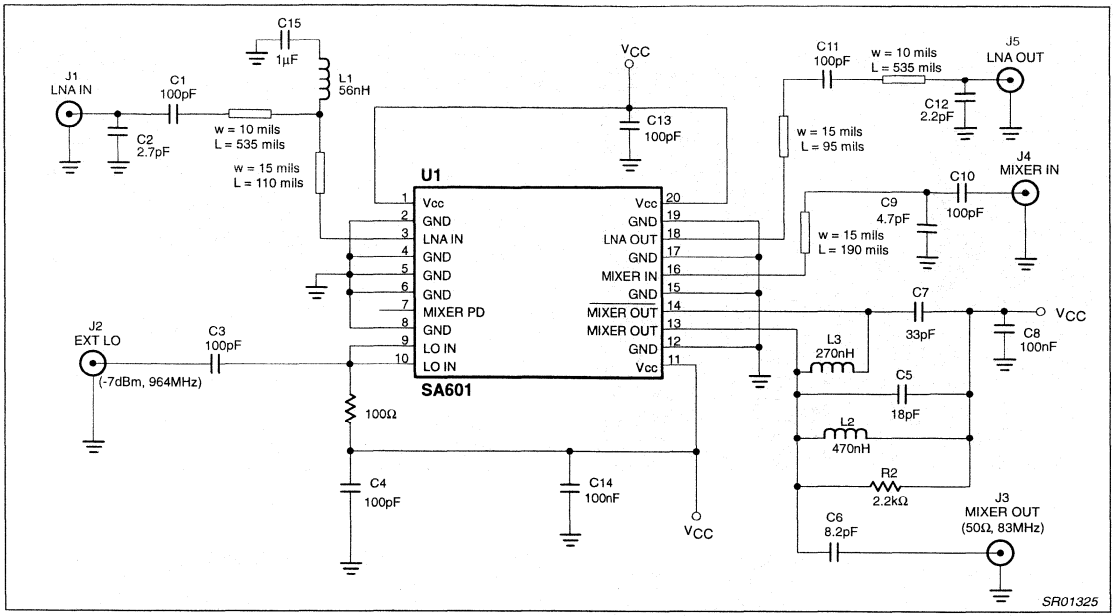
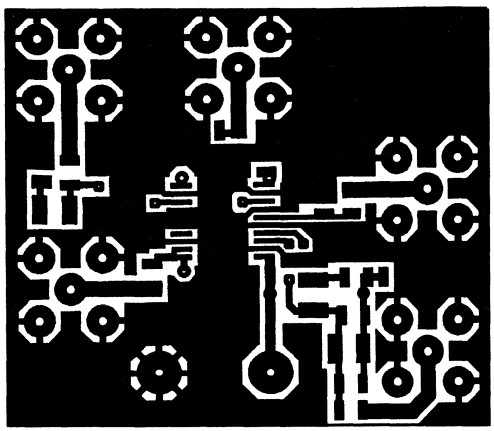
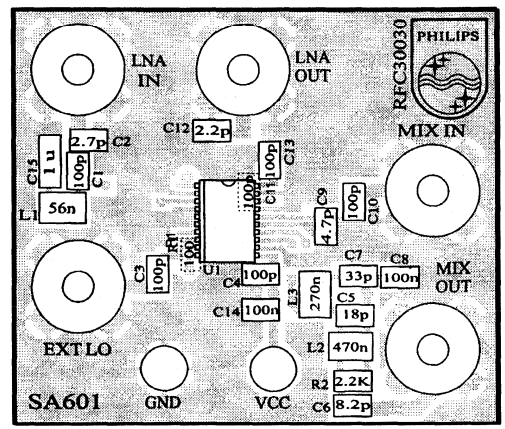


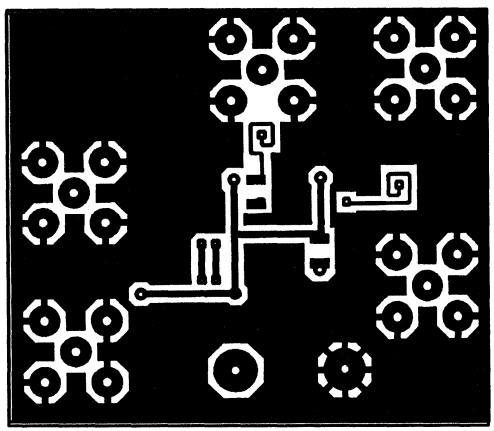
Figure 67. SA601 Application Board Schematic



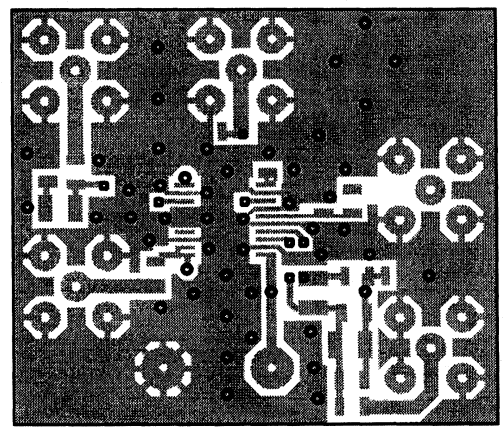
Top View



Silk Screen



Bottom View



Via Layer

SR01326

Figure 68. SA601 Demoboard Layout (Not Actual Size)

Table 5. Customer Application Component List for SA601

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	2.2pF	50V	C12	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG229C9BB0
1	2.7pF	50V	C2	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG279C9BB0
1	4.7pF	50V	C9	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG479C9BB0
1	8.2pF	50V	C6	Cer Cap 0805 NPO ± 0.5pF	Garrett	Philips	0805CG829C9BB0
1	18pF	50V	C5	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG180J9BB0
1	33pF	50V	C7	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG330J9BB0
6	100pF	50V	C1, C3, C4, C10, C11, C13	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG101J9BB0
2	0.1µF	50V	C8, C14	Cer Cap 0805 Z5U ± 20%	Garrett	Philips	0805E104M9BB0
1	1µF	25V	C15	Cer Cap 1206 Y5V ± 20%	Garrett	Rohm	MCH312F105ZP
Surface Mount Resistors							
1	100Ω	50V	R1	Chip Res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR10JW101
1	2.2kΩ	50V	R2	Chip Res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR10JW222
Surface Mount Inductors							
1	56nH		L1	1008 size chip inductor ± 10%	Coilcraft	Coilcraft	1008HS-560XKBB
1	270nH		L3	1008 size chip inductor ± 10%	Coilcraft	Coilcraft	1008HS-271XKBB
1	470nH		L2	1008 size chip inductor ± 10%	Coilcraft	Coilcraft	1008HS-471XKBB
Surface Mount Integrated Circuit							
1		3V	U1	RF low noise amplifier / mixer	Philips	Philips	SA601DK
Miscellaneous							
5				SMA gold connector	Newark	EF–Johnson	142-0701-801
2				Terminal	Newark	Cambion	160-1558-02-01
1				Printed Circuit Board	Excel	Philips	SA601 - RFC30030
29 Total Parts							

XIII. APPLICATION BOARDS

SA601 Applications Board

Figure 67 shows the schematic of the current application board for the SA601.

The functional description of each pin and its associated external circuitry is summarized below.

Pins 1, 11 and 20 are all V_{CC} supply pins. Capacitor C_{13} is for decoupling purposes.

Pins 2, 4, 5, 6, 8, 12, 15, 17 and 19 are all ground connections and should be tied to a common ground plane and as close to the chip as possible.

Pin 3 is the LNA mixer input pin. The LNA input has an associated network for the purpose of optimizing the return loss while minimizing the degradation of the noise figure. This network is composed of Capacitor C_2, L_1 and the 535 mil spiral inductor. Capacitor C_1 is a DC blocking cap.

Capacitor C_{15} and inductor L_1 also provide the LNA with voltage compensation.

Pin 7 is the mixer power-down pin. It will disable the mixer if set low. The application board simply leaves this pin open.

Pin 9 and Pin 10 are both connected to the local oscillator input. It is important to have good return loss at this pin to allow small LO drive-levels to be used. Capacitors C_4 and C_{14} are decoupling caps. C_3 is a DC blocking cap.

Pin 13 and Pin 14 are the differential mixer outputs. Inductor L_3 and capacitors C_5 and C_7 comprise the differential-to-single-ended translation circuit which combines the output currents and forces them to be in phase with each other. This circuit is extensively described in the previous discussions. R_2 sets the output impedance of the mixer output and L_2 is the DC bypass inductor which increases the gain of the open-collector output. Capacitor C_6, in conjunction with L_2, is used to match the mixer output port to 50Ω.

Pin 16 is the mixer input pin. Capacitor C_9 is used to optimize return loss and noise figure. Capacitor C_{10} is a DC blocking cap.

Pin 18 is the LNA output pin. Capacitor C_{12} in conjunction with the 535 mil spiral inductor comprise a network for optimizing return loss and obtaining best noise figure. C_{11} is a DC blocking cap.

SA601 Application Board Modification For Increasing Mixer Gain

The SA601 application board can be modified by disconnecting the 2.2kΩ resistor R2 in Figure 67 and reconnecting it in parallel with C7. Figure 69 shows a comparison of the mixer gain with and without this modification. This modification yields a 2dB improvement in mixer conversion gain for LO drive-levels from -10dBm to 0dBm. Figure 70 shows a comparison of the mixer $IP3_{IN}$ with and without this modification over the same LO drive-level range as in Figure 69. This data shows that the $IP3_{IN}$ performance of the mixer is not degraded for LO drive-levels less than or equal to -5dBm. Some degradation does occur for LO drive-levels above -5dBm. Laboratory comparison data of noise figure performance also showed that over the LO drive-level range of -10dBm to 0dBm the modification of R_2 yielded a decrease in noise figure of approximately 0.3dB. The R_2 modification does draw about 0.3mA more supply current, however.

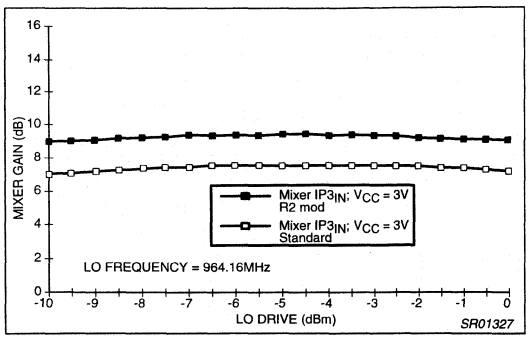


Figure 69. SA601 Mixer Gain vs LO Drive Standard/R2 Modification Comparison

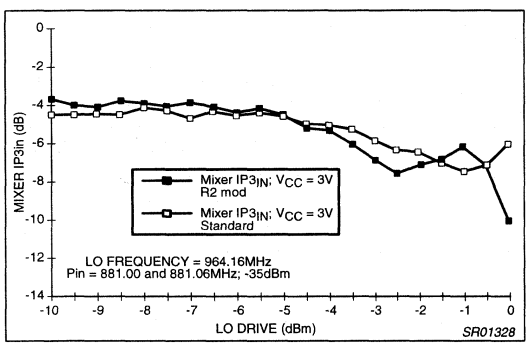


Figure 70. SA601 Mixer $IP3_{IN}$ vs LO Drive Standard/R2 Modification Comparison

SA620 Applications Board [7]

Figure 71 shows the schematic of the current application board for the SA620. The functional description of each pin and it's associated circuitry is summarized below.

Pin 1 is the LNA enable pin. This pin is used for selecting the gain in the LNA path.

The logic levels for the SA620 LNA enable are specified as:

Logic "1" level (LNA on):	+2.0V to V_{CC}
Logic "0" level (LNA off):	-0.3 to +0.8V

Referring to the application board schematic, resistor R_8 and capacitor C_{25} are used to improve LNA enable switching time. If fast switching is not a requirement, or if the LNA does not need to be disabled, these two components can be eliminated.

Pins 2, 4, 5 and 19 are ground connections. These pins provide the RF ground path for the LNA and should be tied to a common ground plane as close to the IC, and each other, as possible.

Pin 3 is the LNA input. The LNA input exhibits a return loss of 7dB at 900MHz. However, the designer can implement an external matching circuit to further improve the match. For this reason, S_{11} plots of the LNA input impedance measured right at Pin 3 are provided in the SA620 data sheet.

Referring again to the application board schematic, the 260 mil long transmission line, inductors L_1, the 4.7nH spiral inductor, and capacitor C_2 are the matching elements. Capacitor C_1 is a DC blocking capacitor. Conjugately matching the LNA input for optimum gain performance will degrade the noise figure slightly. Typically, 1.6dB noise figure can be achieved when the return loss is improved to 10dB.

Pin 6 and Pin 12 are the oscillator ground connections. These pins provide the RF ground path for the oscillator section of the SA620 and should be tied to a common ground plane as close to the IC, and each other, as possible.

Pin 7 and Pin 8 are the mixer and oscillator power down pins, respectively. These pins can be used to individually power down the mixer and the oscillator sections of the SA620.

The DC levels at Pins 7 and 8 are approximately 2.3V and 1.5V, respectively, and these levels must be established by the IC and not the power down circuitry. Placing a Schottky diode (V_f = 0.3V) between each power down pin and the LNA ENABLE pin will allow the designer to power-down the IC via a single control voltage, the LNA enable, while allowing the voltages at Pins 7 and 8 to float at the IC levels when in the power-up mode.

Pin 9 and Pin 10 drive the base of one and the collector of another of the broadband VCO differential pair input stage transistors as shown in Figure 64. Components C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, L_2, R_1, R_2, R_3, R_4, D_1 and the 300 mil μ-strip comprise the resonant tank circuit described in detail above and shown in Figure 66.

Pin 11 is the open-collector VCO output and is provided to couple out VCO energy for frequency synthesis for example. Resistor R_5 is chosen to be small so as not to excessively load down the VCO. Hence, only about -20dBm of VCO fundamental output power will be measured at the VCO_{OUT} connector on the application board. Note that the second harmonic power level will actually be slightly higher than that of the fundamental. This is not a problem because this isn't the same signal that is driving the mixer, and the mixer develops its own second harmonic as a result of the mixing process anyway. The 4.7nH spiral inductor and capacitor C_{12} on the application board are the 50Ω matching elements. Capacitor C_{13} is a decoupling capacitor.

Pin 13 is the open-collector mixer output. Referring to the application board schematic, R_6 establishes the output impedance to be 1kΩ. Inductor L_3 and capacitors C_{15} and C_{16} are 50Ω matching elements.

Pin 14 is the mixer bypass pin. This is not a signal output. It is provided for designers to optimize the IP3 performance of the mixer circuit. If you look closely at the application board schematic, you will notice that the two circuit elements at Pin 14, the 2.5 - 6.0pF capacitor and the 4.7nH spiral inductor, are very small impedances at the 83MHz IF frequency. The intent is to reflect RF leakage energy back into Pin 14 to achieve phase cancellation of this energy inside the IC, thus reducing the level of third-order intermodulation products. While looking at the third-order intermodulation products on a spectrum analyzer, the designer can tune with C_{17} to minimize the level of these products at the IF output. To obtain the best $IP3_{IN}$ performance over the entire frequency range of the VCO the following procedure is recommended:

1. Set the VCO control voltage to its mid-range value of 2.5V.
2. Adjust capacitor C_9 to obtain the desired mid-range frequency,
3. Tune C_{17} for best $IP3_{IN}$.

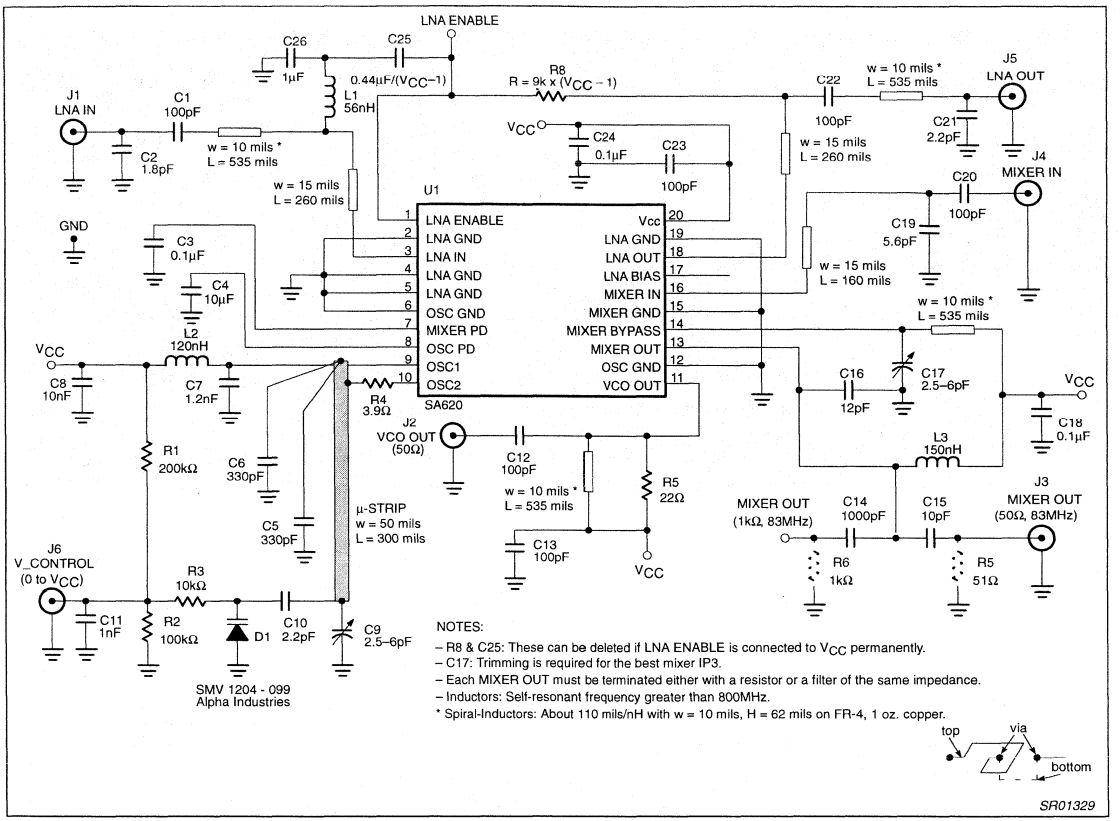


Figure 71. SA620 Application Board

Pin 15 is the mixer ground connection. This pin provides the RF ground path for the mixer section of the SA620 and should be tied to a common ground plane as close to the IC as possible.

Pin 16 is the mixer input pin. The mixer input is not matched to 50Ω, therefore, external matching elements are required to achieve optimum performance. The 160 mil long transmission line and capacitor C_{19} are the matching elements on the application board. C_{20} is a DC blocking capacitor. If no matching elements are used, the IP3 performance is typically maximized at +3dBm at the expense of gain, which will be reduced by 3dB.

Pin 17 is the LNA bias pin. This is a DC check pin for use during the manufacture of the SA620 only. Customers should float this pin in their designs.

Pin 18 is the LNA output pin. The LNA output has an intrinsic return loss of approximately 9dB at 900MHz. However, to achieve optimum performance from the SA620, the designer can implement an external matching circuit to further improve the match. For this reason, S_{22} plots of the LNA output impedance measured right at Pin 18 are provided in the SA620 data sheet. Referring again to the application board schematic, the 260 mil long transmission line, the 4.7nH spiral inductor, and capacitor C_{21} are the matching elements. Capacitor C_{22} is a DC blocking capacitor.

Pin 20 is the DC power input to the SA620 where capacitors C_{23} and C_{24} are strictly for decoupling purposes.

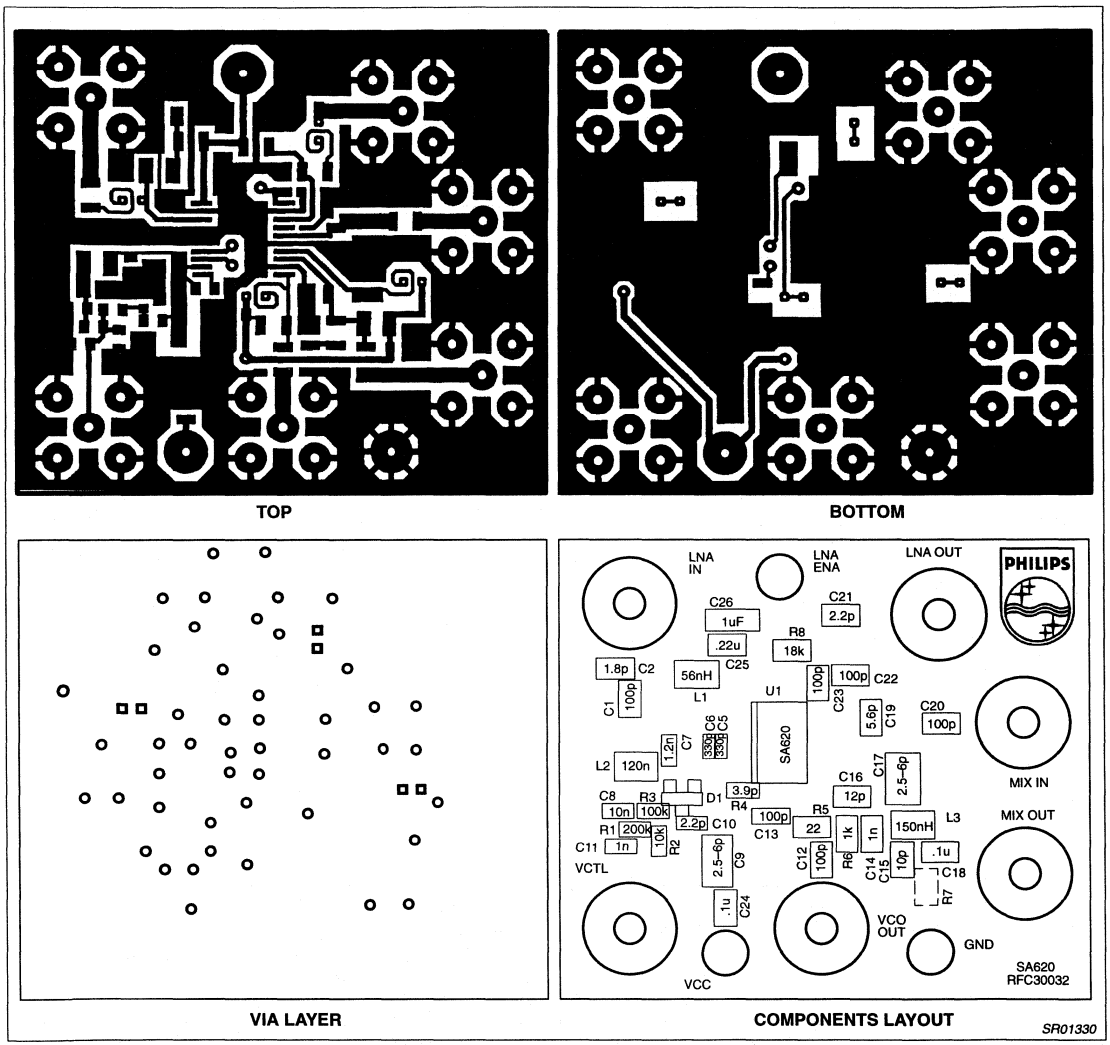


Figure 72. SA620 Demoboard Layout (Not Actual Size)

XIV. TEST AND MEASUREMENT TIPS

Noise Figure and Gain

The LNA of both the SA601 and SA620 can be tested identically. The gain and noise figure can be measured on a noise figure meter such as the HP8970. The correct measurement mode on this particular piece of equipment is obtained by selecting special function 1.0. It is important to do all noise figure measurements within a screen room to ensure the receiver of the noise figure meter is not picking up any stray signals. The LNA gain can also be measured on a spectrum analyzer. For accurate measurements, be sure to properly compensate for losses in the cables and connectors used. Also, make sure that the input power used is well below the 1dB compression point for the device. P_{IN} = -25dBm is a good value.

The SA601 and SA620 mixers require more precaution while testing. The correct measurement mode for mixer noise figure and gain measurements is obtained on the HP8970 by selecting special function 1.4. It should be stated again that all noise figure measurements should be done within a screen room. The noise source used in conjunction with the noise figure meter is generally a wideband noise source. So, for a given LO frequency there are two regions of the wideband noise power spectrum which will mix to the specified IF frequency. Thus, an image-reject bandpass filter should be placed between the noise source and the mixer input. In this way

the unwanted input noise power will be rejected yielding proper single sideband noise figure measurements. The loss through this image-reject filter should also be accounted for. Losses prior to the mixer input can be compensated for on the HP8970 by selecting special function 34.2. The noise figure of the mixers is highly dependent on the strength and quality of the LO signal. The LO signal should be passed through a high-pass filter. A 500MHz HPF is typically used. The noise figure is dependent on the LO drive-level. Generally, the noise figure will decrease as the LO drive-level is increased. The noise figure has also been observed to show some dependence on the range setting of the signal generator. The high-frequency components present at the IF output of the mixer should also be filtered out prior to entering the input port of the noise figure meter. This is typically done with a 300MHz low-pass filter. If the conversion gain of the mixer is to be measured directly on a spectrum analyzer, be sure that the input power is well below the 1dB compression point. Again, -25dBm is a good value.

Table 6. Customer Application Component List for SA620

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	2.2pF	50V	C10	Cer Cap 0603 NPO ± .25pF	Garrett	Rohm	MCH185A2R2CK
2	330pF	50V	C5, C6	Cer Cap 0603 NPO ± 5%	Garrett	Rohm	MCH185A331JK
1	1000pF	50V	C11	Cer Cap 0603 X7R ± 10%	Garrett	Rohm	MCH185C102KK
1	1200pF	50V	C7	Cer Cap 0603 X7R ± 10%	Garrett	Rohm	MCH185C122KK
1	0.01µF	25V	C8	Cer Cap 0603 X7R ± 10%	Garrett	Rohm	MCH185C103KK
1	1.8pF	50V	C2	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG189C9BB0
1	2.2pF	50V	C21	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG229C9BB0
1	5.6pF	50V	C19	Cer Cap 0805 NPO ± 0.5pF	Garrett	Philips	0805CG569C9BB0
1	10pF	50V	C15	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG100J9BB0
1	12pF	50V	C16	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG120J9BB0
6	100pF	50V	C1, C12, C13, C20, C22, C23	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG101J9BB0
1	1000pF	50V	C14	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG102J9BB0
3	0.1µF	50V	C3, C18, C24	Cer Cap 0805 Z5U ± 20%	Garrett	Philips	0805E104M9BB0
1	0.22µF	50V	C25	Cer Cap 0805 Y5V ± 20%	Garrett	Rohm	MCH212F224ZK
1	10µF	10V	C4	Tant Chip Cap B 3528 ± 10%	Garrett	Philips	49MC106C010KOAS
1	1µF		C26	Cer Cap 1206 Y5V ± 20%	Garrett	Rohm	MCH312F105ZP
Surface Mount Variable Capacitors							
2	2–6pF		C9, C17	Trimmer capacitor	Murata	Murata	TZV02Z060A110
Surface Mount Resistors							
1	3.9Ω		R4	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW3.9
1	10kΩ		R3	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW103
1	100kΩ		R2	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW104
1	200kΩ		R1	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW204
1	22Ω		R5	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW220
1	51Ω		R7	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW510
1	1kΩ		R6	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW102
1	18kΩ		R8	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW183
Surface Mount Inductors							
1	56nH		L1	Chip inductor 1008CS ± 10%	Coilcraft	Coilcraft	1008CS-560XKBB
1	120nH		L2	Chip inductor 1008CS ± 10%	Coilcraft	Coilcraft	1008CS-121XKBB
1	150nH		L3	Chip inductor 1008CS ± 10%	Coilcraft	Coilcraft	1008CS-151XKBB
Surface Mount Integrated Circuit							
1		3V	U1	Low voltage LNA & Mixer	Philips	Philips	SA620DK
Miscellaneous							
1			D1	Varactor	Wireless Components	Alpha Industries	SMV 1204-099
6				SMA gold connector	Newark	EF-Johnson	142-0701-801
3				Terminal	Newark	Cambion	160-1558-02-01
1				Printed Circuit Board	Excel	Philips	SA620 - RFC30032
49 Total Parts							

1dB Compression Point

This is determined by taking P_{OUT} vs. P_{IN} data at very low input power where the relationship between these quantities is linear. An input power range between -35dBm and -30dBm is sufficient for both the LNA and mixer. The input power is then increased to the

point where the difference between an extrapolation of the low input vs output power line and the output power is 1dB. The input power at which this occurs is the 1dB compression point. A shorter and more practical method of obtaining this parameter is to adjust the input power at a low level such that the output power is some integer number. Then increase the input power in 1dB increments. The output should also increase in 1dB increments. When the output power becomes exactly 1dB less than the expected value, the input power at which this occurs is the 1dB compression point.

Input Third-Order Intercept Point

$IP3_{IN}$ is typically measured on a spectrum analyzer by combining two input signals of equal power that are detuned by approximately 60kHz. This is then connected to the input of the device. Be sure to measure the output power of the two peaks after the power combiner because the two ports of the power combiner rarely attenuate equally. $IP3_{IN}$ is read off the spectrum analyzer by measuring the difference between the two carrier peaks and the intermodulation peaks, then adding half this difference to the input power.

It is extremely important to take this data at very low input power because this calculation assumes linearity. Input power of -35dBm is sufficient.

Phase Noise

The most economical way to measure phase noise is using the spectrum analyzer. As previously stated, this is done very simply by measuring the difference between the carrier frequency peak power and the power at some specified offset from the carrier. Unfortunately, the spectrum analyzer does not have the capability of measuring this with a 1Hz resolution bandwidth. Thus, a calculation must be made as follows:

$$\text{Phase Noise (dBc/Hz)} = -(|\Delta| + 10\log(\text{RBW}))$$

where Δ is the difference between the peak power at the carrier frequency and the power at the specified offset frequency, and RBW is the resolution bandwidth of the spectrum analyzer while taking the measurement.

XV. COMMON QUESTIONS AND ANSWERS

Q. I'm not getting the Mixer Noise Figure that is stated in the databook. What could be wrong?
A. There are quite a few things that can affect your noise figure. The most important thing to do initially is to check your measurement setup by following the suggestions in the test and measurement section of this application note. Aside from that, maintaining a good match at the LO input is very important and using the same LO drive-level specified in the databook is also necessary.

Q. Does the SA620 VCO meet AMPS stringent phase noise requirements?
A. The SA620 VCO phase noise is typically about -102dBc/Hz @ 60kHz. This does not meet AMPS specifications of -110dBc/Hz @ 60kHz.

Q. Can the SA620 be used with an external VCO to get better phase noise performance?
A. Although possible, this is not recommended due to the higher output power of the external VCO causing LO leakage problems at the mixer output.

Q. Why was the current-combiner implemented with a C - L - C arrangement instead of its dual circuit approach?
A. The C - L - C arrangement has the advantage of being low-pass in nature. Thus, it supplies additional rejection of the higher frequency RF_{IN} and LO signals at the mixer output.

Q. Why am I not getting the $IP3_{IN}$ values that are stated in the databook?
A. In addition to checking your test setup, you might want to check what the offset is between your two RF input signals. Some of the databook values are taken with an offset of 1MHz. Chances are that your offset is much smaller. For instance, AMPS alternate channel spec is only 60kHz. $IP3_{IN}$ will decrease when this offset is decreased.

Q. What are the necessary components needed to ensure unconditional stability of the LNAs.
A. Capacitor C_{15} and inductor L_1 on the SA601 schematic of Figure 67 are the necessary components needed to ensure stability. Without these components, the amplifier will generate spurs approximately 1.5MHz off the carrier at V_{CC} = 3V. The similar components on the SA620 schematic in Figure 71 are capacitor C_{26} and inductor L_1.

XVI. REFERENCES

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Using the SA7025(RevA) and SA8025A for narrow band systems AN1890

Author: Wing S. Djen

INTRODUCTION

The SA7025 (RevA) and SA8025A are improved versions of the SA7025 and SA8025 suitable for narrow band systems like the America Digital Cellular System (IS-54) and Japan Personal Digital Cellular System (PDC). The new design improves the performance of the fractional spurs compensation, which is a by-product of the fractional-N divider. Complete design procedure and performance measurements on both the SA7025 (RevA) and SA8025A are included in this document.

The basics of the fractional-N PLL frequency synthesizers can be found in Philips Semiconductors application note AN1891, "SA8025 Fractional-N synthesizer for 2GHz band applications". AN1891 can be used in conjunction with this document for designing-in the SA7025, SA8025, SA7025 (RevA), and SA8025A.

Fractional Spurs Compensation

The fractional-N divide ratio is achieved by changing the divide ratio between N and N+1. In lock condition, this technique will introduce an instantaneous phase error in the phase detector. This causes the VCO to generate unwanted spurs at the offset of the fractions of the comparison frequency.

On the new SA7025 (RevA) and SA8025A, the fractional compensation circuitry was re-designed to achieve better performance. Three improvements can be found on the SA7025 (RevA) and SA8025A due to this modification:

1. The CN range is much tighter. The CN values are the binary current setting factor for the charge pumps. These values may be varied across the desired frequency band (e.g. 25MHz) for fractional spurs compensation. For the SA7025/SA8025, the CN range is greater than 50 for narrow band systems (e.g. channel spacing, f_{CH}=30kHz). For the new SA7025 (RevA)/SA8025A, this range is much tighter and a **fixed** CN value is usually good enough for all synthesized frequencies on the SA7025 (RevA)/SA8025A.
2. A more accurate calculation of the resistor RF, which determines the amount of fractional compensation current. Eq. 1 gives an approximate value of I_{RF}. RF can be calculated using Eq. 2, which is the same as the one for calculating resistor RN. To obtain an optimum performance, the CN value can be adjusted accordingly.

$$I_{RF} = \frac{3 \cdot I_{RN} \cdot CN \cdot f_{XTAL}}{Q \cdot f_{VCO}} \quad (1)$$

$$RF = \frac{V_{DDA} - 0.9 - 150 \cdot \sqrt{I_{RF}}}{I_{RF}} \quad (2)$$

3. Better performance over temperature. The variation of fractional spurs was minimized over the rated temperature range (-40 to +80°C).

Compatibility Between the SA7025/SA8025 and SA7025 (RevA)/SA8025A

The SA7025/SA8025 and SA7025 (RevA)/SA8025A are pin-to-pin compatible and have exactly the same performance except for the fractional compensation section. When replacing the SA7025/SA8025 with SA7025 (RevA)/SA8025A, new values for CN and resistor RF may have to be used. Users should calculate resistor RF using Eq. 1 and 2 and experiment with it on the bench with the new RF value.

PLL Design Equations

δ : final frequency resolution after settling.

$$\delta = \frac{\text{frequency error after settling}}{\text{switching step}} \quad (3)$$

t_{SW} : switching time (sec)
f_N : natural frequency of the 2nd order system(Hz), $\omega_N = 2\pi f_N$ (rad/s)
N : total divide ratio
ξ : damping factor of the 2nd order system. Typical value is 0.707.
K_{VCO}: VCO gain (Hz/V) or 2π * VCO gain (rad/V)
K_ϕ : phase detector gain = $I_{CP}/2\pi$ (A/rad)

$$\omega_N = \frac{-\ln(\delta \cdot \sqrt{1 - \xi^2})}{\xi \cdot t_{SW}} \quad (4)$$

$$C_1 = \frac{K_\phi \cdot K_{VCO}}{N\omega_N^2} \quad (5)$$

$$R_1 = 2 \cdot \xi \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C_1}\right)^{0.5} \quad (6)$$

$$C_2 \le \frac{C_1}{10} \quad (7)$$

$$\omega = \frac{1}{C_3 \cdot R_2} \quad \omega \text{ should be at least 10 times larger than } \omega_N \quad (8)$$

Note: The unit of the factor $K_\phi \cdot K_{VCO}$ is unity when all the variables are expressed in radians. Therefore, designers can simply multiply the charge pump output current (I_{CP}) with the VCO gain in Hz/V to obtain this factor.

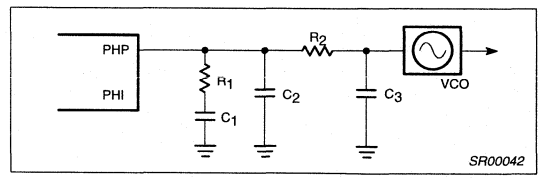


Figure 1. 3-Poles RC Lowpass Loop Filter

SA7025 (RevA) Design Example

This section shows a design example using the SA7025 (RevA) for the IS-54. The system parameters are as follows:

VCO frequency (f_{VCO}) = 913 to 938MHz
Channel spacing (f_{CH}) = 30kHz
Comparison frequency (f_{COMP}) = 8 * 30 kHz = 240kHz
Switching time (t_{SW}) = 1.5ms
Switching step = 25MHz
Frequency error = within 1 kHz
VCO gain (K_{VCO}) = 12MHz/V (measured), Murata MQE001-926
Reference Crystal (f_{REF}) = 14.4MHz

1. Determine total divide ratio N

To synthesize channels from 913 to 938MHz with f_{COMP}=240kHz, N should be between 3804 and 3908. For the same loop components, a larger value of N yields lower natural frequency (f_N). So, jumping from high-end to low-end (larger N) is slower than from low-end to

high-end (smaller N). To ensure the same switching time from both directions, we use N=3908 for the worst case.

2. Determine ω_N

Using Eq. 3 $$\delta = \frac{1000}{25e6} = 0.04e\text{-}3$$

Pick $\xi = 0.707$ and use $t_{SW} = 1.5$ms.

Using Eq. 4 $$\omega_N = \frac{-\ln(0.04e\text{-}3 \cdot 0.707)}{0.707 \cdot 1500e\text{-}6} = 9830$$

3. Determine RN and I_{CP}

Pick RN = 51 kΩ and CN = 200. I_{RN} becomes 58μA when V_{DDA}=5V.

Using the PHP charge pump current equation

$$I_{CP} = 200\left(\frac{58e\text{-}6}{32}\right) = 363\mu A$$

4. Determine R_1, C_1, and C_2

Using Eq. 5 with the 2π's from K_{VCO} (rad/V) and K_ϕ (A/rad) cancel out

$$C_1 = 12e6\left(\frac{363e\text{-}6}{3908 \cdot 9830^2}\right) = 11.5nF$$

Using Eq. 6

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{3908}{12e6 \cdot 363e\text{-}6 \cdot 11.5e\text{-}9}\right)^{0.5} = 13k\Omega$$

Using Eq. 7 $$C_2 = \frac{11.5e\text{-}9}{10} = 1.15nF$$

5. Determine R_2 and C_3

R_2 and C_3 can help attenuate the comparison spurs at 240kHz offset.

Using Eq. 8 $$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_N$$

6. Determine RF

Crystal frequency (f_{XTAL}) = 14.4MHz
Mid VCO frequency (f_{VCO}) = 926MHz
Q (fractional modulus) = 8
Using Eq. 1 and Eq. 2

$$I_{RF} = \frac{3 \cdot 58e\text{-}6 \cdot 200 \cdot 14.4e6}{8 \cdot 926e6} = 67.65\mu A$$

$$RF = \frac{5 - 0.9 - 150 \cdot \sqrt{67.65e\text{-}6}}{8 \cdot 926e6} = 43k\Omega$$

A minor adjustment of CN maybe required if optimum fractional spurs suppression is needed across the 25MHz band. The experimental results yielded the best spurious suppression at a value of RF=47kΩ.

Component values used on the SA7025(Rev A) demo board:
C31 = 10 nF
R23 = 13 kΩ
C32 = 1 nF
R24 = 100 kΩ
C33 = 18 pF
R21 = 47 kΩ (RF)
R22 = 51 kΩ (RN)
CN = 200
Strobe width = 260μs

Measurement Results of the SA7025 (RevA)

Figure 2 shows the measured close-in noise at 940.05MHz. The phase noise at 1kHz carrier offset is -49.4 - 10 * log (100) = -69.4 dBc/Hz. Fractional spurs performance is shown in Figures 3 to 6. The worst case spurs occur when NF=1 and NF=7 are less than -60dBc. Spurs at the alternate channel, the 60kHz carrier offset required by the IS-54, are totally suppressed. Figures 7 and 8 show the measured switching times. These results show that the PLL can jump a 25MHz step in less than 1.5ms from both directions.

Table 2 shows the difference in performance between the SA7025 and SA7025 (RevA) using the same demoboard. Unless otherwise mentioned, CN=200, RN=51kΩ, RF=47kΩ.

Speed-up Design for Achieving Better Close-in Noise

Better close-in noise can be achieved at the expense of operational current. The PHP charge pumps on the SA7025 (RevA) and SA8025A are both capable of delivering more than 1.5mA in the speed-up mode. To stay in this mode, the STROBE signal has to be kept high after the programming word 'A' is sent. The CL register sets the amount of charge pump current which is either 3 times (CL=0), 5 times (CL=1), or 9 times (CL=2) higher than the current in normal mode. Assume that we want to modify the previous design and use speed-up with CL=1. This implies that the charge pump output current becomes 5*363μA = 1.8mA. In order to maintain the same natural frequency, the value of C31 and C32 is increased by a factor of 5 and R23 is decreased by the same factor of 5. Therefore, the new values used on the demo board are:

C31 = 100nF in parallel with 100nF
C32 = 4.7nF
R23 = 2.4kΩ

Figure 9 compares the close-in phase noise of the two designs with the same natural frequency. The bottom trace has a 4dB improvement in the close-in noise when speed-up mode (higher current) is used. Since the phase noise beyond the loop bandwidth is solely determined by the VCO phase noise, two traces start to merge together at about 5kHz offset.

SA8025A Design Example

This section shows a design example using the SA8025A for the Personal Digital System (PDC1500), a narrow band system. The design procedure is the same as the previous section. The system parameters are as follows:

VCO frequency (f_{VCO}) = 1607 to 1631 MHz
Channel spacing (f_{CH}) = 25kHz
Comparison frequency (f_{COMP}) = 8 * 25kHz = 200kHz
Switching time (t_{SW}) = 1.5ms
Switching step = 24MHz
Frequency error = within 1kHz
VCO gain (K_{VCO}) = 24 MHz/V (measured), Murata MQE060-1619
Reference Crystal (f_{REF}) = 19.2MHz

Table 2. Performance Comparison: SA7025 to SA7025 (Rev A)

	SA7025	SA7025 (Rev A)	Figure
Fractional spurs (dBc) @30kHz, VCO=912.99MHz	-57.6 (CN=200, RF=2MΩ)	-63.6	3
Fractional spurs (dBc) @60kHz, VCO=912.99MHz	not present (CN=200, RF=2MΩ)	not present	3
Fractional spurs (dBc) @30kHz, VCO=939.87MHz	-63.5 (CN=100, RF=2MΩ)	-63.9	5
Fractional spurs (dBc) @60kHz, VCO=939.87MHz	not present (CN=100, RF=2MΩ)	not present	5
Close-in noise (dBc/Hz) @1kHz, VCO=1631.025MHz	-69	-69	2
I_{TOTAL} (mA) for the demo board	21.2	21.2	
Switching time (ms)	<1.5	<1.5	7, 8

1. Determine total divide ratio N

$$N = \frac{1631MHz}{200kHz} = 8155$$

2. Determine ω_N

Using Eq. 3 $$\delta = \frac{1000}{24e6} = 0.042e\text{-}3$$

Pick $\xi = 0.707$ and use $t_{SW} = 1.5ms$.

Using Eq. 4 $$\omega_N = \frac{-\ln(0.042e\text{-}3 \cdot 0.707)}{0.707 \cdot 1500e\text{-}6} = 9830$$

3. Determine R_N and I_{CP}

Pick RN = 51kΩ and CN = 200. I_{RN} becomes 58μA when V_{DDA}=5V.

Using the PHP charge pump current equation

$$I_{CP} = 200\left(\frac{58e\text{-}6}{32}\right) = 363\mu A$$

4. Determine R_1, C_1, and C_2

Using Eq. 5

$$C_1 = 24e6\left(\frac{363e\text{-}6}{8155 \cdot 9830^2}\right) = 11.1nF$$

Using Eq. 6

$$R_1 = 2 \cdot 0.707 \cdot \sqrt{\left(\frac{8155}{24e6 \cdot 363e\text{-}6 \cdot 11.1e\text{-}9}\right)} = 13k\Omega$$

Using Eq. 7 $$C_2 = \frac{11.1e\text{-}9}{10} = 1.1nF$$

5. Determine R_2 and C_3

R_2 and C_3 can help attenuate the comparison spurs at 200kHz offset.

Using Eq. 8 $$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_N$$

Pick $R_2 = 360k\Omega$, then $C_3 = 18pF$.

6. Determine RF

Crystal frequency (f_{XTAL}) = 19.2MHz
Mid VCO frequency (f_{VCO}) = 1619MHz
Q (fractional modulus) = 8
Using Eq. 1 and Eq. 2

$$I_{RF} = \frac{3 \cdot 58e\text{-}6 \cdot 200 \cdot 14.4e6}{8 \cdot 926e6} = 67.65\mu A$$

$$RF = \frac{5 - 0.9 - 150 \cdot \sqrt{67.65e\text{-}6}}{8 \cdot 926e6} = 43k\Omega$$

Minor adjustment of CN is required if optimum fractional spurs suppression is needed.

Component values used on the demo board:
C31 = 10nF
R23 = 13kΩ
C32 = 1nF
R24 = 360kΩ
C33 = 18pF
R21 = 56kΩ (RF)
R22 = 51kΩ (RN)
CN = 200
Strobe width = 260μs

Measurement Results of the SA8025A

Close-in phase noise spectrum is shown in the Figure 10. At 1kHz carrier offset, the phase noise is -45.3 - 10*log (100) = -65.3 dBc/Hz. The 3dB loop bandwidth is 3kHz, which is about twice as much as the loop natural frequency (f_N). Fractional spurs performance is shown in Figure 11 to 14. Worst case spurs when NF=1 and NF=7 for the low and high bands are all less than -59dBc. Spurs at 50kHz carrier offset, the alternate channel for PDC1500, were totally suppressed. Switching time measurements are shown in Figure 15 and 16. The PLL can reach the desired frequency for a 24MHz jump in less than 1.5ms from both directions.

Table 3 shows the difference in performance between the SA8025 and SA8025A using the same demoboard. Unless otherwise mentioned, CN=200, RN=51kΩ, RF=56kΩ.

Table 3. Performance Comparison: SA8025 to SA8025A

	SA8025	SA8025A	Figure
Fractional spurs (dBc) @25kHz, VCO=1606.625MHz	-41.5 (CN=250, RF=560kΩ)	-60.6	11
Fractional spurs (dBc) @50kHz, VCO=1606.625MHz	not present (CN=250, RF=560kΩ)	not present	11
Fractional spurs (dBc) @25kHz, VCO=1631.025MHz	-59.0 (CN=200, RF=560kΩ)	-59.5	13
Fractional spurs (dBc) @50kHz, VCO=1631.025MHz	not present (CN=200, RF=560kΩ)	not present	13
Close-in noise (dBc/Hz) @1kHz, VCO=1631.025MHz	-65	-65	10
I_{TOTAL} (mA) for the demo board	28.3	28.3	
Switching time (ms)	<1.5	<1.5	15, 16

SA8025A for the PHS System

Philips Semiconductors applications note AN1891, "Using the SA8025 in 2GHz band applications", shows a design for the PHS system based on the SA8025. If the SA8025A is used in the same design, only RF needs to be changed.

Crystal frequency (f_{XTAL}) = 19.2MHz
Mid VCO frequency (f_{VCO}) = 1665MHz
Q (fractional modulus) = 8
I_{RN} = 80μA
CN = 100
Using Eq. 1 and Eq. 2

$$I_{RF} = \frac{3 \cdot 80e\text{-}6 \cdot 100 \cdot 19.2e6}{8 \cdot 1865e6} = 34.6\mu A$$

$$RF = \frac{3 - 0.9 - 150 \cdot \sqrt{34.6e\text{-}6}}{34.6e\text{-}6} = 35.2k\Omega$$

On the demo board, RF=36kΩ was used. The measured fractional spurs when NF=1 and NF=7 are both better than -70dBc.

Table 4 summarizes the components change for the SA7025/SA8025 and the SA7025 (RevA)/SA8025A demo boards.

Table 4. Summary of Component Changes

Component	SA7025	SA7025 (Rev A)	SA8025	SA8025A
R21	560kΩ	47kΩ	560kΩ	36kΩ
R22	33kΩ	51kΩ	10kΩ	10kΩ
R23	24kΩ	13kΩ	10kΩ	10kΩ
R24	22kΩ	100kΩ	18kΩ	18kΩ
R25	22kΩ	0Ω	0Ω	0Ω
C30	330pF	NL	NL	NL
C31	3.3nF	10nF	3.9nF	3.9nF
C32	220pF	1nF	390pF	390pF
C33	220pF	18pF	150pF	150pF
C34	100pF	NL	NL	NL
NL = Not Loaded				

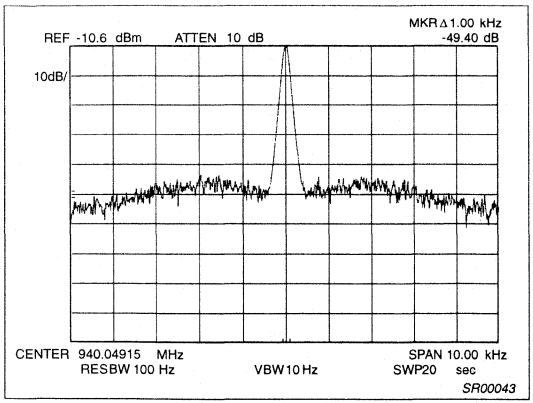


Figure 2. Close-In Noise at 940.05MHz

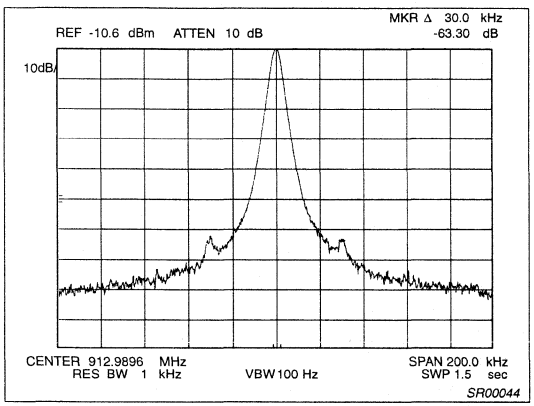


Figure 3. Fractional Spurs, (f_{VCO} = 912.99MHz; NF = 1)

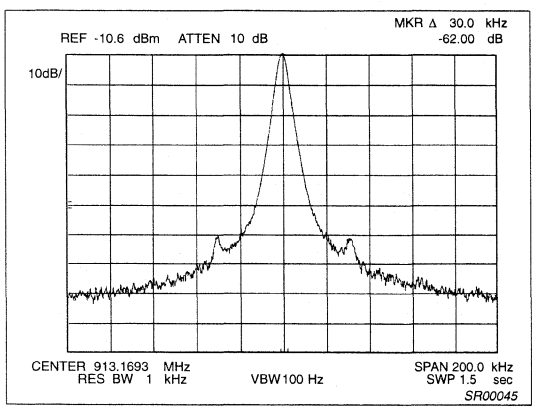


Figure 4. Fractional Spurs, (f_{VCO} = 913.17MHz; NF = 7)

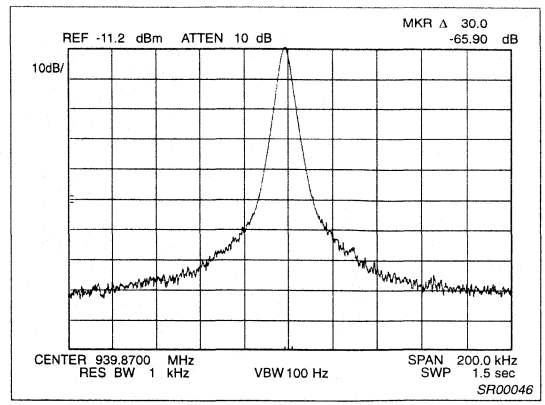


Figure 5. Fractional Spurs, (f_{VCO} = 939.87MHz; NF = 1)

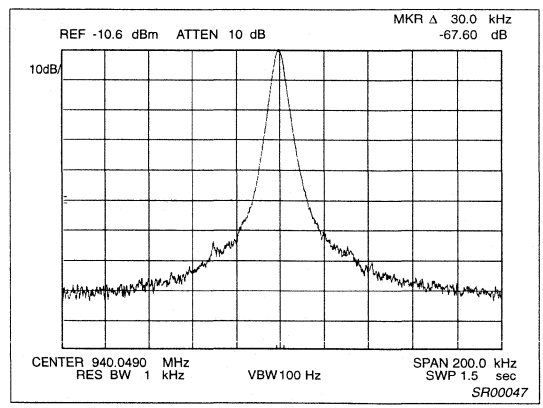


Figure 6. Fractional Spurs, (f_{VCO} = 940.05MHz; NF = 7)

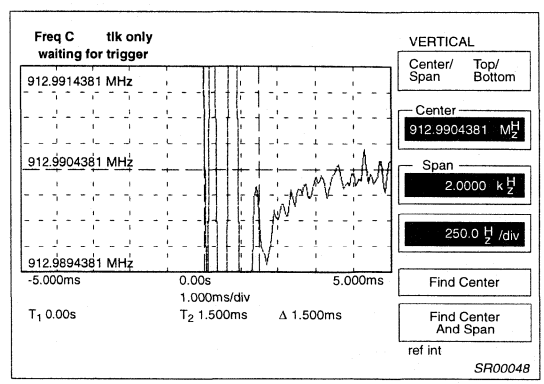


Figure 7. Switching Time (939.87 to 912.99MHz Step to Within 1kHz)

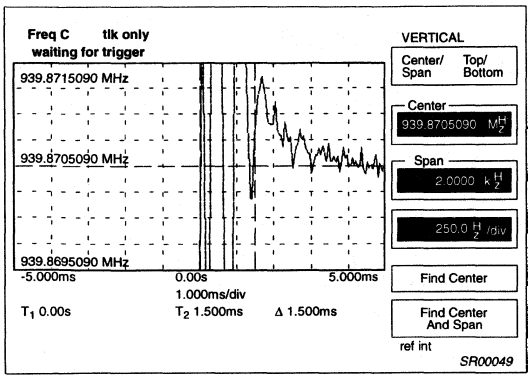


Figure 8. Switching Time (912.99 to 939.87MHz Step to Within 1kHz)

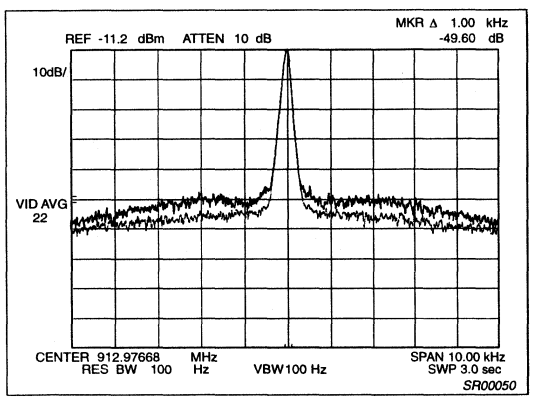


Figure 9. Close-In Phase Noise When CL = 1

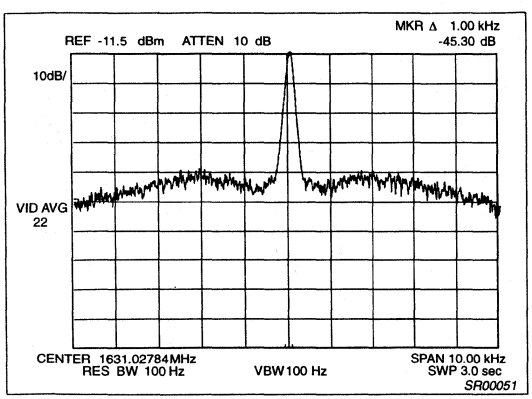


Figure 10. Close-In Phase Noise at 1631.025MHz

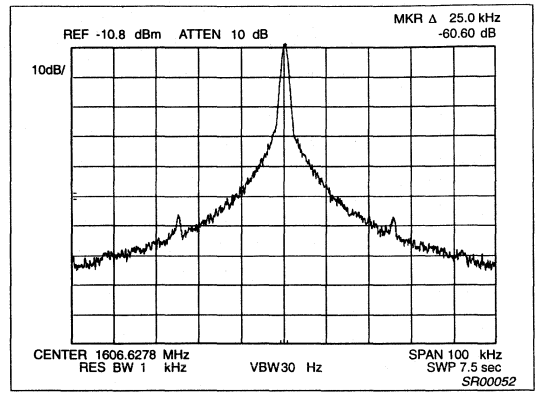


Figure 11. Fractional Spurs, (f_{VCO} = 1606.625MHz; NF = 1)

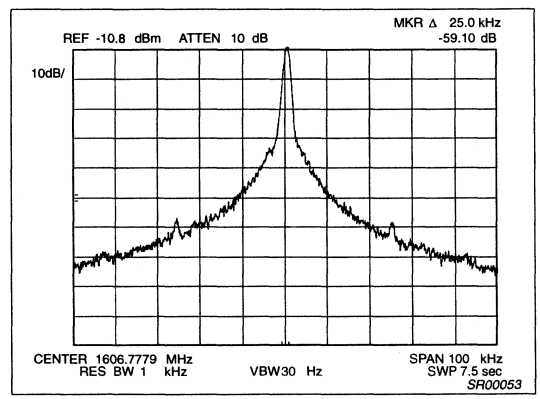


Figure 12. Fractional Spurs, (f_{VCO} = 1606.775MHz; NF = 7)

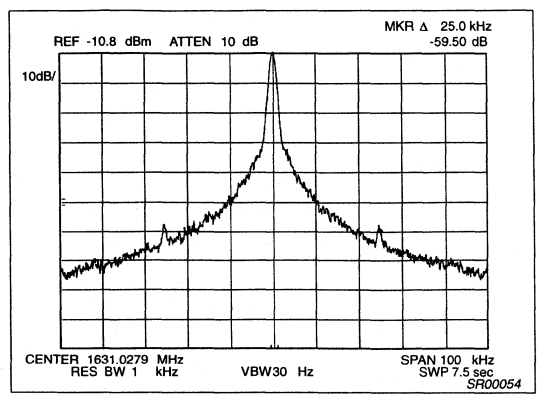


Figure 13. Fractional Spurs, (f_{VCO} = 1606.775MHz; NF = 7)

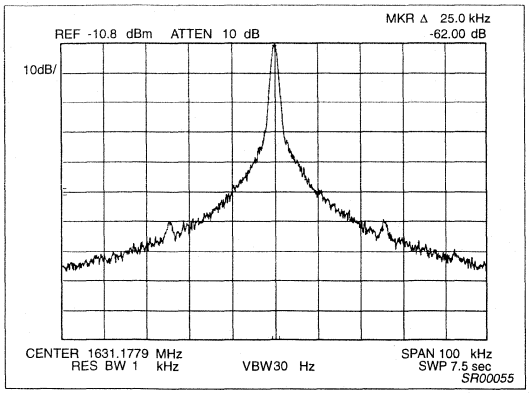


Figure 14. Fractional Spurs, (f_{VCO} = 1631.175MHz; NF = 7)

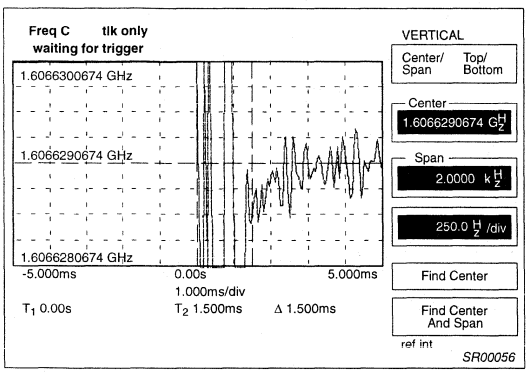


Figure 15. Switching Time (1631.025 to 1606.625MHz Step to Within 1kHz)

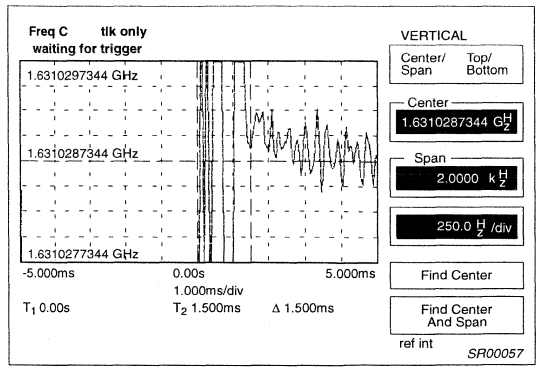


Figure 16. Switching Time (1606.625 to 1631.025MHz Step to Within 1kHz)

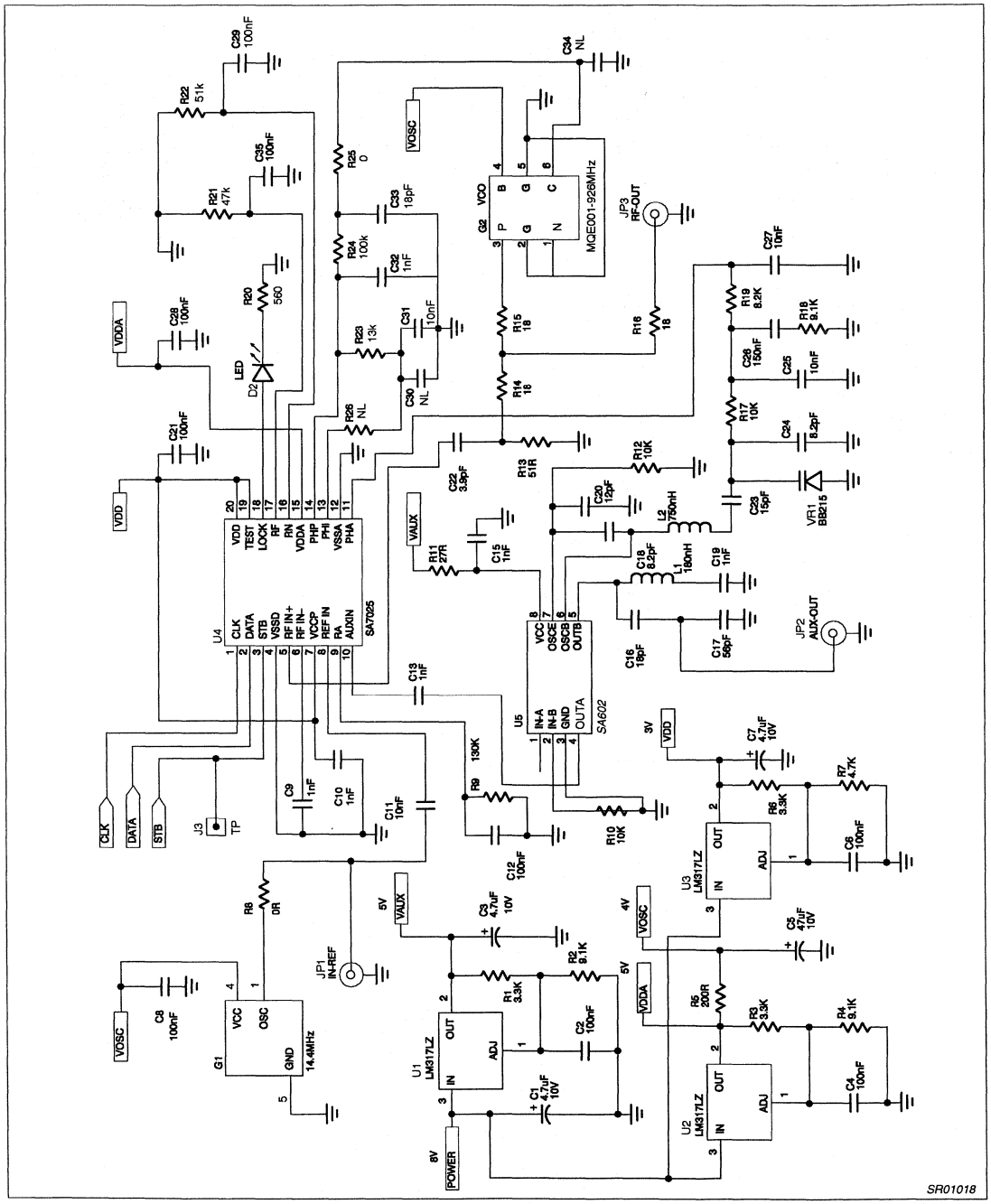


Figure 17. SA7025DK Application Circuit

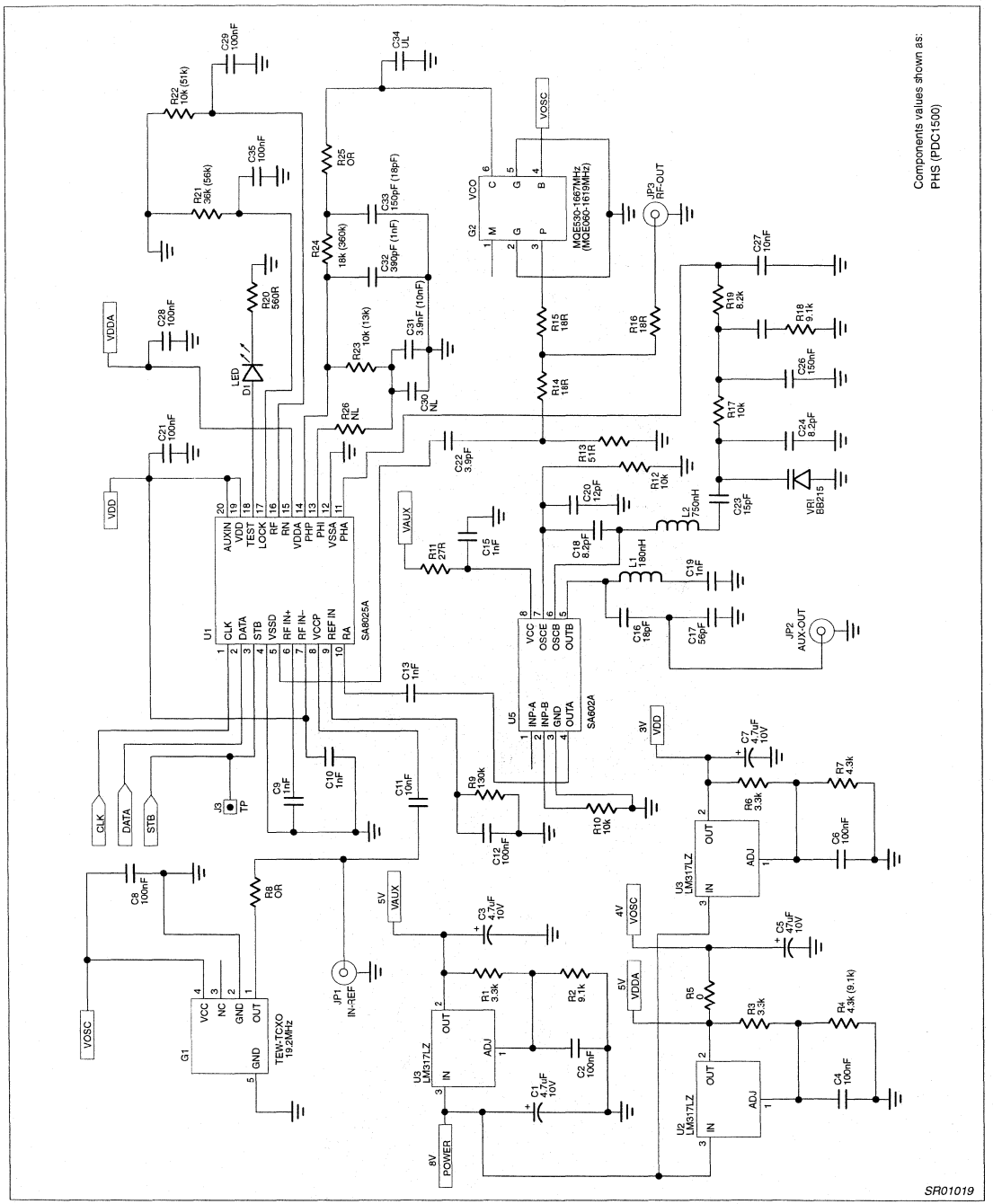
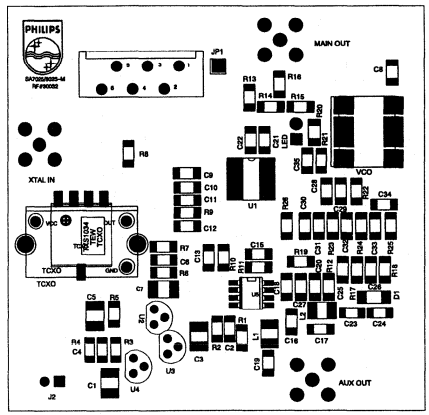
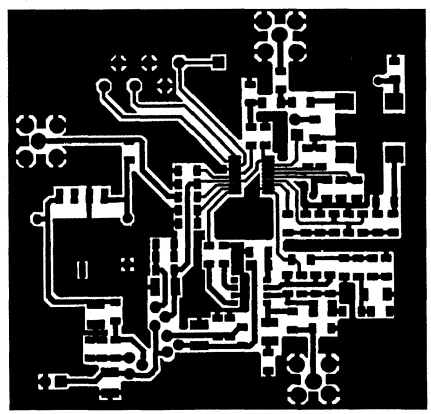


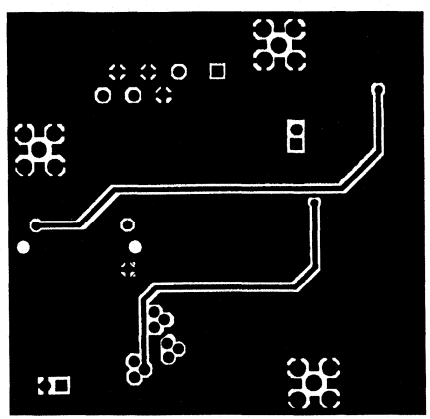
Figure 18. SA8025ADK Application Circuit



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

SR01020

Figure 19. SA8025ADK Demoboard Layout (NOT ACTUAL SIZE)

Table 5. Customer Application Component List for SA7025DK

Qty.	Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	3.9pF	50V	C22	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A3R9CK
2	8.2pF	50V	C24, C18	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A8R2CK
1	12pF	50V	C20	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A120JK
1	15pF	50V	C23	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A150JK
2	18pF	50V	C16, C33	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A180JK
1	56pF	50V	C17	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A560JK
6	1000pF	50V	C9, C10, C13, C15, C19, C32	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315A102JP
4	0.01µF	50V	C11, C25, C27, C31	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C103KK
9	0.1µF	50V	C2, C4, C6, C8, C12, C21, C28, C29, C35	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C104KP
1	0.15µF	16V	C26	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C154KP
4	4.7µF	10V	C1, C3, C5, C7	Tant. chip cap. A 3216 ±10%	Garrett	Philips	49MC475B010KOAS
Surface Mount Resistors							
2	0Ω	50V	R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
3	18Ω	50V	R14, R15, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW180E
1	27Ω	50V	R11	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW270E
1	51Ω	50V	R13	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW510E
1	100Ω	50V	R5	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW101E
1	560Ω	50V	R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
3	3.3kΩ	50V	R1, R3, R6	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW332E
1	4.7kΩ	50V	R7	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW472E
1	8.2kΩ	50V	R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW822E
3	9.1kΩ	50V	R2, R18, R4	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW912E
3	10kΩ	50V	R10, R12, R17	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW103E
1	13kΩ	50V	R23	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW133E
1	47kΩ	50V	R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW473E
1	51kΩ	50V	R22	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW513E
1	100kΩ	50V	R24	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW104E
1	130kΩ	50V	R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW134E
1	560kΩ	50V	R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW564E
Surface Mount Diodes							
1			VR1 (Varactor)	Variable capacitance SMD diode	Digikey	Philips	BB215
1			D1	SM Led	Digikey		
Surface Mount Inductors							
1	0.18µH		L1	Chip inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-181XKBB
1	0.75µH		L2	Chip inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-751XKBB
Voltage Regulators							
3	100mA		U1, U2, U3	Voltage regulator	Digikey	National	LM317LZ
TCXO							
1	14.4MHz		G1	Temp. controlled crystal osc.	TEW	TEW	TXS0924M-14.4MHz
VCO							
1	926MHz		G2	Voltage controlled osc.	Murata	Murata Erie	MQE001-926
Surface Mount Integrated Circuits							
1			U4	1GHz Fractional-N Synthesizer	Philips	Philips	SA7025DK
1			U5	Double Balanced Mixer Oscillator	Philips	Philips	SA602A
Miscellaneous							
3			JP1, JP2, JP3	SMA right angle jack receptacle	Newark	EF Johnson	142-0701-301
1			J1	Male 6-pins connector	STOCKO	STOCKO	MKS1956-6-0-606
1			J2	Male 2-pins connector	STOCKO	STOCKO	MKS1851-6-0-202
1			J3	Test point	Digikey	3M	929647-36
1				Printed circuit board	Philips	Philips	SA7025/8025-M
75 Total Parts							

Table 6. Customer Application Component List for SA8025ADK

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	3.9pF	50V	C22	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A3R9CK
2	8.2pF	50V	C24, C18	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A8R2CK
1	12pF	50V	C20	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A120JK
1	15pF	50V	C23	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A150JK
1	18pF	50V	C16	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A180JK
1	56pF	50V	C17	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A560JK
1	150pF	50V	C33	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A151JK
1	390pF	50V	C32	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A391JK
5	1000pF	50V	C9, C10, C13, C15, C19	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315A102JP
1	3900pF	50V	C31	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C392KK
3	0.01µF	50V	C11, C25, C27	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C103KK
9	0.1µF	50V	C2, C4, C6, C8, C12, C21, C28, C29, C35	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C104KP
1	0.15µF	16V	C26	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C154KP
4	4.7µF	10V	C1, C3, C5, C7	Tant. chip cap. A 3216 ±10%	Garrett	Philips	49MC475B010KOAS
Surface Mount Resistors							
3	0Ω	50V	R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
3	18Ω	50V	R14, R15, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW180E
1	27Ω	50V	R11	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW270E
1	51Ω	50V	R13	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW510E
1	560Ω	50V	R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
3	3.3kΩ	50V	R1, R3, R6	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW332E
2	4.3kΩ	50V	R4, R7	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW432E
1	8.2kΩ	50V	R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW822E
2	9.1kΩ	50V	R2, R18	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW912E
5	10kΩ	50V	R10, R12, R17, R22, R23	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW103E
1	18kΩ	50V	R24	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW183E
1	36kΩ	50V	R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW364E
1	130kΩ	50V	R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW134E
Surface Mount Diodes							
1			VR1 (Varactor)	Variable capacitance SMD diode	Digikey	Philips	BB215
1			D1	SM Led	Digikey		
Surface Mount Inductors							
1	0.18µH		L1	Chip inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-181XKBB
1	0.75µH		L2	Chip inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-751XKBB
Voltage Regulators							
3	100mA		U1, U2, U3	Voltage regulator	Digikey	National	LM317LZ
TCXO							
1	19.2MHz		G1	Temp. controlled crystal osc.	TEW	TEW	TXS1034N-19.2MHz
VCO							
1	1667MHz		G2	Voltage controlled osc.	Murata	Murata Erie	MQE530-1667
Surface Mount Integrated Circuits							
1			U4	2GHz Fractional-N Synthesizer	Philips	Philips	SA8025ADK
1			U5	Double Balanced Mixer Oscillator	Philips	Philips	SA602A
Miscellaneous							
3			JP1, JP2, JP3	SMA right angle jack receptacle	Newark	EF Johnson	142-0701-301
1			J1	Male 6-pins connector	STOCKO	STOCKO	MKS1956-6-0-606
1			J2	Male 2-pins connector	STOCKO	STOCKO	MKS1851-6-0-202
1			T3	Test point	Digikey	3M	929647-36
1				Printed circuit board	Philips	Philips	SA7025/8025-M
75 Total Parts							

SA8025 Fractional-N synthesizer for 2GHz band applications AN1891

Author: Wing S. Djen

INTRODUCTION

The SA8025 is a 3V, 1.8GHz, SSOP 20-pin packaged fractional-N phase locked-loop (PLL) frequency synthesizer. It is targeted for systems like the Japan Personal Handy Phone System (PHS, formerly PHP) which demands fast switching time and good noise performance. Built on the QUBiC BiCMOS process, it has phase detectors with maximum frequency of 5MHz and an auxiliary synthesizer that can operate up to 150MHz. This design was based on the UMA1005 (all CMOS), an earlier version fractional-N synthesizer which requires an external prescaler for 1 and 2GHz applications. There is also a 1GHz version fractional-N PLL frequency synthesizer, the SA7025, available for systems operating under 1GHz. One should expect the performance of the SA8025 and SA7025 to be comparable to the UMA1005 with an extra prescaler. This application note will serve as a supplement to the application note for the UMA1005 (Report No: SCO/AN92002) or as a stand-alone document specifically for the SA8025.

OVERVIEW OF THE FRACTIONAL-N FREQUENCY SYNTHESIZER

Figure 1 shows the basic building blocks of a PLL frequency synthesizer. It consists of a programmable reference divider, phase detector and programmable RF divider (prescaler and main divider). The low-pass filter and voltage-controlled oscillator (VCO) are external to provide design flexibility. The loop has a self-correction mechanism which forces comparison frequency $f_{COMP} = f_{COMP'}$. Since $f_{COMP} = f_{REF}/M$ and $f_{COMP'} = f_{VCO}/N$, the desired frequency becomes $f_{VCO} = (f_{REF}/M)N$. M (reference divider) is fixed for generating f_{COMP}. By incrementing or decrementing the value of N, different frequencies can be synthesized.

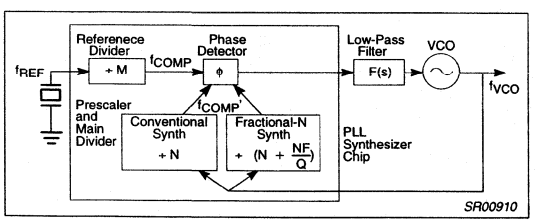


Figure 1. PLL Synthesizer

For conventional synthesizers, the phase detector comparison frequency must be equal to the channel spacing (frequency resolution) because the main divider (N) can only increment and decrement in integer steps. However, the main divider of the fractional-N synthesizer is capable of generating steps to be a fraction of the comparison frequency. Now the total divider ratio consists of an integer part (N) and a fractional part (NF/Q). The numerator (NF) and the denominator (Q, either 5 or 8) of a fraction are controlled through software programming.

Referring to Figure 2, to synthesize channels 1680MHz, 1680.3MHz and 1680.6MHz with channel spacing of 300kHz, the values have to be 5600MHz, 5601MHz and 5602MHz, respectively. The channel spacing of a fractional-N synthesizer is a fraction of the comparison frequency. When using the SA8025, the comparison frequency is increased to either 1.5MHz (mod 5) or 2.4MHz (mod 8), yielding a smaller N value of 1120 (mod 5) or 700 (mod 8) to synthesize 1680MHz.

The advantage of fractional-N synthesizers is two-fold. Since the close-in noise floor is directly related to total divide ratio (N), reducing N five or eight times theoretically implies a close-in noise floor improvement of 14dB (20log(5)) or 18dB (20log(8)), respectively. At the same time, the comparison breakthrough will be 5 or 8 times further away than it would be if a conventional synthesizer were used. This allows a wider loop filter to be used, thus achieving a faster switching time. Faster switching is also achieved due to the higher number of comparison cycles.

To synthesize 1680, 1680.3, 1680.6MHz with channel spacing = 300kHz

Conventional syn. $f_{VCO} = f_{COMP}$ (N)	SA8025 (mod 5) $f_{VCO} = f_{COMP}$ (N + NF/5)	SA8025 (mod 8) $f_{VCO} = f_{COMP}$ (N + NF/8)
1680 = 0.3 (5600)	1680 = 1.5 (1120 + 0/5)	1680 = 2.4 (700 + 0/8)
1680.3 = 0.3 (5601)	1680.3 = 1.5 (1120 + 1/5)	1680.3 = 2.4 (700 + 1/8)
1680.6 = 0.3 (5602)	1680.6 = 1.5 (1120 + 2/5)	1680.6 = 2.4 (700 + 2/8)
f_{COMP} = f_{CH} = 0.3MHz	f_{COMP} = 5 x f_{CH} = 1.5MHz	f_{COMP} = 8 x f_{CH} = 2.4MHz

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Figure 2. What Is Fractional-N?

DESIGNING WITH THE SA8025

Reference Signal and Divider

Since the synthesized signal is derived from the reference signal, using a clean crystal with an appropriate level is crucial. The reference signal should be AC coupled and deliver between 300 and $600mV_{P-P}$ to Pin 8 for the input buffer to convert it into a CMOS compatible level. The maximum crystal frequency the part can handle is determined by both analog and digital supplies because the input buffer and the reference divider are powered by V_{DDA} and V_{DD}, respectively. For a $V_{DD} = V_{DDA} = 3V$ configuration, the maximum crystal frequency allowed is 20MHz. When $V_{DD} = 3V$ and $V_{DDA} = 5V$, this frequency becomes 30MHz.

Phase Detector and Charge Pumps

The main and auxiliary phase detectors (see Figure 3) detect both the phase and frequency difference between the divided-down VCO and reference signals. If the main/aux leads the reference, there will be a pulse coming out of the phase detector which turns on the N-type charge pump and sinks current from the low-pass filter. On the other hand, if the main/aux lags the reference, the P-type charge pump will be activated and more current will be delivered to the low-pass filter.

Due to the internal delays of CMOS devices, the phase comparator needs a minimum phase difference, backlash time, to generate an output pulse. This backlash time will introduce a dead-zone around zero phase difference where a small phase error cannot be detected. The way the SA8025 eliminates this problem is by having a minimum on-time of $1/f_{REF}$ for the P pump (sourcing) and N pump (sinking) when the loop is in lock condition, which is shown in Figure 4. Since the charge pump on-time is determined by the crystal reference frequency (f_{REF}), the higher the frequency, the better will be the close-in noise performance. Typically, there will be 3dB close-in noise improvement for a 50% increase in reference frequency (e.g., from 9.6 to 14.4MHz).

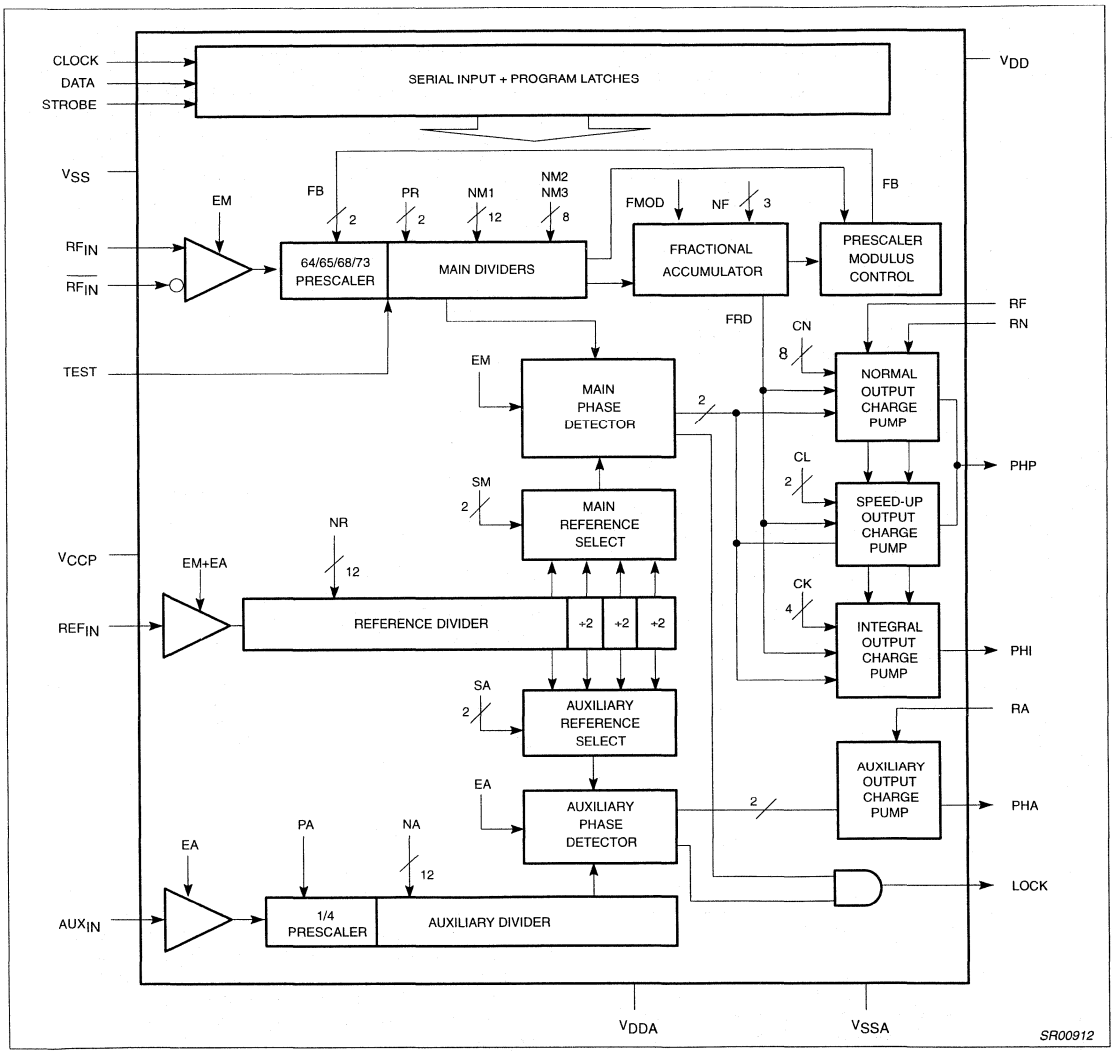

Figure 3. Block Diagram of the SA8025

Since the phase detector detects phase from -2π to 2π, its gain (K_Φ) equals the charge pump output current (I_{CP}) divided by 2π with units of A/rad.

The charge pump output current, I_{CP} (A), is determined by the external resistor RN and the internal registers CN, CK and CL values. The I_{CP} for normal mode operation (PHP pump only) is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} \quad \text{(EQ. 1)}$$

where

$$RN = \frac{V_{DDA} - 0.9 - 150(I_{RN})^{0.5}}{I_{RN}} \quad \text{(EQ. 2)}$$

Figure 5 shows a graphical representation of Eq. 2. The curves are valid for both main and aux synthesizers. Notice that in normal mode, currents due to the CK and CL values are negligible and only the PHP pump is activated. When the part is in speed-up, both charge pumps are on and the I_{CP} for PHP is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} (2^{CL+1} + 1) \quad \text{(EQ. 3)}$$

I_{CP} for PHI is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} (2^{CL+1}) \, CK \quad \text{(EQ. 4)}$$

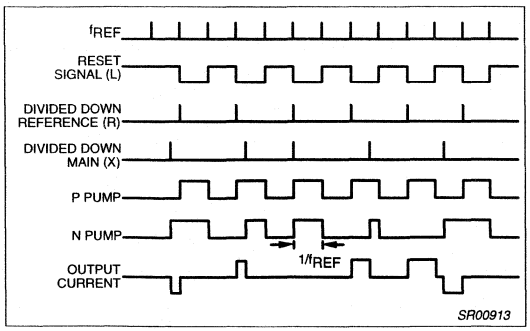

Figure 4. Phase Detector Timing Diagram

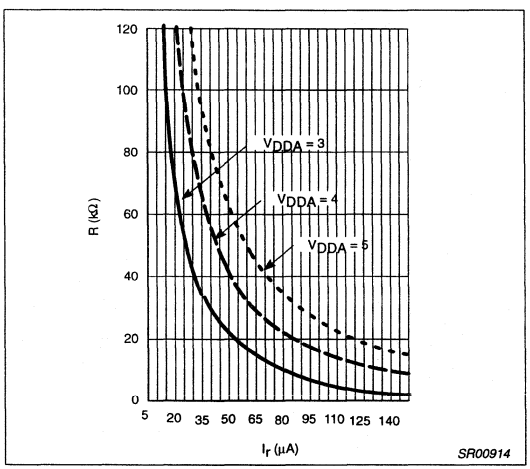

Figure 5. RN(RA) vs. $I_{RN}(I_{RA})$ for Different V_{DDA}

From Eq. 3 notice that in speed-up mode, the PHP output current will be at least 3 times higher than the normal mode current even though CL=0. Speed-up mode stays active as long as the STROBE signal is high after an A word is sent.

Bypass capacitors (100nF) should be used for RN, RF and RA pins to prevent high frequency noise being coupled into the pins causing modulation of the VCO.

Main Divider

The total divide ratio, N, is determined by the combination of the main divider ratio (NM1, NM2, NM3, NM4) and the prescaler values. The part is internally controlled to produce division ratios of N or N+1 when a fractional function is used. The minimum divide ratio, N', which guarantees that all the channels above this ratio can be synthesized consecutively (no blind channels) is different for each prescaler ratio. Since the fractional-N synthesizer increases the comparison frequency, lower N values can be used. To accomplish this, the SA8025 uses a 4 modulus (64/65/68/73) prescaler that lowers the minimum divide ratio to 933.

When programming a total divide ratio (N) which has no components of NM3 or NM4, simply treat them as "don't cares".

Using divide ratios below the minimum divide ratio (N') to synthesize channels is possible, but it requires trial and error. For instance, in the Japan Personal Handy Phone System (PHS), the VCO is running at 1646.7 to 1670.1MHz (248.45MHz first IF). Using a modulus 8 fraction with 300kHz channel spacing, the required N value is between 686 and 695, which is less than the N' of the 4 modulus prescaler. Calculation showed that only N = 695 is not obtainable using the 4 modulus prescaler, but it can be obtained using the 64/65/73 prescaler. The B word must be sent to change the prescaler ratio.

Table 1.

Prescaler Ratio	PR Bits	N'	Total Divide Ratio, N
64/65	01	4032	N = (NM1 + 2) × 64 + NM2 × 65
64/65/68	10	1348	N = (NM1 + 2) × 64 + NM2 × 65 + (NM3 + 1) × 68
64/65/68/73	11	933	N = (NM1 + 2) × 64 + NM2 × 65 + (NM3 + 1) × 68 + (NM4 + 1) × 73
64/65/73	00	1096	N = (NM1 + 2) × 64 + NM2 × 65 + (NM4 + 1) × 73

Determining the Programming Values for NM1, NM2, NM3 and NM4

For the 2-modulus prescaler (64/65), NM1 and NM2 can be determined by:

$$NM2 = 64 \cdot FRAC\left(\frac{N}{64}\right) \quad \text{(EQ. 5)}$$

$$NM1 = INT\left(\frac{N}{64}\right) - NM2 - 2 \quad \text{(EQ. 6)}$$

where FRAC (...) and INT (...) takes the fractional integer part of the argument.

For the 3-modulus prescaler, NM1, NM2 and NM3 (NM4 when PR = 00) can be determined by:

$$K1 = INT\left(\frac{N-R}{64}\right) - 3, \quad K2 = FRAC\left(\frac{N-R}{64}\right) \cdot 64 \quad \text{(EQ. 7)}$$

$$NM3 = INT\left(\frac{K2}{R}\right) \quad \text{(EQ. 8)}$$

$$NM2 = FRAC\left(\frac{K2}{R}\right) \cdot R \quad \text{(EQ. 9)}$$

$$NM1 = K1 - NM2 - NM3 \quad \text{(EQ. 10)}$$

where R = 4 for 64/65/68 prescaler, R = 9 for 64/65/73 prescaler.

For the 4-modulus prescaler (64/65/68/73), we first arbitrarily choose NM4 (smaller values are preferable) and then use the following formulas to calculate NM1, NM2 and NM3:

$$K1 = INT\left(\frac{N-13}{64}\right) - 4, \quad K2 = FRAC\left(\frac{N-13}{64}\right) \cdot 64 \quad \text{(EQ. 11)}$$

$$NM3 = INT\left(\frac{K2 - 9 \cdot NM4}{4}\right) \quad \text{(EQ. 12)}$$

$$NM2 = FRAC\left(\frac{K2 - 9 \cdot NM4}{4}\right) \cdot 4 \quad \text{(EQ. 13)}$$

$$NM1 = K1 - NM2 - NM3 - NM4 \quad \text{(EQ. 14)}$$

Notice that the formulas shown above will give only one set of NM1, NM2, NM3 and NM4 that generates the desired N value. Generating continuous N below 933 (4 modulus) is still possible if all

four modulus options are used. It was found that the part can generate N continuously from 702. The program "8025NMIN.EXE", provided with the "UMAWINE.EXE" for controlling the SA8025 demoboard, calculates all the N values that the part can generate. Users should run the program to find out the right NM1, NM2, NM3 and NM4 if N value of less than 702 is needed. This program will give only one possible combination of NM1 to NM4 for each N.

```
program sa8025
Philips Semiconductors, Sunnyvale, CA
Author: Wing S. Djen
Date: 5/9/94
Purpose: To find the minimum divide ratio on the SA8025

integer i, n1, n2, n3, n4, mod2, mod3a, mod3b, mod4,
+        delta1, delta2, delta3, delta4,
+        temp2, temp3a, temp3b, temp4
+        lown, highn

write(*,*) 'Enter the lowest N value→'
read(*,*) lown
write(*,*) 'Enter the highest N value→'
read(*,*) highn
do 10 i=lown, highn
do 10 n1=0,10
do 10 n2=0,10
do 10 n3=0,10
do 10 n4=0,10
   mod2 = (n1+2)*64 + n2*65
   mod3a = (n1+2)*64 + n2*65 + (n3+1)*68
   mod3b = (n1+2)*64 + n2*65 + (n4+1)*73
   mod4 = (n1+2)*64 + n2*65 + (n3 + 1)*68 + (n4+1)*73
  delta1 = i-mod2
  delta2 = i-mod3a
  delta3 = i-mod3b
  delta4 = i-mod4
  if (delta1.eq.0) then
    if (temp2.eq.mod2) goto 1
    write(*,5) mod2, n1, n2
5   format(' PR="01" N=',i5,3x,'NM1',i2,3x,
+             'NM2=',i2)
    temp2=mod2
    endif
1   if (delta2.eq.0) then
    if (temp3a.eq.mod3a) goto 2
    write(*,6) mod3a, n1, n2, n3
6   format(' PR="10" N=',i5,3x,'NM1',i2,3x,
+             'NM2=',i2,3x,'NM3=',i2)
    temp3a=mod3a
    endif
2   if (delta3.eq.0) then
    if (temp3b.eq.mod3b) goto 3
    write(*,7) mod3b, n1, n2, n4
7   format(' PR="00" N=',i5,3x,'NM1',i2,3x,
+             'NM2=',i2,3x,'NM4=',i2)
    temp3b=mod3b
    endif
3   if (delta4.eq.0) then
    if (temp4.eq.mod4) goto 10
    write(*,8) mod4, n1, n2, n3, n4
8   format(' PR="11" N=',i5,3x,'NM1',i2,3x,
+             'NM2=',i2,3x,'NM3=',i2,3x,'NM4=',i2)
    temp4=mod4
    endif
10  continue
    end
```

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The following is a sample output of the "8025NMIN.EXE" program. It shows the divide ratios that cover the PHS band.

PR="01"	N=128	NM1=0	NM2=0		
PR="01"	N=192	NM1=1	NM2=0		
PR="01"	N=193	NM1=0	NM2=1		
:	:	:	:		
:	:	:	:		
PR="11"	N=679	NM1=0	NM2=1	NM3=4	NM4=1
PR="00"	N=679	NM1=1	NM2=3	NM4=3	
PR="00"	N=680	NM1=0	NM2=4	NM4=3	
PR="11"	N=680	NM1=1	NM2=1	NM3=2	NM4=2
PR="11"	N=681	NM1=0	NM2=2	NM3=2	NM4=2
PR="11"	N=682	NM1=0	NM2=0	NM3=5	NM4=1
PR="11"	N=683	NM1=0	NM2=3	NM3=0	NM4=3
PR="11"	N=684	NM1=0	NM2=1	NM3=3	NM4=2
PR="11"	N=685	NM1=1	NM2=1	NM3=1	NM4=3
PR="00"	N=685	NM1=3	NM2=0	NM4=4	
PR="11"	N=686	NM1=0	NM2=2	NM3=1	NM4=3
PR="00"	N=686	NM1=2	NM2=1	NM4=4	
PR="11"	N=687	NM1=0	NM2=0	NM3=4	NM4=2
PR="00"	N=687	NM1=1	NM2=2	NM4=4	
PR="00"	N=688	NM1=0	NM2=3	NM4=4	
PR="11"	N=688	NM1=1	NM2=0	NM3=2	NM4=3
PR="11"	N=689	NM1=0	NM2=1	NM3=2	NM4=3
PR="11"	N=690	NM1=1	NM2=1	NM3=0	NM4=4
PR="11"	N=691	NM1=0	NM2=2	NM3=0	NM4=4
PR="11"	N=692	NM1=0	NM2=0	NM3=3	NM4=3
PR="11"	N=693	NM1=1	NM2=0	NM3=1	NM4=4
PR="11"	N=694	NM1=0	NM2=1	NM3=1	NM4=4
PR="00"	N=694	NM1=2	NM2=0	NM4=5	
PR="00"	N=695	NM1=1	NM2=1	NM4=5	
PR="00"	N=696	NM1=0	NM2=2	NM4=5	
PR="11"	N=697	NM1=0	NM2=0	NM3=2	NM4=4
PR="11"	N=698	NM1=1	NM2=0	NM3=0	NM4=5
PR="11"	N=699	NM1=0	NM2=1	NM3=0	NM4=5
PR="11"	N=702	NM1=0	NM2=0	NM3=1	NM4=5

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RF Inputs

The RF inputs were designed to be used differentially for better noise rejection. However, the part can also be driven single-endedly with $RF_{IN}+$ or $RF_{IN}-$ pin terminated by a 1nF capacitor. The matching network between VCO and RF input was intended for matching both the VCO and the Main Out on the demoboard to 50Ω (see Figure 6).

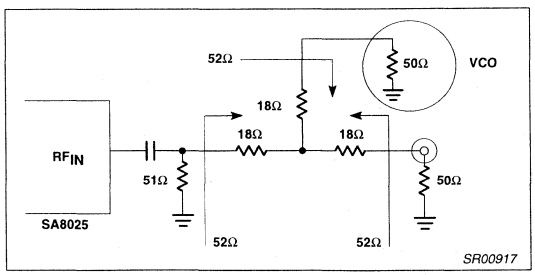

Figure 6. Matching Network for the RF_{IN} Pin

Lock Detect

The LOCK pin is selectable by software to be either the lock detect indicator, output of the main divider, output of the reference divider, or output of the auxiliary divider. Programming details can be found in the data sheet. The pin voltage will go to V_{DD} once the lock condition has been satisfied. Upon power up, the part is in an unknown state and the LOCK pin may go high. It will be functional only after the part is programmed.

Auxiliary Synthesizer

The auxiliary synthesizer does not have fractional-N capability. Therefore, its close-in phase noise and comparison breakthrough performance is comparable to that of a conventional synthesizer. However, this type of performance is not necessary for creating an offset frequency for a Frequency Division Duplex (FDD) system or the 2nd LO in a dual-conversion receiver. Also, an FM signal (e.g., GFSK or analog FM) can be obtained by directly frequency modulating the auxiliary VCO in a PLL structure. The auxiliary phase detector has the same bandwidth (5MHz) as the main phase detector. Current setting for the charge pump (I_{RA}) can be calculated using Eq. 2 and Figure 5. The charge pump output current (I_{CP}) becomes

$$I_{CP} = 8 \cdot I_{RA} \quad \text{(EQ. 15)}$$

Fractional Spurs and Compensation

The total divide ratio of the SA8025 is constantly changing between N and N + 1 to achieve fractional-N capability. This effect introduces an instantaneous phase error at the output of the phase detector in lock condition, which will cause the VCO to generate unwanted spurs at the fractions ($f_{VCO} \pm NF/Q$) of the comparison frequency (f_{COMP}). The SA8025 has internal circuitry which generates appropriate amounts of current to compensate for the phase error for different NF.

Due to the difference in processing technology, fractional compensation current on the SA8025 will not follow the UMA1005. Experimental results show that the resistor RF has to be between 200 and 600 kΩ for optimum fractional spur suppression. It is recommended to adjust the CN value for the high, the middle and the low channel to minimize the fractional spurs. Then linear interpolation technique can be applied to calculate all the CN values for the rest of the channels. A long "A" word (A1) needs to be sent to change the channel and set the CN value at the same time.

PCB Layout

Since careful PCB layout has a great impact on the performance of the synthesizer, users should pay special attention to the rules in building RF circuits. Here are some tips for the synthesizer board layout:

- Follow the layout in this document or on the demoboard.
- It is important that VCO ground is large in size and coupled immediately to the grounded side of the PCB. Make sure that there is a clean path for the VCO ground to get to the system ground (power supply ground).
- To avoid interference, the lead between the VCO output and the RF input should be kept as short as possible. A 50Ω termination resistor should be placed close to the RF input.
- Digital ground (V_{SS}) and analog ground (V_{SSA}) must be separated on the component side of the board. They have to be large in size on the PCB and coupled immediately to the grounded side of the PCB. Designers should refer to the latter part of this application note for the recommended PCB layout.
- Power supply bypass capacitors (100nF) for all devices should be located close to the devices with short leads.
- V_{SSA} should be separated from the ground of other devices such as VCO and mixer chip (SA602).

LOOP FILTER DESIGN

This section presents the procedure for designing the loop filter. Due to the sampling nature of the phase detector and the delay introduced in frequency dividers, complicated mathematical analysis is required for deriving the loop design formulas. However, to give designers a convenient tool for quick design, a simple design procedure based on linear control theory is given below. The detailed derivation is included in the Appendix.

Figure 7a shows a simple 1 pole + 1 zero passive low-pass filter which is commonly used with the PLL synthesizer whose phase detector output is current. This filter has a pole at 0Hz and a zero at $(1/2\pi R_1 C_1)$Hz. Together with the pole introduced by the VCO, this filter will give a 2nd order type 2 (2 poles at 0Hz) PLL loop, which our design procedure is based upon. The inclusion of C_2, R_2 and C_3 (see Figure 7b) effectively introduces two more poles located far away from the zero. This will provide more attenuation, if necessary, on the spurious sidebands without affecting the 2nd order nature of the loop.

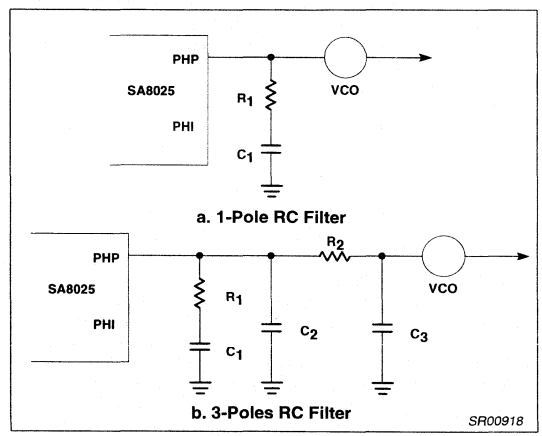

Figure 7. RC Filter Configurations

Definition of the PLL parameters:

δ: final frequency resolution after settling

$$\delta = \frac{\text{frequency error after settling}}{\text{switching step}} \quad \text{(EQ. 16)}$$

t_{SW}: switching time (sec)

f_N: natural frequency of the 2nd order system (Hz), $\omega_N = 2\pi f_N$ (rad/s)

N: total divide ratio

ξ: damping factor of the second order system. Typ. value is 0.707

K_{VCO}: VCO gain (Hz/V) or $2\pi \times$ VCO gain (rad/V)

K_ϕ: phase detector gain = $I_{CP}/2\pi$ (A/rad)

Normal Mode Design

The set of formulas (see Appendix) presented here is valid for normal mode operation in which only charge pump PHP is connected to the low-pass filter. This assumes the STROBE length

is short enough so that speed-up due to STROBE high is minimum in the switching process. Designers should use the normal mode design approach as a starting point and go on to the adaptive mode design if desired PLL performance cannot be met using this configuration.

$$\omega_N = \frac{-\ln(\delta \cdot \xi)}{\xi \cdot t_{SW}} \quad \text{(EQ. 17)}$$

$$C_1 = \frac{K_\phi \cdot K_{VCO}}{N\,\omega_N^{\,2}} \quad \text{(EQ. 18)}$$

$$R_1 = 2 \cdot \xi \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C_1}\right)^{0.5} \quad \text{(EQ. 19)}$$

$$C_2 \leq \frac{C_1}{10} \quad \text{(EQ. 20)}$$

$$\omega = \frac{1}{C_3 \cdot R_2} \quad \omega \text{ should be at least 10 times larger than } \omega_n \quad \text{(EQ. 21)}$$

NOTE: The unit of the factor $K_\phi \times K_{VCO}$ is unity when all the variables are expressed in radians. Therefore, designers can simply multiply the charge pump output current (I_{CP}) with the VCO gain in Hz/V to obtain this factor.

Adaptive Mode Design

The adaptive mode allows designers to take advantage of having one filter with two different loop filter responses. When the synthesizer is switching from channel to channel, a wider filter bandwidth (speed-up) is desired. Once the loop is locked at the correct frequency, a narrower filter is required to achieve lower noise. This mode can be realized by connecting the PHI charge pump to the integrating capacitor C1 (see Figure 8), controlling the width of the STROBE (amount of time for speed-up), and programming the CK and CL registers. Due to this configuration, the zero of the filter gets multiplied by $[2^{CL+1}\ (CK + 1) + 1] / [1 + 2^{CL+1}]$ times, which makes the loop more stable in speed-up mode. One drawback of this design is that switching from speed-up to normal current will cause a difference in the final phase error due to different current gain, which results in frequency instability or a "glitch" in the frequency domain. Because of this effect, the actual switching time will be longer than what the speed-up loop is designed for, since the loop has to re-settle again due to the glitch. Experimental trial of the width of the STROBE can help alleviate this problem.

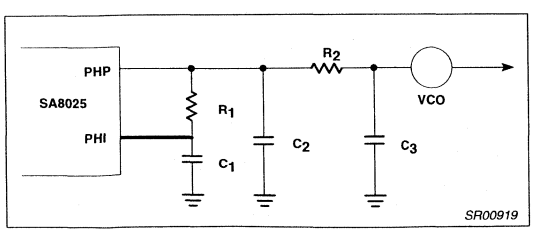

Figure 8. Adaptive Filter

Definition:

ξ_S: speed-up mode damping ratio

ξ_N: normal mode damping ratio

ω_{NS}: speed-up mode natural frequency

ω_{NN}: normal mode natural frequency

Design Steps:

1. Calculate ω_{NS} to meet the system switching time requirement using Eq. 17.
2. Decide how many times ω_{NN} is smaller than ω_{NS}. 5 times will be a good number.
3. Calculate filter component values using Eq. 17 to Eq. 20.
4. Calculate CL and CK values according to

$$CL = 3.32 \log_{10}\left(\frac{\xi_s \cdot \omega_{NS}}{\xi_N \cdot \omega_{NN}} - 1\right) - 1 \quad \text{(EQ. 22)}$$

$$CK = \left[\frac{\left(\frac{\omega_{NS}}{\omega_{NN}}\right)^2 - 1}{\left(\frac{\xi_S \cdot \omega_{NS}}{\xi_N \cdot \omega_{NN}} - 1\right)}\right] - 1 \quad \text{(EQ. 23)}$$

The above procedure ensures the loop bandwidth in speed-up mode is 5 times greater than that in normal mode while maintaining the required stability of the loop.

DESIGN EXAMPLE

This section shows a design example using the SA8025 for the Personal Handy Phone System (PHS), where the device is used in the normal mode (only PHP charge pump is active). The system parameters are as follows:

VCO frequency (f_{VCO}) = 1646.7 to 1670.1MHz

Channel spacing (f_{CH}) = 300kHz

Comparison frequency (f_{COMP}) = 8 × 300kHz = 2.4MHz

Switching time (t_{SW}) = 500µs

Switching step = 25MHz

Frequency error = within 1kHz

VCO gain (K_{VCO}) = 15MHz/V

Reference Crystal (f_{REF}) = 19.2MHz

Determine total divide ratio N

To synthesize channels from 1646 to 1670MHz with f_{COMP} = 2.4MHz, N should be between 686 and 695. For the same loop components, larger N yields smaller natural frequency (f_N). So, jumping from high-end to low-end (larger N) is slower than from low-end to high-end (smaller N). To ensure the same switching time from either direction, we use N = 695 for the worst case.

Determine ω_N

Using Eq. 16

$$\delta = \frac{1000}{25e6} = 0.04e\text{-}3$$

Pick ξ = 0.707 and use t_{SW} = 400µs for safety.

Using Eq. 17

$$\omega_N = \frac{-\ln(0.04e\text{-}3 \cdot 0.707)}{0.707 \cdot 400e\text{-}6} = 37,035$$

Determine R_N and I_{CP}

Pick RN = 10kΩ and CN = 100. Referring to Figure 5, I_{RN} becomes 80µA when V_{DDA} = 3V.

Using Eq. 1

$$I_{CP} = 100\left(\frac{80e\text{-}6}{32}\right) = 250\mu A$$

Determine R_1, C_1 and C_2

Using Eq. 18 with 2π's from K_{VCO} (rad/V) and K_ϕ (A/rad) cancel out

$$C_1 = 15e6 \left(\frac{250e\text{-}6}{695 \cdot 37,035^2}\right) = 3.93nF$$

Using Eq. 19

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{695}{15e6 \cdot 250e\text{-}6 \cdot 3.9e\text{-}9}\right)^{0.5} = 9.7k\Omega$$

Using Eq. 20

$$C_2 = \frac{3.93e\text{-}9}{10} = 390pF$$

Determine R_2 and C_3

R_2 and C_3 can help attenuate the unwanted fractional spurs at 300kHz offset.

Using Eq. 21

$$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_N$$

Pick R_2 = 18kΩ, then C_3 = 150pF.

Fractional spurs compensation, if necessary

With f_{COMP} = 300kHz, there would be some spurs located at 300kHz or multiples of 300kHz when NF not equal to 0. For this particular design, we are able to use a fixed CN value (100) to achieve spurs suppression of at least -64dBc for spurs located at 300kHz carrier offset. Spurs located at other frequencies are not present.

Design results

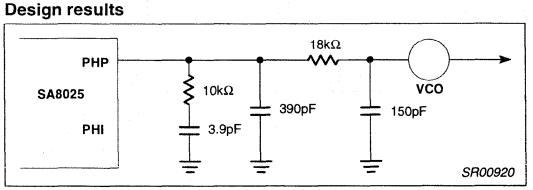

Figure 9. Main Loop Filter

Component values used on the demoboard:
C31 = 3.9pF
R23 = 10kΩ
C32 = 390pF
R24 = 18kΩ
C33 = 150pF
R21 = 560kΩ (RF)
R22 = 10kΩ (RN)

Software setting:
CN = 100
STROBE = 190µs

MEASUREMENT RESULTS

The major performance parameters for a PLL synthesizer are close-in phase noise, spurious sidebands and switching time. This section presents the measurement results obtained from the design made in the section on LOOP FILTER DESIGN.

Close-In Phase Noise

The close-in phase noise level directly correlates with the residual FM and integrated jitter performance, two integrated noise parameters. It is measured within the loop bandwidth (the peak of the "hump" around the carrier) at a specified carrier frequency offset, e.g., 1kHz, and it is expressed in -dBc/Hz. Figure 10 displays the result of such a measurement. The carrier is located at 1668.3MHz (NF = 1) and the span is 10kHz. The resolution bandwidth (measurement bandwidth) is 100Hz. Therefore, the close-in phase noise at 1kHz offset is:

= -58.2dBc – 10 log (100)

= -78.2dBc/Hz

Spurious Performance

Figures 11 and 14 show the spurious performance of the highest and the lowest bands of interest with NF = 1 and 7, which are the worst case for fractional spurs. Other spurs within the band are totally compensated.

Switching Time

The switching time (see Figures 15 and 16) was measured using the HP 53310A Modulation Domain Analyzer (MDA) with option 031. Under the TRIGGER Menu of the MDA, "Triggered", "Ext Edge" and "Arm Only" were selected. The instrument was setup to accept an external trigger, which was the STROBE signal used for programming the synthesizer. This signal was connected to the Ext Arm input while the VCO signal was fed into the Channel C. The MDA would display the frequency versus time variation of the VCO signal upon the arrival of the STROBE signal. This design achieved a switching time of 400µs to within 1kHz of the final frequency for a 21.6MHz jump between 1646.7 and 1668.3MHz in either direction. The STROBE width used in this experiment was 190µs.

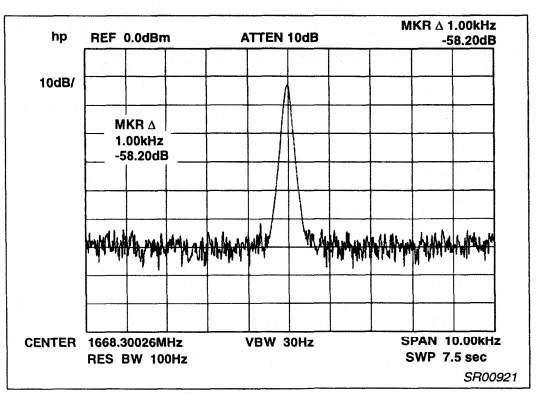

Figure 10. Close-In Phase Noise at 1668.3MHz

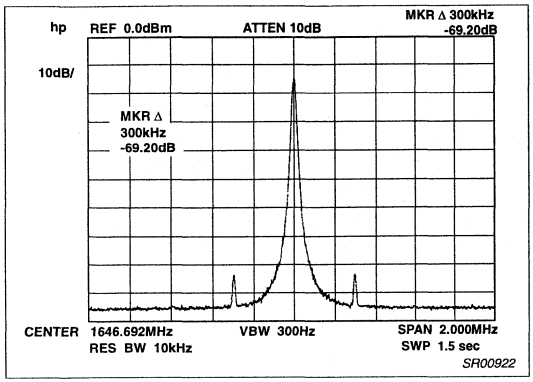

Figure 11. Fractional Spurs (f_{VCO} = 1646.7MHz, NF = 1)

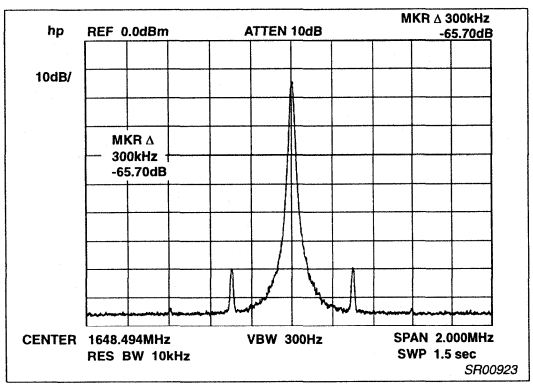

Figure 12. Fractional Spurs (f_{VCO} = 1648.5MHz, NF = 7)

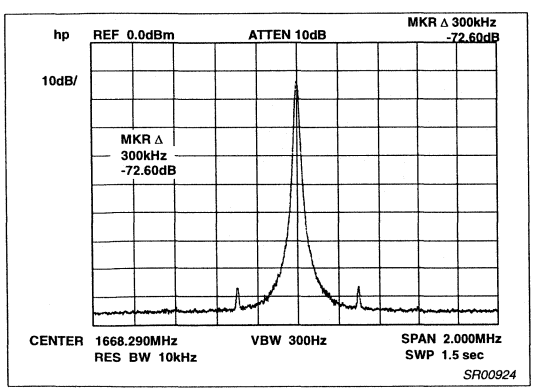

Figure 13. Fractional Spurs (f_{VCO} = 1668.3MHz, NF = 1)

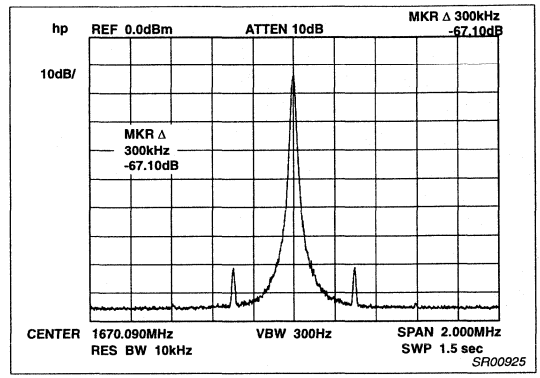

Figure 14. Fractional Spurs (f_{VCO} = 1670.1MHz, NF = 7)

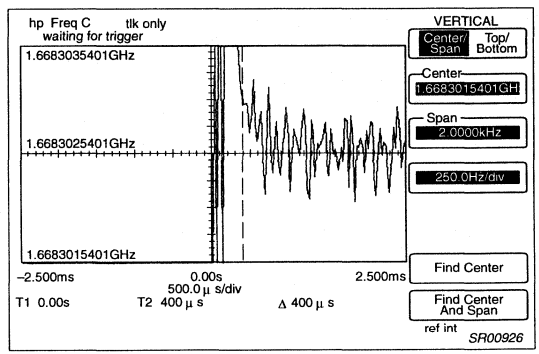

Figure 15. Switching Time
(1668.3 to 1646.7MHz Step to Within 1kHz)

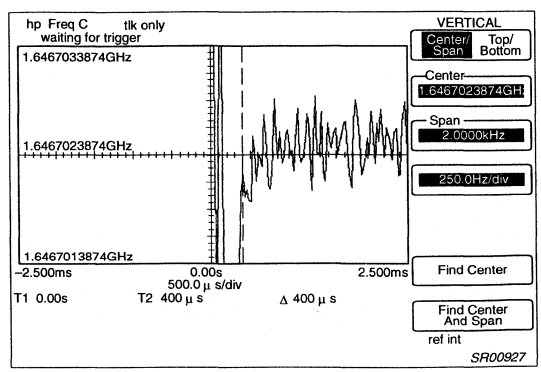

Figure 16. Switching Time
(1646.7 to 1668.3MHz Step to Within 1kHz)

MODULO 4 DESIGN

Previous sections showed a design using a 4 modulus prescaler (64/65/68/73) to synthesize total divide ratios (N) from 686 to 694. This requires sending both B and A words since NM4 is stored in B word. In some designs, users may prefer to send only one word for channel switching due to hardware limitation. We could have used modulo 5 (FMOD = 5) to make N five times higher and used a triple modulus prescaler (64/65/68 or 64/65/73). In some situations this is impossible since the comparison frequency has to be an integer factor of the crystal reference. For instance, if f_{REF} is 19.2MHz and f_{CH} is 300kHz, f_{COMP} becomes 1.5MHz, which is not an integer factor of 19.2MHz. To get around this problem, a modulo 4 design must be used.

Figure 17 shows the concept of a modulo 4 design. In the mod 4 case, f_{COMP} is four times the channel spacing, f_{CH}. Instead of programming NF to one through seven, even numbers are used.

To synthesize 1656.3, 1656.6, 1656.9, 1657.2MHz with channel spacing = 300kHz using mod 8 and mod 4.

SA8025 (mod 8)	SA8025 (mod 4)
$f_{VCO} = f_{COMP}$ (N+NF/8)	$f_{VCO} = f_{COMP}$ (N+NF/8)
1656.3 = 2.4 (690 + 1/8)	1656.3 = 1.2 (1380 + 2/8)
1656.6 = 2.4 (690 + 2/8)	1656.6 = 1.2 (1380 + 4/8)
1656.9 = 2.4 (690 + 3/8)	1656.9 = 1.2 (1380 + 6/8)
1657.2 = 2.4 (690 + 4/8)	1657.2 = 1.2 (1381 + 0/8)
f_{COMP} = 8 x f_{CH} = 2.4MHz	f_{COMP} = 4 x f_{CH} = 1.2MHz

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Figure 17.

To achieve the same loop response with the mod 8 design, the same loop filter with twice the charge pump current can be used. This can be derived from Eq. 18. When N is doubled, K_ϕ (two times more current) has to be doubled as well to maintain the same natural frequency which determines the switching time and residual FM. In this case, we use CN = 200 for the mod 4 design.

The only penalty of this method is that theoretical close-in phase noise performance is affected. Since N is twice as much, the close-in noise floor should be 20log(2) = 6dB higher. However, minor degradation for using mod 4 was measured in the laboratory. This could be due to the fact that the comparison cycles are fewer with mod 4, which makes the charge pump ON time less, thus producing less noise. In addition, higher charge pump current improves the phase noise.

MOD 4 DESIGN MEASUREMENT RESULTS

Figures 18 to 22 show the measurement results for the mod 4 design. The close-in phase noise level is shown to be -77.1dBc/Hz at 1kHz carrier offset with a measurement bandwidth of 100Hz. Spurious sidebands (see Figures 19 and 20), which are caused by fractional jitter, are -67dB down from carrier for the high band and -68dB down for the low band. Switching time (see Figures 21 and 22) is exactly the same as the mod 8 design (400µs) because the loop natural frequency is the same for both cases.

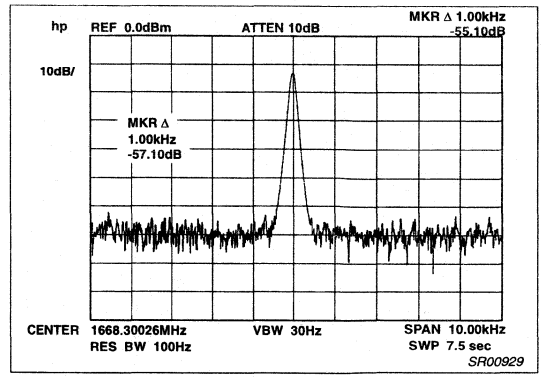


Figure 18. Close-In Phase Noise at 1668.3MHz

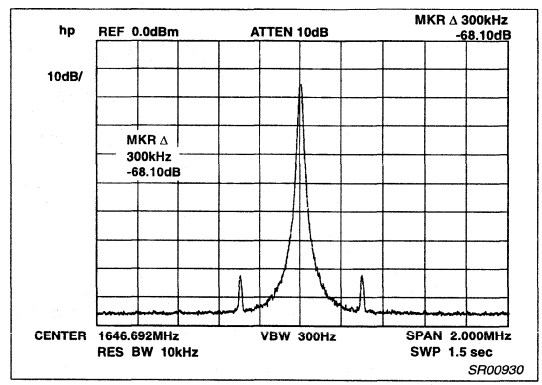


Figure 19. Fractional Spurs (f_{VCO} = 1646.7MHz, NF = 2)

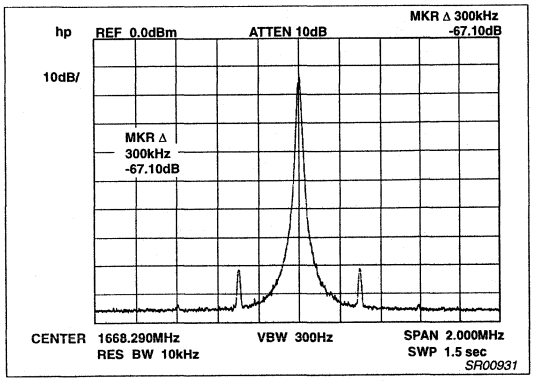


Figure 20. Fractional Spurs (f_{VCO} = 1668.3MHz, NF = 2)

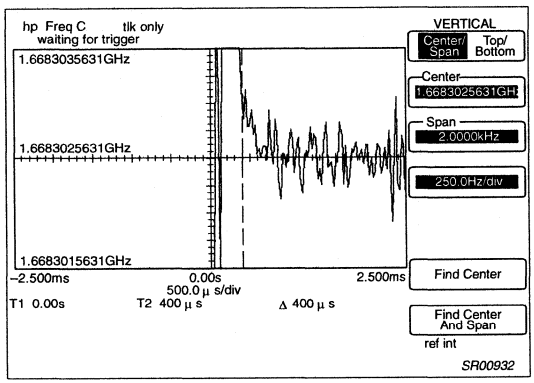


Figure 21. Switching Time (1668.3 to 1646.7MHz Step to Within 1kHz)

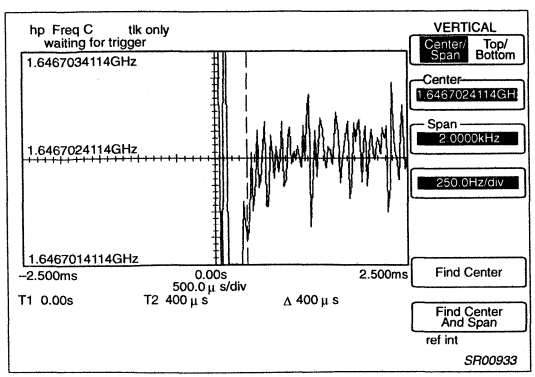


Figure 22. Switching Time (1646.7 to 1668.3MHz Step to Within 1kHz)

FREQUENTLY ASKED QUESTIONS

Q. The part is powered-up and programmed. The VCO is still free-running. What's wrong?

A. Three things to check for if the PLL does not lock:

1. Make sure the correct data have been transmitted to the CLK, DATA and STROBE pins
2. Make sure a reference signal with correct frequency and amplitude are present at the REF_{IN} pin.
3. Make sure that the prescaler value is chosen correctly. The SA8025 has two 3 modulus prescalers and uses different programming bits.
4. Be aware of cold solder joints. Pay special attention to the loop filter section and the connection from the VCO to the RF_{IN} pin.

Q. The synthesizer locks up, but it locks at a wrong frequency. Why?

A. Check the NM1, NM2, NM3 and NM4 bits. Make sure they are correctly programmed.

Q. I see spurs sitting at the comparison frequency offset and they don't change with the filter bandwidth. How can I get rid of them?

A. These spurs may be caused by improper grounding of the VCO and the filter section. Make sure they all have short and clean paths going back to the supply ground. Also, clean the filter section to avoid leakage.

Q. I see some spurs which are neither fractional nor comparison spurs. What are they?

A. Since the VCO is a very sensitive device, it can be influenced by many noise sources. Common ones are:

1. Computer monitor. The sweeping frequency of the screen will modulate the VCO and create spurious sidebands at 30 to 40kHz carrier offset.
2. Free-running auxiliary VCO. Even though the EA bit is disabled, if the auxiliary VCO is still ON, it will modulate the main VCO and cause spurs.
3. Fluorescent lamp.

Q. How can the residual FM be improved?

A. Three things can be done to improve residual FM:

1. Use a narrower loop filter.
2. Use a higher crystal reference frequency. This will reduce the charge pumps ON time and make the charge pumps generate less noise.
3. Use higher charge pump output current. This will increase the signal to noise ratio at the charge pump, which makes the circuit less noisy.

Q. When I FM modulate the AUX synthesizer, I see modulation on the MAIN carrier as well. Is that normal?

A. Yes, that is normal. The amount of interference between the AUX and the MAIN has to be verified experimentally.

Q. If I double the phase detector gain (twice the current), what should be done to keep the switching time the same?

A. Referring to Eq. 18 and Eq. 19, the value of C_1 should be doubled and R_1 should be halved if you want to maintain the same natural frequency of the loop when the detector gain (K_ϕ) is twice what it was before.

Q. When I use the 3 modulus prescaler (PR = 10), what should the values for NM4 be?
A. Simply treat them as "don't cares".

Q. What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?
A. The phase detector gain (K_ϕ) is equal to the charge pump output current (I_{CP}) divided by 2π since the phase detector covers 2π range. However, when we use the design formulas shown in the "Loop Filter Design" section, K_ϕ can be replaced directly by I_{CP} because the 2π factor will be cancelled out by the 2π from the VCO gain, K_{VCO}.

Q. What should I do with the RA and PHA pins when the auxiliary synthesizer is not used?
A. When the auxiliary synthesizer is not used, leave PHA open, connect AUX_{IN} to ground, connect RA to V_{DDA} or leave it open and program EA bit to zero.

Q. Variations on the RF pins input impedance for different prescaler value can cause VCO pulling. Does that happen to the SA8025?
A. The RF input to the prescaler is well buffered, and the input impedance should always stay the same.

Q. Can the clock signal be disconnected after the A word is sent?
A. Yes, the clock signal can be disabled after the A word is sent and enabled again for sending new words to the part.

Q. Can I drive the part with a +5dBm RF signal even though the spec is 0dBm max?
A. Users should refer to the graphs put in the latter part of the data sheet for minimum and maximum input power. The device should be able to handle +5dBm at 1800MHz, but this is not guaranteed in the data sheet.

Q. I am doing open-loop modulation on the main synthesizer. How do I put the charge pump to high impedance state to allow modulation?
A. Program CN register to zero. This will set the charge pump to a high output impedance state so that FM modulation can be done.

Q. Is the demoboard layout good for any applications? If not, what should I do?
A. The demoboard layout included in this document was optimized only for this particular design. Designers should consult the PCB layout hints in the "PCB Layout" section of this application note when laying out circuit boards for other applications.

Q. I am using the S8025 for PHS system and seeing different amplitudes on the fractional spurs from part to part. However, this variation does not appear to affect my RX/TX performance. Is this a safe assumption?
A. Yes, because the SA8025 is targeted for the PHS system and any spurs that only fall in the adjacent channels (at 300kHz carrier offset) are acceptable for the PHS.

REFERENCES

"Digital PLL Frequency Synthesizers", Ulrich L. Rohde, Prentice Hall, 1983.

"Designer Guide to Frequency Synthesis Using the UMA1005", Application Note, Report No: SCO/AN92002.

"Modem Control Systems", Richard C. Dorf, Addison Wesley, 1989.

APPENDIX

Derivation of the 2nd order PLL design formula:

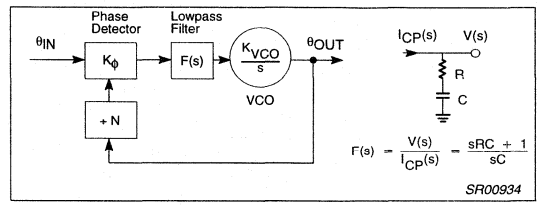


Figure 23. PLL Block Diagram

The transfer function of the loop low-pass filter is represented by:

$$F(s) = \frac{sRC + 1}{sC} \qquad \text{(EQ. 24)}$$

The low-pass filter has a pole at 0Hz (set denominator to zero) and a zero at $1/2\pi RC$ Hz (set numerator to 0).

Referring to Figure 23, the open-loop response of the system (multiplication of the Forward Gain and Feedback Gain) becomes:

$$G(s)H(s) = \frac{K_\phi \cdot K_{VCO}}{Ns}\left(\frac{sRC + 1}{sC}\right) \qquad \text{(EQ. 25)}$$

Phase Margin (ϕ_{PM}) is defined as the difference between -180° and the phase at the point where the open-loop response has unity gain. A stable system must have a ϕ_{PM} greater than 0°. Eq. 25 shows that there are two poles sitting at 0Hz, one from the filter and one from the VCO, which causes -180° phase shift. In order to have a stable system, a zero has to be added to the filter so that ϕ_{PM} will be greater than zero. ϕ_{PM} is related to the damping factor, ξ, with $\xi = 0.01 \times \phi_{PM}$.

To find the characteristic equation (CE) of the system, we equate 1 + G(s)H(s) to zero. Therefore,

$$1 + \frac{K_\phi \cdot K_{VCO}\,(sRC + 1)}{s^2 NC} = 0 \qquad \text{(EQ. 26)}$$

The CE becomes

$$s^2 + \frac{K_\phi \cdot K_{VCO} \cdot R}{N}s + \frac{K_\phi \cdot K_{VCO}}{NC} \qquad \text{(EQ. 27)}$$

Compare Eq. 27 with the standard 2nd order CE ($s^2 + 2\zeta\omega_N s + \omega_N^2$), we have

$$\omega_N^2 = \frac{K_\phi \cdot K_{VCO}}{NC} \Rightarrow C = \frac{K_\phi \cdot K_{VCO}}{N\,\omega_N^2} \qquad \text{(EQ. 28)}$$

$$2\xi\omega_N^2 = \frac{K_\phi \cdot K_{VCO} \cdot R}{N} \Rightarrow R = 2 \cdot \xi \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C}\right)^{0.5} \text{(EQ. 29}$$

which are the design used in "Loop Filter Design" section.

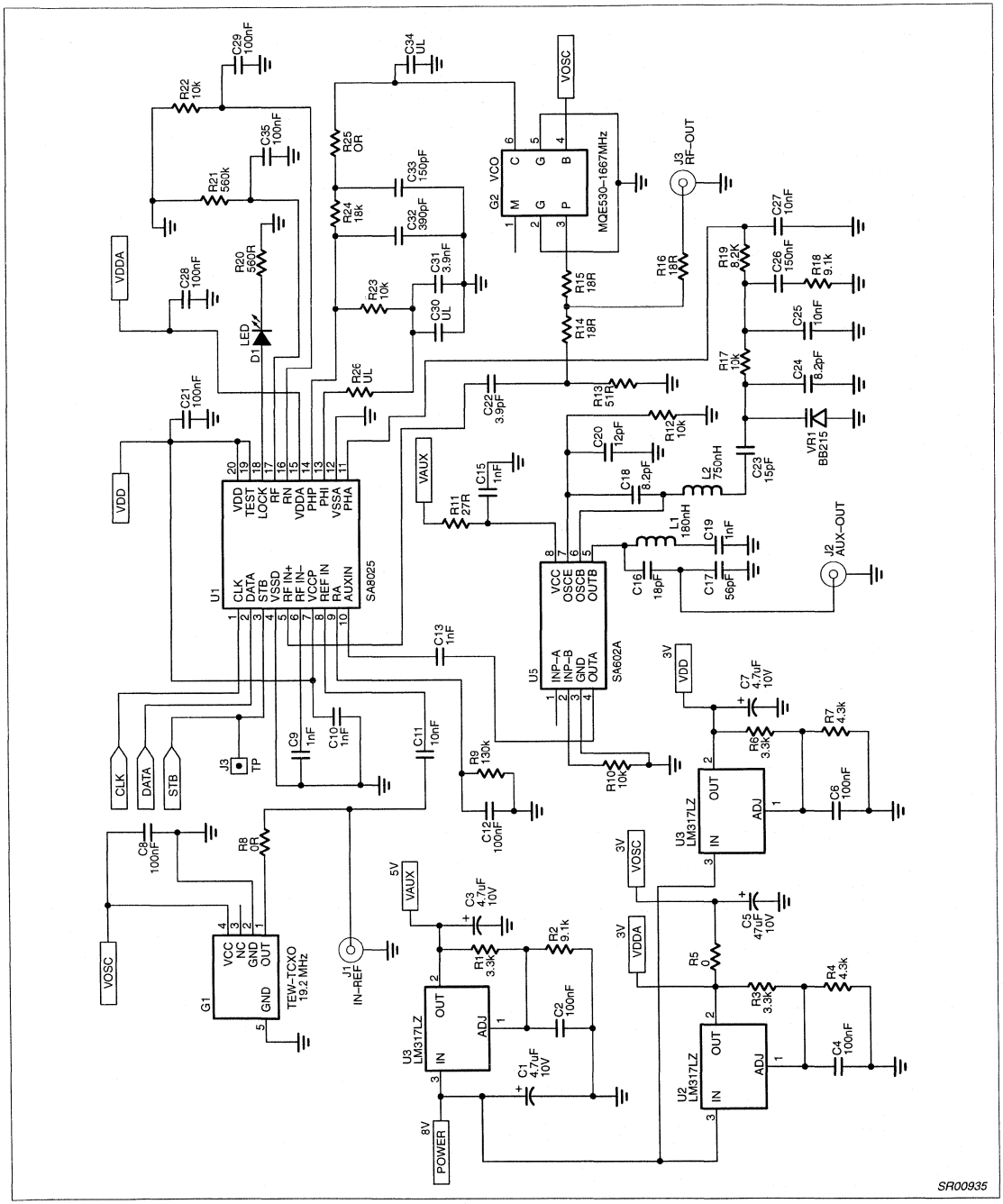
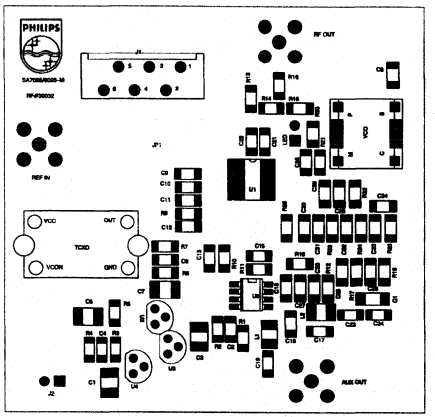
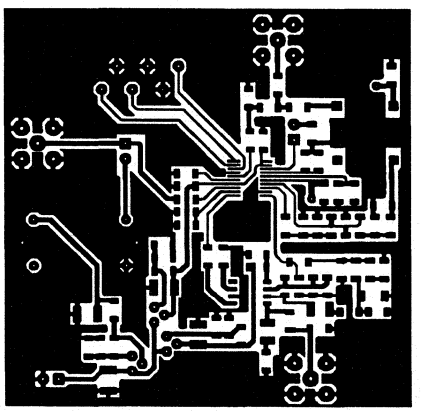


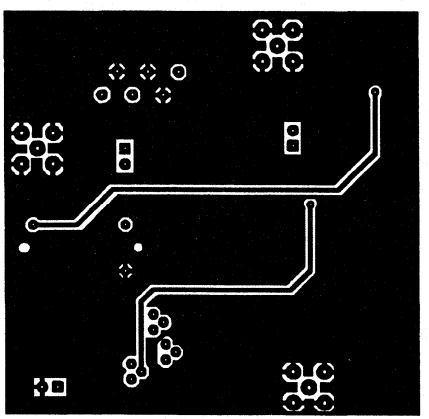
Figure 24. SA8025DK Application Circuit



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

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Figure 25. SA8025DK Demoboard Layout (NOT ACTUAL SIZE)

Table 2. Customer Application Component List for SA8025DK

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	3.9pF	50V	C22	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A3R9CK
2	8.2pF	50V	C24, C18	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A8R2CK
1	12pF	50V	C20	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A120JK
1	15pF	50V	C23	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A150JK
1	18pF	50V	C16	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A180JK
1	56pF	50V	C17	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A560JK
1	150pF	50V	C33	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A151JK
1	390pF	50V	C32	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A391JK
5	1000pF	50V	C9, C10, C13, C15, C19	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315A102JP
1	3900pF	50V	C31	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C392KK
3	0.01µF	50V	C11, C25, C27	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C103KK
9	0.1µF	50V	C2, C4, C6, C8, C12, C21, C28, C29, C35	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C104KP
1	0.15µF	16V	C26	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C154KP
4	4.7µF	10V	C1, C3, C5, C7	Tant. chip cap. A 3216 ±10%	Garrett	Philips	49MC475B010KOAS
Surface Mount Resistors							
3	0Ω		R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
3	18Ω		R14, R15, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW180E
1	27Ω		R11	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW270E
1	51Ω		R13	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW510E
1	560Ω		R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
3	3.3kΩ		R1, R3, R6	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW332E
2	4.3kΩ		R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW432E
1	8.2kΩ		R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW822E
2	9.1kΩ		R2, R18	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW912E
5	10kΩ		R10, R12, R17, R22, R23	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW103E
1	18kΩ		R24	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW183E
1	130kΩ		R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW134E
1	560kΩ		R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW564E
Surface Mount Diodes							
1			VR1 (Varactor)	Variable capacitance SMD diode	Digikey	Philips	BB215
1			D1	SM Led	Digikey		
Surface Mount Inductors							
1	0.18µH		L1	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R18M
1	0.75µH		L2	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R68M
Voltage Regulators							
3			U1, U2, U3	Voltage regulator	Digikey		LM317LZ
TCXO							
1	19.2MHz		G1	Temp. controlled crystal osc.	TEW	TEW	TXS1034N-19.2MHz
VCO							
1	1667MHz		G2	Voltage controlled osc.	Murata	Murata Erie	MQE530-1667
Surface Mount Integrated Circuits							
1			U4	1MHz Fractional-N Synthesizer	Philips	Philips	SA8025DK
1			U5	Double Balanced Mixer Oscillator	Philips	Philips	SA602A
Miscellaneous							
3			SMA1, SMA2, SMA3	SMA right angle jack receptacle	Newark	EF Johnson	142-0701-301
1			J1	Male 6-pins connector	STOCKO	STOCKO	MKS1956-6-0-606
1			J2	Male 2-pins connector	STOCKO	STOCKO	MKS1851-6-0-202
1			JP1	Test point	Digikey	3M	929647-36
1				Printed circuit board	Philips	Philips	SA7025/8025-M
75 Total Parts							

SA900 I/Q transmit modulator for 1GHz applications AN1892

Author: Wing S. Djen

INTRODUCTION

The SA900 (Figure 1) is a truly universal in-phase and quadrature (I/Q) radio transmitter that can perform many types of analog and digital modulation including AM, FM, SSB, QAM, BPSK, QPSK, FSK, etc. It is a highly integrated system which saves space and cost for the manufacturers producing cellular and wireless products. The device allows baseband signals to directly modulate the I/Q carriers, which are generated by internal phase shift network, in the 1GHz range, and to maintain good linearity required for linear modulation scheme (e.g., π/4-DQPSK). It contains an on-chip frequency divider, phase detector, and VCO, which can be built into a phase-locked loop (PLL) frequency synthesizer to create a transmit offset frequency. Its unique internal design allows frequency conversion without having an external image rejection filter for eliminating the sum term after mixing. The SA900 meets the specifications required by the IS-54, the industry standard for North America Digital Cellular (NADC) system. This application note reviews the basic concept of I/Q modulation and discusses the key points when designing the SA900 for an RF transmitter.

I/Q MODULATION

Any bandpass RF signals can be represented in polar form by

$$s(t) = A(t) \cos [\omega_c t + \phi(t)] \quad \text{(EQ. 1)}$$

where A(t) is the signal envelope and $\phi(t)$ is the phase. By using the trigonometric identities, we can represent EQ. 1 in rectangular form by

$$s(t) = I(t) \cos [\omega_c t] - Q(t) \sin [\omega_c t] \ , \quad \text{(EQ. 2)}$$

$$I(t) = A(t)\cos[\phi(t)]$$

$$Q(t) = A(t)\sin[\phi(t)]$$

Since the baseband signals I(t) and Q(t) modulate two exactly 90° out-of-phase carriers $\cos(w_c t)$ and $-\sin(w_c t)$ respectively, we call the system implementing EQ. 2 an in-phase and quadrature (I/Q) modulator. Figure 2 shows the mathematics and hardware implementation of an I/Q modulator.

The local oscillator, usually a VCO within a PLL, generates the carrier and is split into two equal signals. One goes directly into a double-balanced mixer to form the I-channel and the other one goes into the other mixer via a 90° phase shifter (realized by passive elements) to provide the Q-channel. The baseband signals I(t) and Q(t), either analog or digital in nature, modulate the carrier to produce the I and Q components which are finally combined to form the desired RF transmitting signal. Since any RF signal can be represented in the I/Q form, any modulation scheme can be implemented by an I/Q modulator.

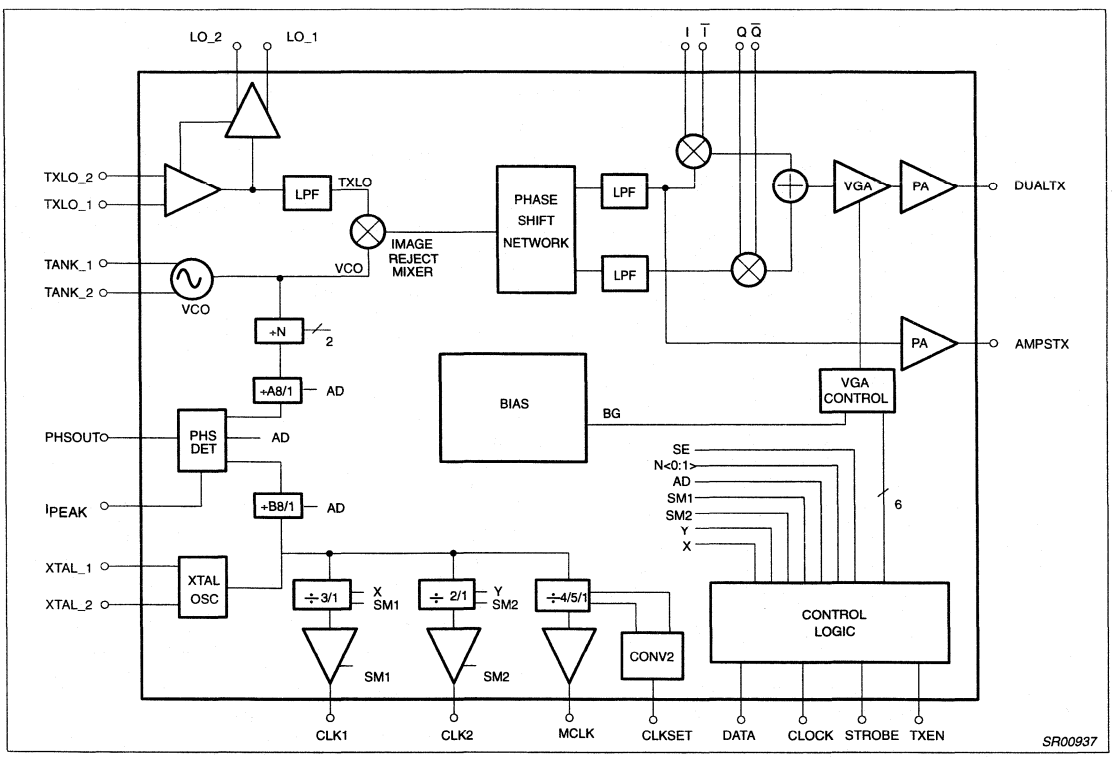


Figure 1. SA900 Transmit Modulator

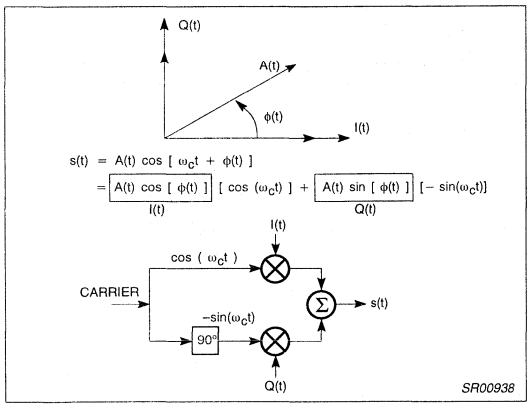


Figure 2. Mathematical Representation and Hardware Implementation of I/Q Modulator

Linear Digital Modulation

Linear digital modulation techniques depend on varying the phase and/or magnitude of an analog carrier according to some digital information: ones and zeros. This digital information can be the output of an analog-to-digital converter (e.g. voice codec), or it can be digital data in some standard formats (e.g. ASCII). The most popular digital signaling format is non return-to-zero (NRZ), where 1s and 0s are converted into signal with amplitude of 1 and -1, respectively, in a symbol duration. Since NRZ signal has infinite bandwidth, transmit filters have to be used to limit the spectral spreading. To ensure each NRZ symbol does not smear into its neighbors due to low-pass filtering and channel distortion causing inter-symbol interference (ISI), the frequency response of the low-pass filter has to satisfy Nyquist criteria. One example of this type of filter is the linear phase square-root-raised cosine filter. Together with the same type of filter for receive low-pass filtering, the signal is guaranteed ISI free in a Gaussian environment. One straight-forward technique of transmitting these bandlimited signals through communication channels would be applying it directly to the mixer of the I-channel to generate the RF signal. This is known as binary phase shift keying (BPSK), where the phase of the carrier is shifted 180° to transmit a data change from 0 to 1 or 1 to 0.

Quadrature or quaternary phase shift keying (QPSK) is a much more common type of modulation scheme used in mobile and satellite communications. It has four possible states (90° apart) and each of them represents two bits of data. Figure 3 shows the baseband generator for QPSK (without the differential phase encoder). NRZ data bits go through the serial-to-parallel converter (see Figure 4) and are mapped in accordance to some rules to generate I and Q values. The generic rule will be the values of I and Q components are 1 and 1 for the data bits "11" (45°) and -1 and -1 for the data bits "00" (-135°). These discrete signals have to be bandlimited by Nyquist low-pass filters to be ISI free.

A more sophisticated way of mapping results in π/4-DQPSK (D for differential encoding), which is chosen for North America Digital Cellular (IS-54), Personal Digital Cellular (PDC) in Japan, and Personal Handy Phone System (PHS) in Japan. In this scheme, consecutive pairs of bits are encoded into one of the four possible phases: π/4 for "11", 3π/4 for "01", -3π/4 for "00", and -π/4 for "10". However, unlike the previous case that "11" is always π/4 and "00" is always -3π/4, the encoded phases are the degrees that the carrier has to shift at each sampling instances. Thus, the information is contained in the phase difference (differential) instead of absolute phase for π/4-DQPSK.

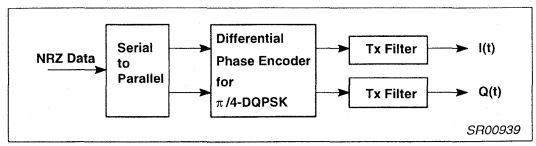


Figure 3. QPSK and π/4-DQPSK Baseband Generator

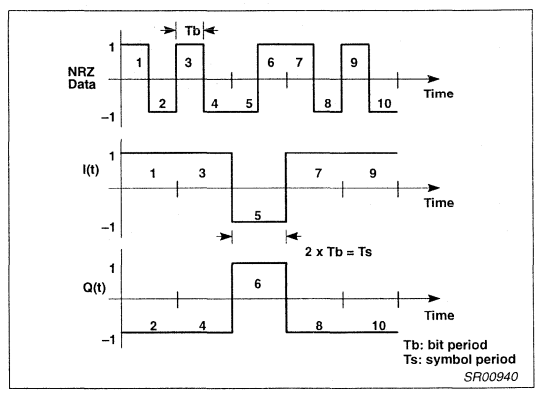


Figure 4. Serial-to-Parallel Conversion

A better way to tell the difference between QPSK and π/4-DQPSK is by looking at the signal constellation diagram, shown in Figure 5, which displays the possible values of I and Q vectors and change of states. Constellation diagram is also known as phase diagram because it shows the phase of the carrier at the sampling point. Notice that the phases of QPSK are assigned for every two bits of data; therefore, it can transmit twice as much information as BPSK in a given bandwidth, i.e., more bandwidth efficient. 8-PSK is another type of modulation used for high efficiency requirements. It maps three bits into 8 phases, 45° apart, in the constellation. More spectral efficient modulation can be created by mapping more bits into one phase at each sampling point. However, as you put more dots in the signal constellation, the signal susceptibility to noise is lower because the decision distance is shorter (dots are closer). Then, it requires higher carrier-to-noise (C/N) ratio to maintain the same bit error rate (BER).

One common misconception is that since π/4-DQPSK has 8 states in the constellation, it is just another type of 8-PSK. Notice that at every sampling instant, the carrier of π/4-DQPSK is only allowed to switch to one of the 4 possible states (see Figure 5). So, we still have two data bits which get encoded into 4 phases. Thus, it has the same spectral efficiency as QPSK for the same carrier power. The reason for using this modulation scheme is twofold. First, the envelope fluctuation, which causes spectral spreading due to nonlinearity of transmitter and amplifier, is reduced because the maximum phase shift is 135° instead of 180°. Second, the signal can be demodulated non-coherently which simplifies the receiver circuitry by eliminating the need for carrier recovery.

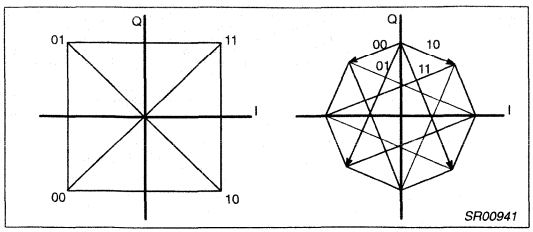


Figure 5. Signal Constellation of QPSK and π/4-DQPSK

Digital and Analog FM

Another family of digital modulation is categorized by frequency change of the carrier instead of phase and/or amplitude change. One of them is frequency shift keying (FSK), where the carrier switches between two frequencies. FSK is also known as digital FM because it can be generated by feeding the NRZ data stream into an analog VCO. FSK appears as a unit circle in the signal constellation because the RF signal envelope is constant and the phase is continuous. Baseband filtering is usually applied for FSK to limit the RF bandwidth of the signal so that more channels can fit into a given frequency band.

One common modulation of this type is known as Gaussian minimum shift keying (GMSK), which is used for GSM and some other wireless applications. GMSK can be generated by following its definition: bandlimit the NRZ data stream by a Gaussian low-pass filter, then modulate a VCO with modulation index (2 x frequency deviation/bit rate) set to 0.5. In other words, the single-sided frequency deviation is one fourth of the bit rate ($\Delta f = R/4$).

Another way of generating GMSK is by I/Q modulator. Referring back to EQ. 2, any RF signal can be split into I and Q components. Unlike the QPSK mentioned before, baseband I(t) and Q(t) are not discrete points for FM signals; rather, they are continuous functions of time. The way to produce FM is shown in Figure 6. We first store all the possible values of $\cos[\phi(t)]$ and $\sin[\phi(t)]$ in a ROM lookup table, which will be addressed by the incoming data to generate the I and Q samples. The output data from the ROM is then applied to D/A converters, after low-pass filtering for signal smoothing, to produce the analog baseband I and Q signals. This method guarantees the modulation index to be exactly 0.5, which is required for coherent detection of GMSK (e.g. GSM system). The same I/Q principle can also be applied to generating analog FM signals.

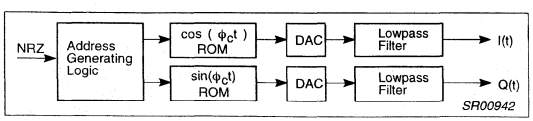


Figure 6. Digital FM (e.g. GMSK) Baseband I/Q Generator

Single sideband AM (SSB-AM)

AM signals can be divided into 3 types: the conventional AM, double sideband suppressed carrier AM (DSB-AM) and SSB-AM. The first type is not attractive because for 100% modulation, two-thirds of the transmit signal power appears in the carrier, which itself conveys no information at all. By using a balanced mixer (e.g. Gilbert cell), one can generate DSB-AM, where the carrier is totally suppressed and only the upper and lower sidebands are present. However, this is still not the best because the information is transmitted twice, once in each sideband. To further increase the efficiency of transmission, only one sideband is needed to deliver the information. The SSB-AM can be generated by an I/Q modulator with the baseband information feeding the modulator (by quadrature), as shown in Figure 7. This modulation technique can greatly reduce the bandwidth of the signal and allows more signals to be transmitted in a given frequency band. This topic is discussed in detail in Philips RF application note, #AN1981, "New low-power single sideband circuits".

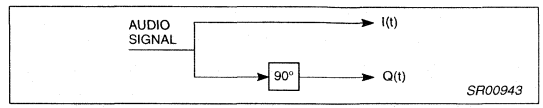


Figure 7. Baseband Processing for SSB-AM

SYSTEM ARCHITECTURE

There are usually two schemes, the dual conversion and direct conversion, used for implementing transmit modulators. Dual conversion is simpler to implement by modulating an oscillator at lower frequency and then up-converting to the carrier frequency. This scheme, however, is more expensive due to the need for additional filtering and more PC board space. By using only one mixer, direct conversion requires fewer components but is harder to implement.

The problems that direct conversion suffers are carrier leakage and modulated signal coupling. Poor RF isolation of the surface mount packages will allow the carrier to be present at the transmitter output thus making it difficult to have -40dBc carrier suppression. In addition to that, modulated RF signal would couple back to the oscillator (usually a VCO in a PLL synthesizer loop) and cause modulation distortion.

Based on the concept of dual conversion, the SA900 uses an image rejection mixer to eliminate the need for IF filtering and allow monolithic integration. The transmit carrier (LO) is down-converted by the frequency synthesized by the on-chip VCO, which operates from 90 to 140MHz. This LO is then modulated by the baseband I/Q signals to obtain a complex modulation scheme. The image (sum term) after mixing and LO is sufficiently suppressed by the image rejection mixer. Any residual amounts can be further suppressed by an external duplex filter.

Figures 8 and 9, respectively, show how the SA900 can be used in frequency division duplex (FDD) and time division duplex (TDD) transceivers. Notice that the LO for both systems is running at a frequency which is higher than the transmit frequency, thus minimizing carrier leakage. In the FDD system only one external VCO is required for generating both transmit and receive LO when using the SA900.

Figure 10 shows the IS-54 front-end chip set which consists of the SA601, SA7025, SA900, and SA637. This receiver architecture (SA637) supports a digital magnitude/phase baseband demodulator. An alternate configuration will be using the SA606 FM/IF receiver in conjunction with an external I/Q demodulator IC. The following table shows the possible configurations for the IS-54 handsets using the SA900 as transmitters.

Rx 1st IF	On-Chip VCO Frequency	On-Chip ÷N Value	Crystal Frequency
83.16MHz	128.16MHz	6	21.36MHz
71.64MHz	116.64MHz	6	19.44MHz
45MHz	90MHz	6	15MHz
84.6MHz	129.6MHz	9	14.4MHz

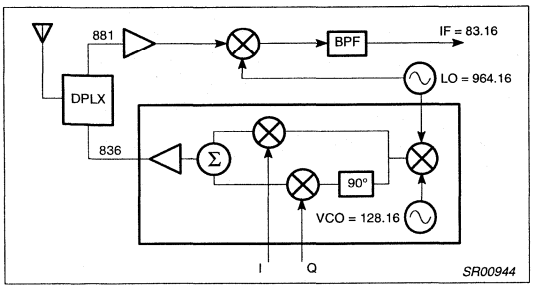


Figure 8. FDD System Using SA900

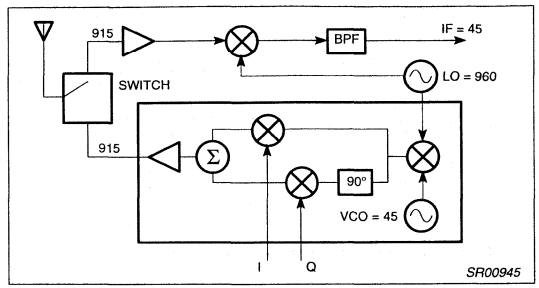


Figure 9. TDD System Using SA900

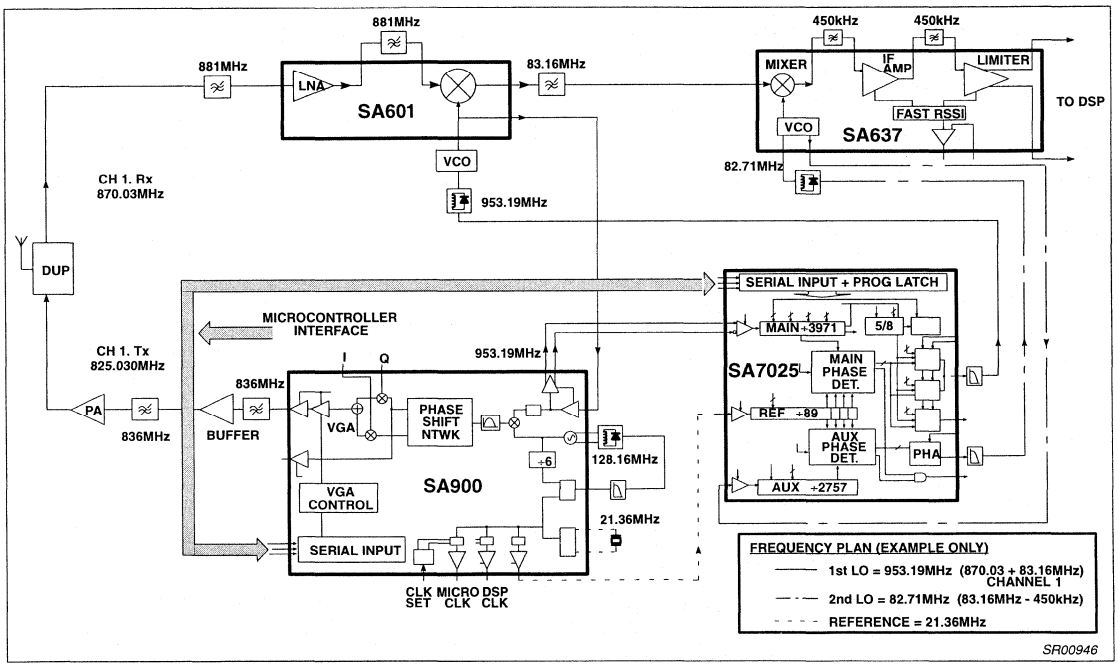


Figure 10. IS-54 front-end chip set from Philips

DESIGNING WITH THE SA900

Baseband I/Q Inputs

The baseband modulation inputs are designed to be driven differentially for the SA900 to operate at its best. The I and Q inputs should have a DC offset of V_{CC} /2, which is externally provided by common DSP chips. If all four inputs are biased from the same source, the device can tolerate $\pm 0.5V_{DC}$ error; however, inaccuracy of DC bias between I1/I2 or Q1/Q2 causes reduced suppression of the carrier. Thus, it is important to have a well regulated DC supply for I and Q signal biasing. The bandwidth of the inputs is much higher than the specified 2MHz. Approximately 2dB of power loss will be experienced if the I and Q inputs are 50MHz.

The SA900 generates a minimum of 0dBm of power to a 50Ω load when the amplitude of the I and Q signals are $400mV_{P-P}$. The output power will decrease by 6dB for every 50% decrease in I/Q amplitude. Single-ended I and Q sources can be used but are not recommended due to the degradation in carrier suppression (more than 10dB compared to differential). In addition, the entire noise performance of the device will suffer. V_{CC} /2 should be applied to I2 and Q2 pins if the part is driven single-endedly.

Transmit Local Oscillator

The transmit local oscillator path consists of a TXLO input buffer, LO output buffer, VCO, image rejection mixer and phase shift network. Together with a few external components, this section provides the I and Q carrier for modulation.

The TXLO inputs and LO outputs are designed to be used in an external PLL which synthesizes different frequencies for channel selection. The RF signal being generated is fed into TXLO inputs and then comes out of LO outputs to complete the system synthesizer loop. The TXLO inputs are differential in nature and

have a VSWR of 2:1 with input impedance of 50Ω. Single-ended sources can be used by AC grounding the TXLO_2, as done on the demoboard. This signal should also be AC coupled into the TXLO_1. The frequency range for these inputs is from 900 to 1040MHz while the input power should be between -10 to -13dBm. The output level will be changed significantly if the input level is below -25dBm.

The output power of the LO buffered signal changes by about 2dB when the SA900 is in a different mode of operation. Typical values are -13.5dBm and -15.5dBm for DUAL mode and STANDBY mode, respectively.

The 90° phase shift network, realized by RC networks, is capable of operating over a wide frequency range. Even though their frequency characteristics are optimized for cellular band, the part can also be used in other applications in a different band. In such cases, designers have to test the part experimentally to find out the performance, such as sideband suppression, carrier suppression, and image rejection.

Crystal Oscillator

The crystal oscillator (XTAL_1 and XTAL_2 pins) is used to provide reference frequency between 10 and 45MHz for the phase detector and the three on-chip clocks. It can be configured as a crystal oscillator using external crystal and capacitors, or it can be driven by an external source. In the latter case, pin XTAL_2 can be left floating. Information regarding crystal oscillator design can be found in Philips RF application note, #AN 1982, "Apply the Oscillator of the SA602 in Low-Power Mixer Applications."

VCO

The VCO, together with the phase detector, the divider and external low-pass filter, can form a PLL for the transmit offset frequency. The image reject mixer down-converts the TXLO signal to the RF carrier by the amount of VCO frequency. Thus, the TXLO frequency should be the desired channel frequency plus the IF offset generated by the VCO. Notice that the part will not function if the VCO section is not used.

The VCO is designed for generating IF frequency between 90MHz and 140MHz. Together with an external varactor diode and resonator, it can be configured as an oscillator as shown in Figure 11.

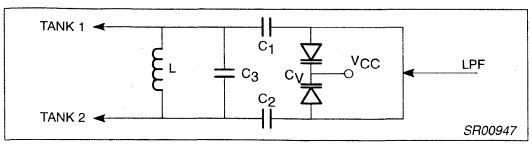


Figure 11. VCO Tank Circuit

The resonant frequency of such a circuit is

$$f_{VCO} = \frac{1}{2\pi\sqrt{LC_T}} \quad \text{(EQ. 3)}$$

where $C_T = (C_1 // C_2 // C_V) + C_3$. C_V is a varactor diode of which capacitance changes linearly with the voltage across it.

Calculation:
$C_1 = C_2 = 33pF$
$C_3 = 5.6pF$
$C_V = 33.5pF$ @ 2.5V
$L = 100nH$

$C_T = 5.6 + (1/33 + 1/33 + 1/33.5)^{-1} = 16.7pF$

$$f_{VCO} = \frac{1}{2\pi\ (100e\text{-}9 \cdot 16.7e\text{-}12)^{0.5}} = 123MHz$$

On the demoboard, a 1:1 ratio RF transformer is also included to allow single-ended external source driving differential inputs when the VCO is not used.

When designing the VCO, careful PCB layout has to be made. Traces have to be short to avoid the parasitic capacitance and inductance which may cause unwanted oscillation. Referring to EQ. 3, there is a large combination of L and C_T values that will give the same resonant frequency. If undesired spurs are found in the design due to PCB layout, experimenting with a different set of LC values may sometimes solve the problem.

Output impedance matching

The equivalent output impedance at the DUALTX pin is approximately equal to 600Ω in parallel with 2pF at 830MHz. It has to be matched properly to generate maximum power into a 50Ω load (e.g. SAW filter). Figure 12 shows the recommended matching network. The shunt inductor (L1) is used to provide maximum swing at the output (short at DC) and also provide reactance to make the real impedance 50Ω looking into the matching network. The remaining negative reactance is canceled by the series inductor (L2). The values used on the demoboard can be used as a reference but may not be suitable if a different layout is implemented. The two shunt capacitors are included to bypass the high frequency RF signal, avoiding direct coupling into V_{CC}. The series AC coupling capacitor is used to maintain the proper bias for the output stage. Their values are big enough to be left out in impedance matching calculation.

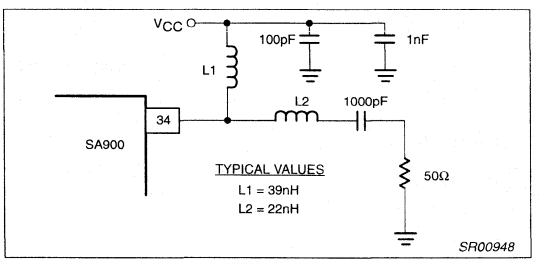
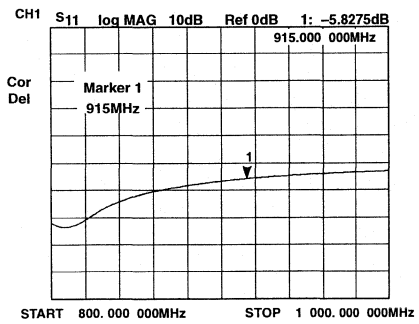
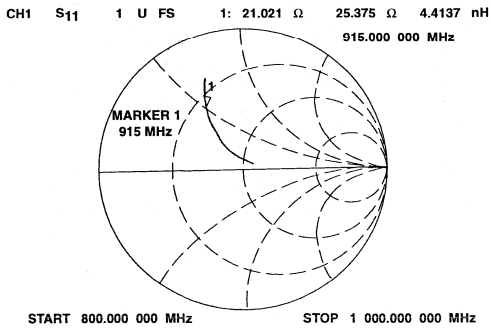


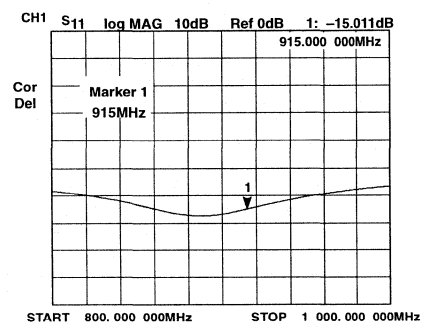
Figure 12. DUALTX Output Matching Network

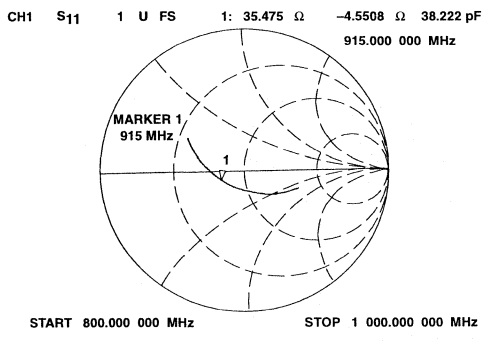
Using a network analyzer to measure the S characteristic is necessary for obtaining optimum matching which generates maximum output power. Figure 13a-d shows how to match the output impedance to a 50Ω load at 915MHz. First, calibrate the network analyzer to the DUALTX SMA connector on the demoboard. Then, short the point where the series inductor is located and use the DELAY feature of the network analyzer to move the point of reference in the Smith Chart to the leftmost point. Now the network analyzer is calibrated to the beginning of the matching network, not just the SMA connector. The frequency response (Figure 13a) shows that the "dip" is around 830MHz, the frequency where the board was originally matched. The Smith Chart shows that it requires less inductance to bring the marker to the center of the chart (50Ω). By using a 15nH series inductor, the "dip" was moved closer to 915MHz (-15dB) and a better matching is achieved (Figure 13b).





a. S_{11} Response and Smith Chart when L2 = 22nH





b. S_{11} Response and Smith Chart when L2 = 15nH

SR00949

Figure 13.

On-Chip Clocks

The crystal oscillator is buffered to provide three external clock signals: CLK1, CLK2, and MCLK. Table 1 shows the divide ratio and the controlling mechanism:

Table 5.

CLK1	divide by 3	X (bit 18) = 1
	divide by 1	X (bit 18) = 0
CLK2	divide by 2	Y (bit 19) = 1
	divide by 1	Y (bit 19) = 0
MCLK	divide by 4	CLKSET pin = V_{CC}
	divide by 5	CLKSET pin = $V_{CC}/2$
	divide by 1	CLKSET pin grounded

CLK1 is usually used for the system synthesizer (e.g. SA7025) reference. Since MCLK is active all the time, it is ideal for providing the master clock for the microcontroller. When the device is in STANDBY mode, CLK1 and MCLK provide the clock signals necessary for receiving RF signals. CLK2 can also be used as a clock for digital signal processing (DSP) chip.

Modes of Operation

The SA900 is intended for either AMPS mode (analog cellular) or DUAL mode (digital cellular, IS-54) operation. When the device is running in AMPS mode, the I/Q modulator, variable gain amplifier (VGA) and phase shifter are disabled. The fixed gain amplifier is powered up during AMPS mode operation. However, since the divide ratio is too low (6, 7 or 8), the comparison frequency of the on-board PLL is too high, making it very difficult for the loop bandwidth to be less than 300Hz for analog FM modulation.

The device includes two power saving modes of operation which disable partial circuitry to reduce the power consumption of the overall chip. The SLEEP mode disables all the circuitry except the master clock (MCLK pin) of the SA900. The STANDBY mode shuts down everything except the TXLO buffer, MCLK, and CLK1, which allows the system synthesizer (e.g. SA7025) to continue running. These two power saving modes are common to both AMPS and DUAL mode operation. The SA900 draws 60mA in DUAL mode, reduced to 3mA and 8mA, respectively, in SLEEP and STANDBY modes.

TXEN pin is for hardware powering down the modulator and synthesizer. The falling edge of the signal disables the modulator and synthesizer while the rising edge enables the modulator. To power down the synthesizer using software, send a data word with SE bit set to '0' ('1' for enable). The synthesizer will be disabled right after the strobe signal is transmitted. Either SE or TXEN going low will turn off the synthesizer. This operation is common to both AMPS and DUAL mode.

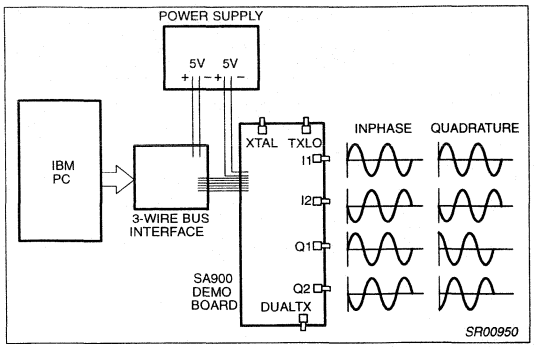


Figure 14. In-phase and Quadrature Modulation Test

PERFORMANCE OF THE SA900

Performance Criteria

Since the I/Q modulator is a universal transmitter, measuring only the frequency stability and modulation index of a generated FM signal would not be useful for other modulation schemes. Measurement parameters should be general enough so that they can represent the performance of modulators when applying different types of modulation and allow fair comparisons among different I/Q modulators. Based on this idea, two measurement techniques, in-phase modulation and quadrature modulation, are used for evaluating I/Q modulators.

The in-phase modulation relies on injecting two equal frequencies and phase signals at f_{mod} into the I and Q inputs. The result of this modulation is two sidebands appearing at f_{mod} offset from the carrier, with the carrier totally suppressed. This is also known as double-sideband (DSB) conversion. The quadrature modulation requires two equal frequencies (but 90° out-of-phase signals) being injected into the I and Q inputs. The result is a single-sideband suppressed carrier (SSB-SC) signal with either the upper or lower sideband at f_{mod} carrier offset being suppressed. This is also known as single-sideband (SSB) up-conversion. Figure 14 summarizes these two tests.

In a practical system, imperfection of an I/Q modulator is directly related to these two measurements. Sideband and carrier suppression from the quadrature modulation test will show the amount of gain imbalance, phase imbalance, and DC offset. On the other hand, intermodulation product suppression from the in-phase modulation test will show the linearity of an I/Q modulator. When making measurements, it is important to have well-balanced I and Q baseband modulating signals for measurement since the signal imperfection will translate into degradation in sideband and carrier suppression.

Performance Graphs

In making those measurements for the demoboard, the following parameters were used:

In-phase modulation:

PIN 43 I1=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=0°

PIN 42 I2=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=180°

PIN 41 Q1=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=0°

PIN 40 Q2=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=180°

Quadrature modulation:

PIN 43 I1=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=0°

PIN 42 I2=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=180°

PIN 41 Q1=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=0°

PIN 40 Q2=400mV$_{P-P}$, DC=V_{CC}/2 at 200kHz, Phase=270°

Figures 15a and 15b illustrate what the typical output spectrum would be if in-phase and quadrature modulation were applied to an I/Q modulator. Quadrature modulation will produce lower sideband (LSB) or upper sideband (USB) signal, depending on the phase angle between the I and Q signals. The SA900 was designed to have USB suppressed when the I signal is leading the Q signal. The undesired signals are carrier breakthrough and the harmonic products of the baseband modulating signals sitting at

$f_c \pm nf_{mod}$, where n is an integer ≥2.

Referring to Figure 15a, the output power is 1.3dBm (cable loss = 0.7dB) for the LSB while better than -38dBc of carrier, sideband, and harmonics suppression is measured. The USB better than -26dBc implies the residual AM of the transmit signal is better than 5%, a requirement of the IS-54 specification.

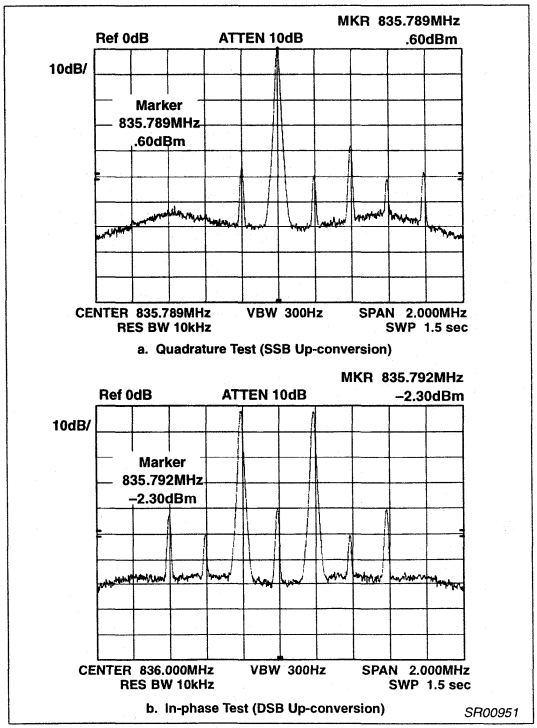


Figure 15.

In-phase modulation test will generate both LSB and USB. Beside these two tones, the carrier breakthrough and the harmonics, intermodulation (IM) products will all appear at the output. The odd IM products are dominant, and they satisfy the following rules:

Let $f_1 = f_c - f_{mod}$, $f_2 = f_c + f_{mod}$

3rd order IM:	$2f_1 - f_2 = f_c - 3f_{mod}$,	$2f_2 - f_1 = f_c + 3f_{mod}$
5th order IM:	$3f_1 - 2f_2 = f_c - 5f_{mod}$,	$3f_2 - 2f_1 = f_c + 5f_{mod}$
7th order IM:	$4f_1 - 3f_2 = f_c - 7f_{mod}$,	$4f_2 - 3f_1 = f_c + 7f_{mod}$

Referring to Figure 15b, both LSB and USB are -1.6dBm (cable loss = 0.7dB) in power, which is 3dB less than the measured power for the quadrature modulation test. The IM3 is better than -35dBc. Much higher order IM products are totally suppressed.

Amplitude and phase unbalance

Both amplitude and phase unbalance (error) of an I/Q modulator can be calculated directly from the SSB performance plots. Assume phase error equals ϕ radian and amplitude error equals K, the sideband suppression, X, in dBc can be expressed as follows (see APPENDIX for derivation):

$$\text{SSB suppression, } X(\text{dBc}) = 10\log\left(\frac{K^2 + 2\cdot K\cdot\cos(\phi) + 1}{K^2 - 2\cdot K\cdot\cos(\phi) + 1}\right) \quad \text{(EQ. 4)}$$

Collecting the like terms and express ϕ in terms of K and X, it becomes:

$$\phi = \cos^{-1}\left(\frac{10^{x/10}\cdot K^2 + 10^{x/10} - 1 - K^2}{2\cdot K + 2\cdot K\cdot 10^{x/10}}\right) \quad \text{(EQ. 5)}$$

For a given X, there will be a set of ϕ and K that satisfies EQ. 5. We can represent this relationship graphically, as shown in Figure 16. The contours show the phase and amplitude errors for SSB suppression, X, from -44 to -26dBc. When X equals -40dBc, phase error is less than 1.2° with a 0dB amplitude error. By the same token, the amplitude error is less than 0.2dB with a 0° phase error.

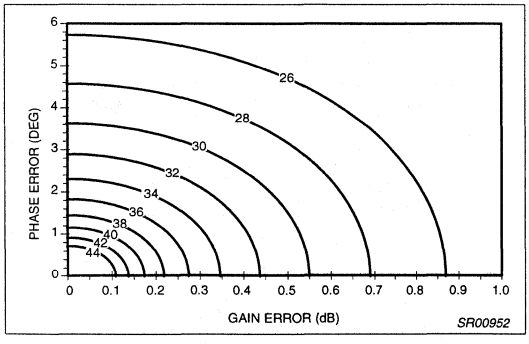


Figure 16. SSB Suppression Contours

Spectral mask

To fully characterize the performance of an I/Q modulator, measurements of the power spectral density of various digital modulation schemes have to be made. Figures 17a and 17b show the measured spectral masks of IS-54 and PDC standards, which designate $\pi/4$-DQPSK as the modulation format.

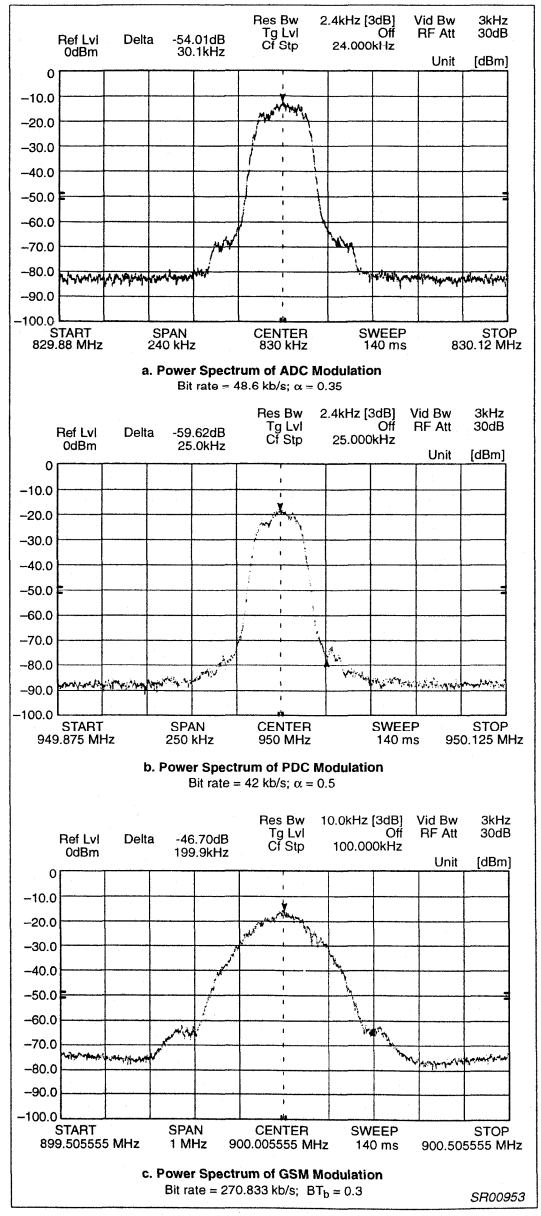


Figure 17.

GMSK is a digital modulation scheme widely used for wireless and mobile communications. Figure 17c shows the spectral mask of the modulation format required by GSM, the digital cellular standard in Europe. At 200kHz and 300kHz carrier offset, the power of the

signal is suppressed by 46dB and 58dB, respectively, which is well within the GSM specification.

Power ON time

The power ON time for the SA900 is mainly determined by the loop bandwidth of the on-board PLL frequency synthesizer. It can be measured by using the HP 53310A Modulation Domain Analyzer set to the EXTERNAL TRIGGERED mode. The STROBE signal from 3-wire bus is used to trigger the equipment. Figure 18 shows that the part can be powered up and locked in about 62µs.

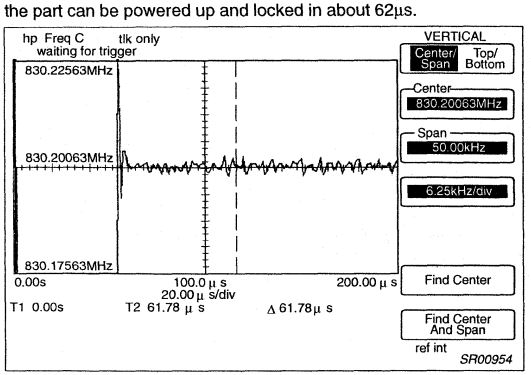


Figure 18. Power ON Time Measurement

ISM band application

The FCC has recently assigned three bands for ISM type of application. The one below 1GHz is from 902 to 928MHz. This band becomes very attractive because users are allowed, without having a license, to transmit up to 1 Watt of power when frequency hopping or direct sequence CDMA is used. The wide bandwidth nature of the SA900 fits well into this application. Figures 19a and 19b are the output spectrum of the SA900 showing how well the image reject mixer works. A common IF (45MHz) was chosen to be the offset frequency, and then injected externally into the VCO pins. The closest images are sitting at 45MHz apart and are better than -36dBc.

COMPONENTS FUNCTION

C241, C242, C243, C245, C246 - Supply bypassing capacitors

C247 - provides AC ground for TXLO2 pin

C249 - AC couples an external signal into TXLO1 pin

C253, C254, C255 - part of the LC tank circuit

C263 - AC couples an external signal into XTAL1 pin

C267, C269 - part of the PLL low-pass filter

C281, C287, C288 - AC coupling capacitors for the clocks

C301 - AC coupling capacitor for the DUALTX pin

C305, C306 - Bypass RF signal coming from DUALTX pin

C312, C313, C314 - AC coupling capacitors

C370, C371 - AC couples an external signal into TANK1 and TANK2 pins when on-board PLL is not used

L252 - part of the LC tank circuit

L304, L372 - matching network for the DUALTX output

R260 - termination resistor

R262 - current setting resistor for the charge pump

R264, R266 - part of the PLL low-pass filter

R274 - jumper

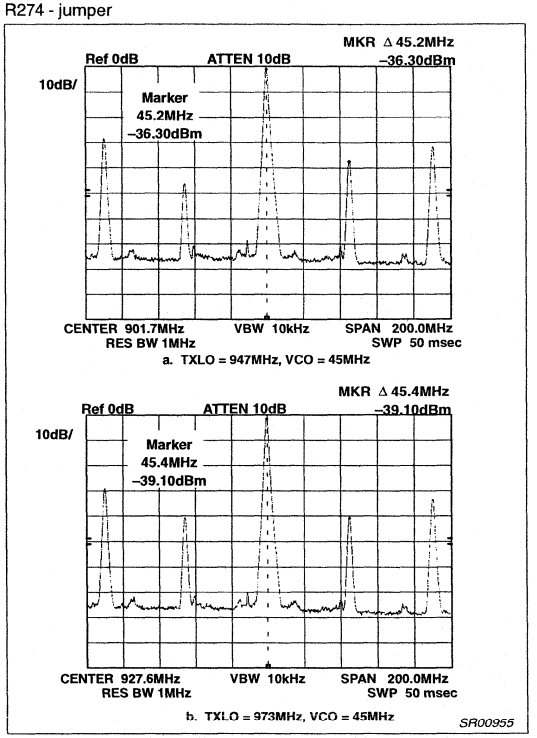


Figure 19. Output Spectrum of the SA900 in the ISM Band

R349, R350 - make up a voltage divider for selecting divide ratio of the MCLK

R352 - termination resistor

R333, 358 - isolation resistors between the LC tank and the PLL low-pass filter

FREQUENTLY ASKED QUESTIONS

Q. What is the bandwidth of the phase shifter for generating I/Q carriers?

A. The bandwidth is between 820 and 920MHz. The part is still functional below 820MHz and above 920MHz, but the carrier and sideband suppression are not guaranteed. In addition, the DUALTX output matching network needs to be optimized for a different frequency.

Q. Can I frequency modulate (FM) the on-board VCO to generate RF signal for AMPS system?

A. Since the divide ratio for the VCO is too low, it is very difficult to obtain the required loop bandwidth (<300Hz) to do AMPS modulation.

Q. What signals constitute the spurious output referred to under the DUALTX function of the AC electrical characteristics in the data sheet?

A. Those spurs could be N*TXLO, N*VCO, TXLO+VCO, N*XO, and TXLO ±N*VCO.

Q. Can external circuitry be added or modified to reduce the broadband noise floor below -136dBm/Hz?
A. Customers can put a bandpass SAW filter at the output of the TXLO to improve the broadband noise floor.

Q. Can the SA900 generate BPSK signal?
A. Yes, it can. Feed the baseband signal into I1 and I2 and leave Q1 and Q2 open or tie them to V_{CC} /2.

Q. What is the response of the image rejection filter?
A. It is actually a SSB mixer; not an image rejection filter.

Q. What happens if the VCO is not used?
A. There will not be any signal at the DUALTX and AMPS output if the VCO is not used.

REFERENCES:

"Implementation of a 900 MHz Transmitter System Using Highly Integrated ASIC", Wing S. Djen and Prasanna M. Shah, Proceedings of the 44th IEEE Vehicular Technology Conference, June 1994, pp. 1341-1345.

"Digital and Analog Communications Systems," Leon W. Couch II, Macmillan, 1990.

"Cellular System Dual-Mode Mobile Station-Base Station Compatibility Standard", IS-54-B, EIA/TIA, April 1992.

"Physical Layer on the Radio-Path", GSM Standard, July 1988.

"π/4-QPSK MODEMS for Satellite Sound/Data Broadcast Systems", Chia-Liang Liu and Kamilo Feher, IEEE Transactions on Broadcasting, March 1991, pp. 1-8.

"PCD5070 GSM Baseband Interface", Preliminary specification, Philips Semiconductors, September, 1992.

APPENDIX

Assume an imperfect I/Q modulator with gain error, K, and phase error, ϕ, modulated by quadrature I/Q signals (SSB up-conversion) wm. Then the signal, s(t), at the output of the I/Q modulator becomes,

$$s(t) = K\cos(\omega_c t + \phi)\cos(\omega_m t) - \sin(\omega_c t)\cos(\omega_m t + 90^o) \quad \text{(EQ. A.1)}$$

Using trigonometric identity and let $\omega c - \omega_m = A$ and $\omega_c + \omega_m = B$, we obtain,

$$s(t) = \frac{K}{2}\cos[At + \phi] + \frac{K}{2}\cos[Bt + \phi] + \frac{1}{2}\cos[At] - \frac{1}{2}\cos[Bt] \quad \text{(EQ. A.2)}$$

Assume the information is in LSB, i.e. A, and the spur is the USB, i.e., B, we have,

$$\text{Signal} = \frac{K}{2}\cos A\cos\phi + \frac{1}{2}\cos A - \frac{K}{2}\sin A\sin\phi \quad \text{(EQ. A.3)}$$

$$\text{Noise} = \frac{K}{2}\cos B\cos\phi + \frac{1}{2}\cos B - \frac{K}{2}\sin B\sin\phi \quad \text{(EQ. A.4)}$$

To find the power, we have to evaluate the envelope (amplitude) of these two signals. Recall that for any given bandpass signal in rectangular form,

Bandpass signal = X cos ωt - Y sin ωt,

the envelope is

Envelope = $(X^2 + Y^2)^{0.5}$

Therefore, from EQ. A.3 and A.4,

$$\text{Signal} = \left[\left(\frac{K}{2}\cos\phi + \frac{1}{2}\right)^2 + \left(\frac{K}{2}\sin\phi\right)^2\right]^{0.5} \quad \text{(EQ. A.5)}$$

$$\text{Noise} = \left[\left(\frac{K}{2}\cos\phi - \frac{1}{2}\right)^2 + \left(\frac{K}{2}\sin\phi\right)^2\right]^{0.5} \quad \text{(EQ. A.6)}$$

Finally, the S/N ratio can be found by taking 20 log the ratio of EQ. A.5 and A.6.

$$\frac{S}{N} = 10\log\left(\frac{K^2 + 2K\cos\phi + 1}{K^2 - 2K\cos\phi + 1}\right)$$

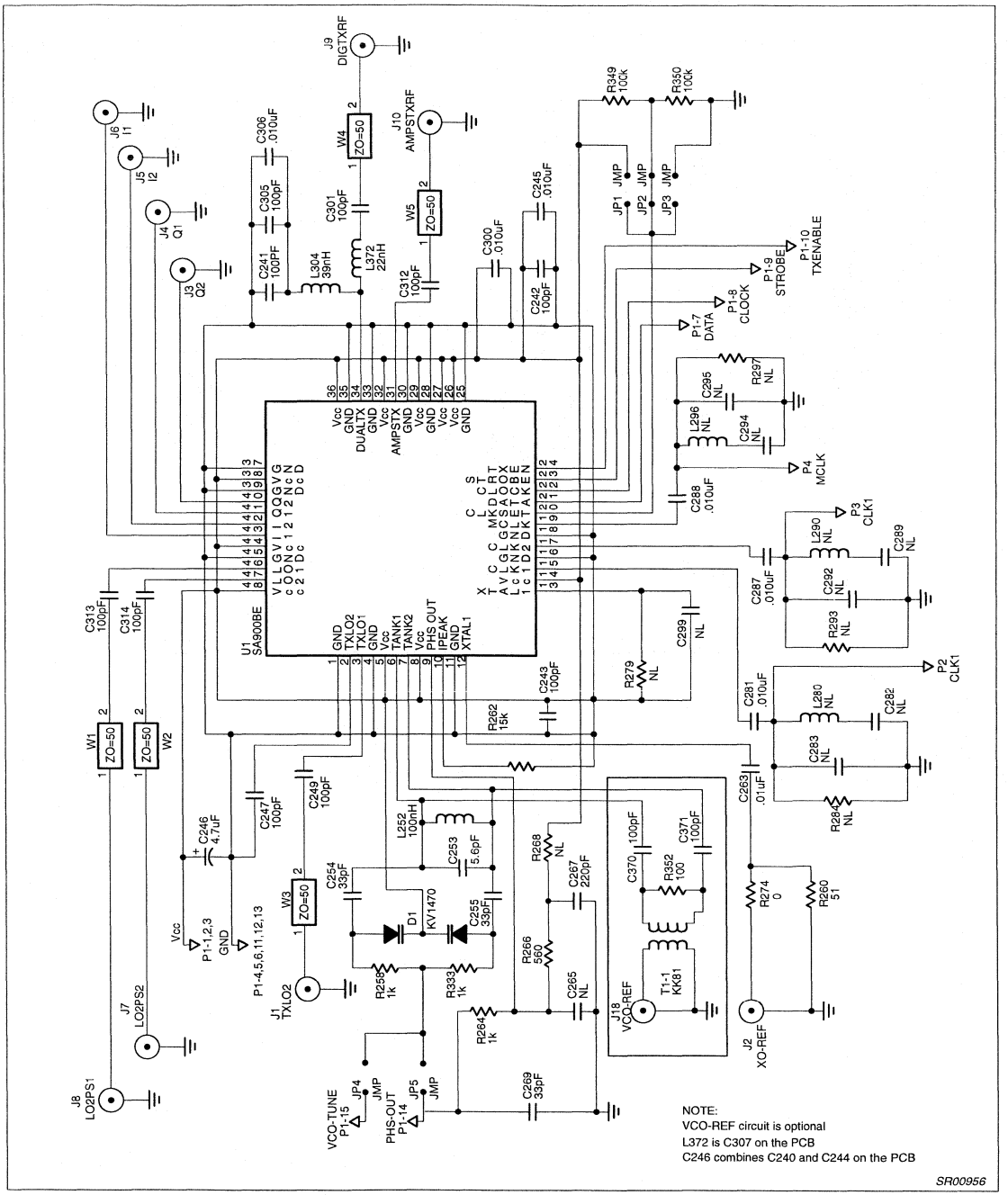


Figure 20. SA900 Demoboard

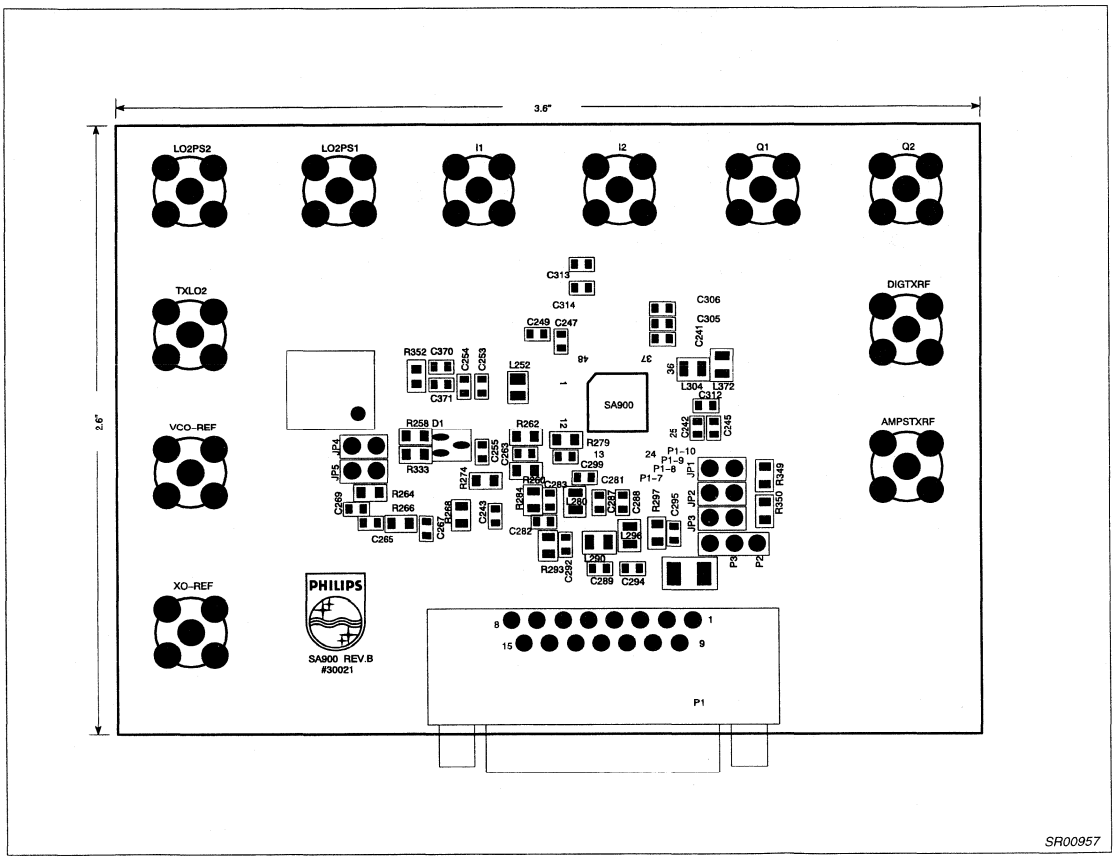


Figure 21. SA900 Board Layout

Table 6. Customer Application Component List for SA900BE

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	5.6pF	50V	C253	Cap. cer. 0603 NPO ±0.25pF	Garrett	Rohm	MCH185A5R6CK
3	33pF	50V	C254, C255, C269	Cap. cer. 0603 NPO ±5%	Garrett	Rohm	MCH185A330JK
13	100pF	50V	C241, C242, C243, C247, C249, C300, C301, C305, C312, C313, C314, C370, C371	Cap. cer. 0603 NPO ±5%	Garrett	Rohm	MCH185A101JK
1	1000pF	50V	C301	Cap. cer. 0603 X7R ±10%	Garrett	Rohm	MCH185C102KK
1	2200pF	50V	C267	Cap. cer. 0603 X7R ±10%	Garrett	Rohm	MCH185C222KK
6	0.01µF	25V	C245, C263, C281, C287, C288, C306	Cap. cer. 0603 X7R ±10%	Garrett	Philips	MCH182C103KK
1	4.7µF	10V	C246	Tant. chip cap. B 3528 ±10%	Garrett	Philips	49MC475B010KOAS
8	NL		C265, C282, C283, C289, C292, C294, C295, C299				
Surface Mount Resistors							
1	0Ω		R274	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW000E
1	51Ω		R260	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW510E
1	100Ω		R352	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW101E
1	560Ω		R266	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW561E
1	1KΩ		R258, R264, R333	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW102E
1	15KΩ		R262	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW153E
2	100KΩ		R349, R350	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW104E
Surface Mount Diodes							
1			D1	SMD Diode (Varactor)	Digikey	TOKO	KV1470TR00
Surface Mount Inductors							
1	0.022µH		L372	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R022M
1	0.039µH		L304	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R039M
1	0.10µH		L252	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R10M
Surface Mount Integrated Circuits							
1			U1	I/Q Transmit modulator	Philips	Philips	SA900BE
Miscellaneous							
1			K353	RF Transformer	Mini-Circuits	Mini-Circuits	T1-1 KK81
11			J1, J2, J3, J4, J5, J6, J7, J8 ,J9, J10, J18	SMA Right Angle Jack Receptacle	Newark	EF Johnson	142-0701-301
5			JP1, JP2, JP3, JP4, JP5	straight, dual row	Newark	IPI	929836-01-36-ND
1			P1	15 pins receptacle D-sub. conn.	Newark	Dupont	51F2456
1				Printed circuit board	Philips	Philips	SA900-30021
66 Total Parts							

New low-power single sideband circuits AN1981

Author: Robert J. Zavrell Jr.

INTRODUCTION

Several new integrated circuits now permit RF designers to resurrect old techniques of single-sideband generation and detection. The high cost of multi-pole crystal filters limits the use of the SSB mode to the most demanding applications, yet the advantages of SSB over full-carrier AM and FM are well documented (Ref 1 &2). The use of multi-pole filters can now be circumvented by reviving some older techniques without sacrificing performance. This has been made possible by the availability of some new RF and digital integrated circuits.

DESCRIPTION

Figure 1 shows the frequency spectrum of a 10MHz full-carrier double-sideband AM signal using a 1kHz modulating tone. This well-known type of signal is used by standard AM broadcast radio stations. Full-carrier AM's advantage is that envelope detection can be used in the receiver. Envelope detection is a simple and economical technique because it simplifies receiver circuitry. Figure 2 shows the time domain "envelope" of the same AM signal.

The 1kHz tone example of Figures 1 and 2 serves as a simple illustration of an AM signal. Typically, the sidebands contain complex waveforms for voice or data communications. In the full-carrier double sideband mode (AM), all the modulation information is contained in both sidebands, while the carrier "rides along" without contributing to the transfer of intelligence. Only one sideband without the carrier is needed to effectively transmit the modulation information. This mode is called "single-sideband suppressed carrier". Because of its reduced bandwidth, it has the advantages of improved spectrum utilization, better signal-to-noise ratios at low signal levels, and improved transmitter efficiency when compared with either FM or full-carrier AM. A finite frequency allocation using SSB can support three times the number of channels when compared with comparable FM or AM full-carrier systems.

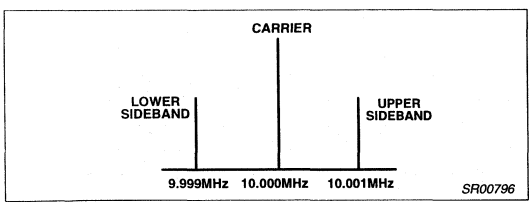


Figure 1. Frequency Domain Display of a 10MHz Carrier AM Modulated by a 1kHz Tone (Spectrum Analyzer Display)

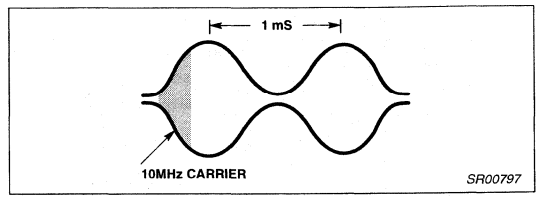


Figure 2. Time Domain Display of the Same Signal Shown in Figure 1. (Oscilloscope Display)

There are three basic methods of single-sideband generation. All three use a balanced modulator to produce a double-sideband suppressed carrier signal. The undesired sideband is then removed by phase and amplitude nulling (the phasing method), high Q multi-pole filters (the filter method), or a "third" method which is a derivation of the phasing technique called here the "Weaver" method for the apparent inventor. The reciprocal of the generator functions is employed to produce sideband detectors. Generators start with audio and produce the SSB signal; detectors receive the SSB signal and reproduce the audio. Since the sideband signal is typically produced at radio frequencies, it can be amplified and applied to an antenna or used as a subcarrier.

Reproduction of the audio signal in a full-carrier AM receiver is simplified because the carrier is present. The signal envelope, which contains the carrier and the sidebands, is applied to a non-linear device (typically a diode). The effect of envelope detection is to multiply the sideband signal by the carrier; this results in the recovery of the audio waveform. The mathematical basis for this process can be understood by studying trigonometric identities.

Since the carrier is not present in the received SSB signal, the receiver must provide it for proper audio detection. This signal from the local oscillator (LO) is applied to a mixer (multiplier) together with the SSB signal and detection occurs. This technique is called product detection and is necessary in all SSB methods. A major problem in SSB receivers is the ability to maintain accurate LO frequencies to prevent spectral shifting of the audio signal. Errors in this frequency will result in a "Donald Duck" sound which can render the signal unintelligible for large frequency errors.

Theory of Single-Sideband Detection

Figures 3 through 8 illustrate the three methods of SSB generation and detection. Since they are reciprocal operations, the circuitry for generation and detection is similar with all three methods. Duplication of critical circuitry is easy to accomplish in transceiver applications by using appropriate switching circuits.

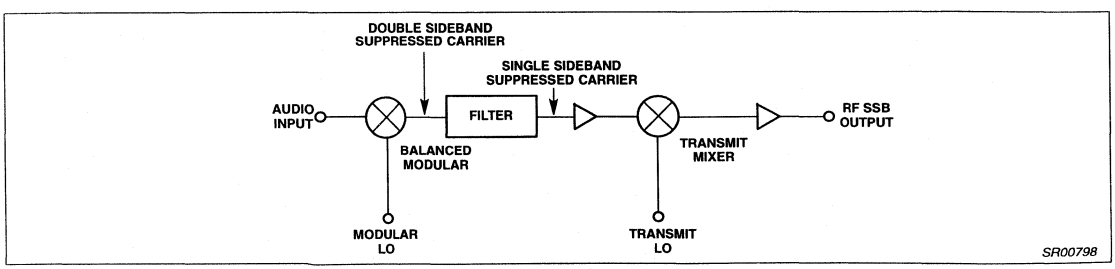


Figure 3. Filter Method SSB Generator

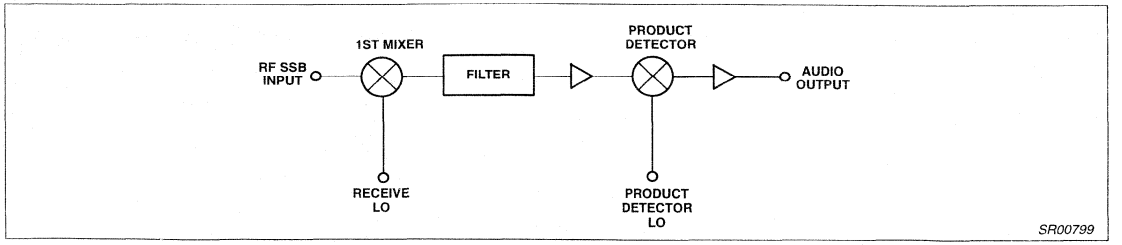


Figure 4. Filter Method SSB Detector

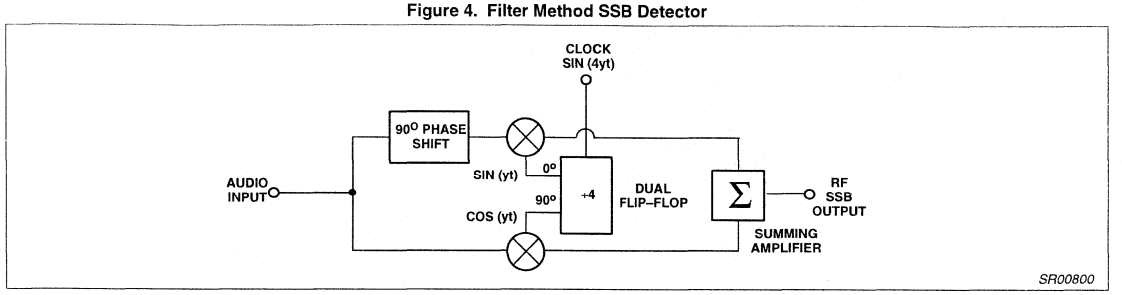


Figure 5. Phasing Method Generator

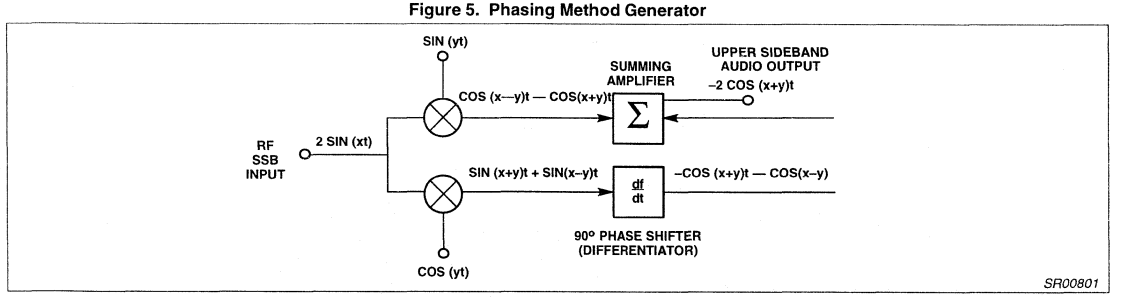


Figure 6. Phasing Method Detector with Simplified Mathematical Model

Figures 3 and 4 show the generation and detection techniques employed in the filter method. In the generator a double sideband signal is produced while the carrier is eliminated with the balanced modulator. Then the undesired sideband is removed with a high Q crystal bandpass filter. A transmit mixer is usually employed to convert the SSB signal to the desired output frequency. The detection scheme is the reciprocal. A receive mixer is used to convert the selected input frequency to the IF frequency, where the filter removes the undesired SSB response. Then the signal is demodulated in the product detector. A major drawback to the filter method is the fact that the filter is fixed-tuned to one frequency. This necessitates the receive and transmit mixers for multi-frequency operation.

Figures 5 and 6 show block diagrams of a generator and demodulator which use the phase method. Figure 6 also includes a mathematical model. The input signal (Cos(Xt)) is fed in-phase to two RF mixers where "X" is the frequency of the input signal. The other inputs to the mixers are fed from a local oscillator (LO) in quadrature (Cos(Yt) and Sin(Yt)), where "Y" is the frequency of the LO signal. By differentiating the output of one of the mixers and then summing with the other, a single sideband response is obtained. Switching the mixer output that is differentiated will change the selected sideband, upper (USB) or lower (LSB). In most cases the mixer outputs will be the audio passband (300 to 3000Hz). Differentiating the passband involves a 90 degree phase shift over more than three octaves. This is the most difficult aspect of using the phasing method for voice band SSB.

For voice systems, difficulty of maintaining accurate broadband phase shift is eliminated by the technique used in Figures 7 and 8. The "Weaver" method is similar to the phasing method because both require two quadrature steps in the signal chain. The difference between the two methods is that the Weaver method uses a low frequency (1.8kHz) subcarrier in quadrature rather than the broad-band 90 degree audio phase shift. The desired sideband is thus "folded over" the 1.8kHz subcarrier and its energy appears between 0 and 1.5kHz. The undesired sideband appears 600Hz farther away between 2.1 and 4.8kHz. Consequently, sideband rejection is determined by a low-pass filter rather than by phase and amplitude balance. A very steep low-pass response in the Weaver method is easier to achieve than the very accurate phase and amplitude balance needed in the phasing method. Therefore, better sideband rejection is possible with the Weaver method than with the phasing method.

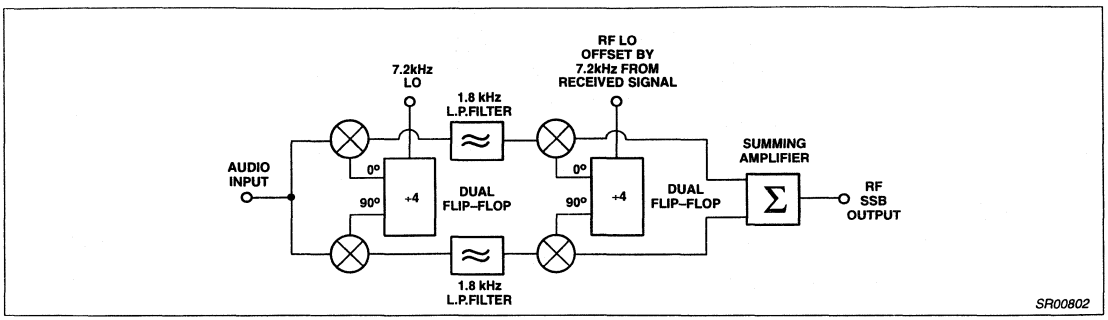


Figure 7. Weaver Method Generator

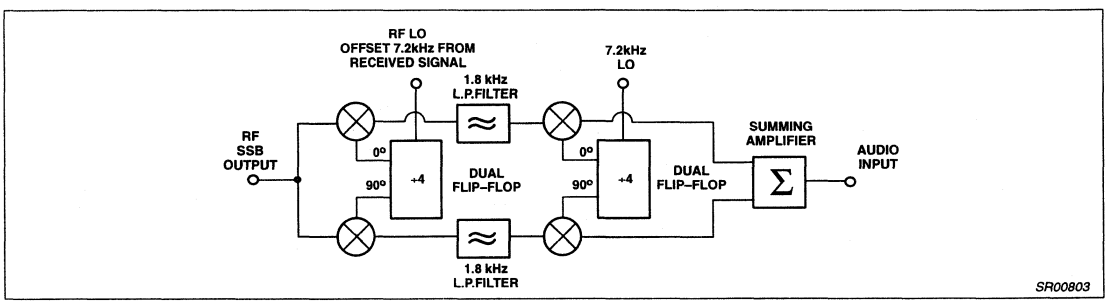


Figure 8. Weaver Method Detector

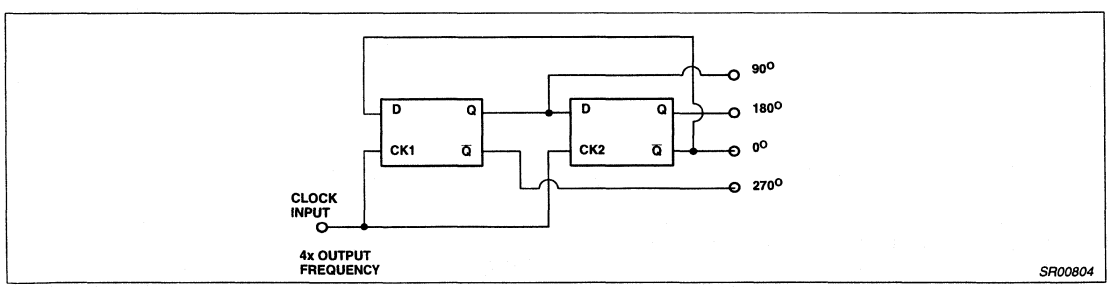


Figure 9. Dual Flip-Flop Quadrature Synthesis

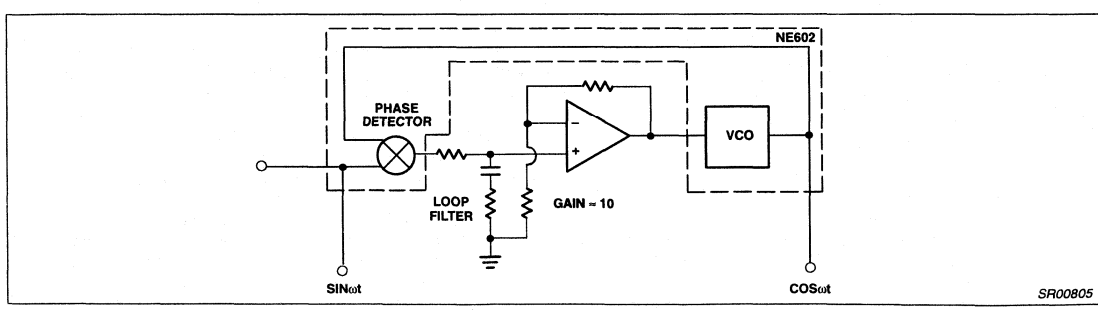


Figure 10. PLL Quadrature Synthesis

Quadrature Dual Mixer Circuits

One of the two critical stages in the phasing method and both critical stages in the Weaver method require quadrature dual mixer circuits. Figures 9 and 10 show two methods of obtaining quadrature LO signals for dual mixer applications. Other methods exist for producing quadrature LO signals, particularly use of passive LC circuits. LC circuits will not maintain a quadrature phase relationship when the operating frequency is changed. The two illustrated circuits are inherently broad-banded; therefore, they are far more flexible and do not require adjustment. These circuits are very useful for SSB circuits, but also can be applied to FSK, PSK, and QPSK digital communications systems.

The SA602 is a low power, sensitive, active, double-balanced mixer which shows excellent phase characteristics up to 200MHz. This makes it an ideal candidate for this and many other applications.

The circuit in Figure 9 uses a divide-by-four dual flip-flop that generates all four quadratures. Most of the popular dual flip-flops can be used in different situations. The HEF4013 CMOS device uses very little power and can maintain excellent phase integrity at clock rates up to several megahertz. Consequently, the HEF4013 can be used with the ubiquitous 455kHz intermediate frequency with excellent power economy. For higher clock rates (up to 120MHz for up to 30MHz operation), the fast TTL 74F74 is a good choice. It has been tested to 30MHz operating frequencies with good results (>30 dB SSB rejection). At lower frequencies (5MHz) sideband rejection increases to nearly 40dB with the circuits shown. The ultimate low frequency rejection is mainly a function of the audio phase shifter. Better performance is possible by employing higher tolerance resistors and capacitors.

The circuit in Figure 10 shows another technique for producing a broadband quadrature phase shift for the LO. The advantage of this circuit over the flip-flops is that the clock frequency is identical to the operating frequency; however, phase accuracy is more difficult to achieve. A PLL will maintain a quadrature phase relationship when the loop is closed and the VCO voltage is zero. The DC amplifier will help the accuracy of the quadrature condition by presenting gain to the VCO control circuit. The other problem that can arise is that PLL circuits tend to be noisy. Sideband noise is troublesome in both SSB and FM systems,

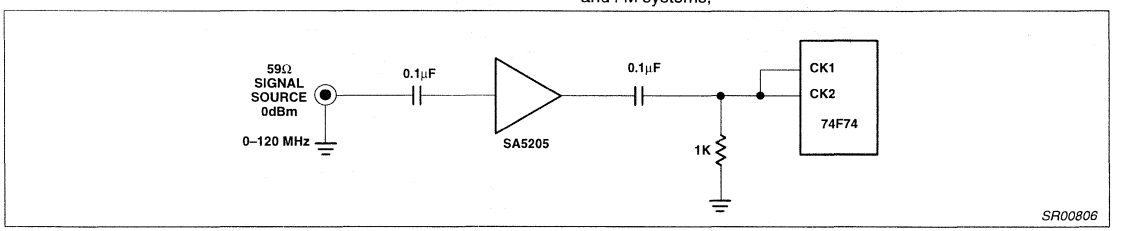


Figure 11. FAST TTL Driver from Analog Signal Source Using SA5205

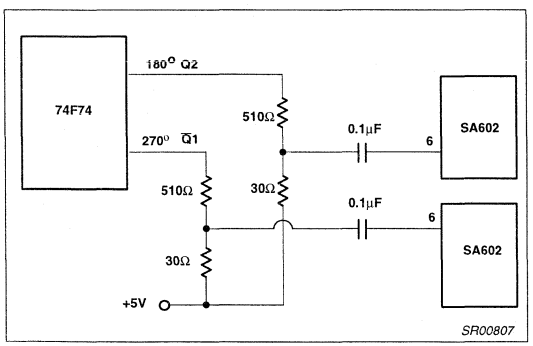


Figure 12. Interface Circuitry Between 74F74 and the SA602s

but SSB is less sensitive to phase noise problems in the LO.

Figure 11 shows a circuit that is effective for driving the 74F74, or other TTL gates, with a signal generator or analog LO. The SA5205 provides about 20dB gain with 50Ω input and output impedances from DC to 450MHz. Minimum external components are required. The 1kΩ resistor is about optimum for "pulling" the input voltage down near the logic threshold. A 50Ω output level of 0dBm can be used to drive the SA5205 and 74F74 to 100MHz. Two SA5205s can be cascaded for even more sensitivity while maintaining extremely wide bandwidth. An advantage of using digital sources for the LO is that low-frequency power supply ripple will not cause hum in the receiver front end. This is a common problem in direct conversion designs.

Figure 12 shows the interface circuitry between the 74F74 and the SA602 LO ports. The total resistance reflects conservative current drain from the 74F74 outputs, while the tap on the voltage divider is optimized for proper SA602 operation. The low signal source impedance further helps maintain phase accuracy, and the isolation capacitor is miniature ceramic for DC isolation.

Audio Amplifiers and Switching

Using active mixers (SA602) in these types of circuits gives conversion gain, typically 18dB. More traditional applications use passive
diode ring mixers which yield conversion loss, typically 7dB. Consequently, the detected audio level will be about 25dB higher when using the SA602. This fact can greatly reduce the first audio stage noise and gain requirements and virtually eliminate the "microphonic" effect common to direct conversion receivers. Traditional direct conversion receivers use passive audio LC filters at the mixer output and low noise, discrete JFETs or bipolars in the first stages. The very high audio sensitivity required by these amplifiers makes them respond to mechanical vibration – thus the "microphonics" result. The conversion gain allows use of a simple op amp stage (Figure 13) set up as an integrator to eliminate ultra-sonic and RF instability. The SA5534 is well known for its low noise, high dynamic range, and excellent audio characteristics (Reference 12) and makes an ideal audio amp for the 602 detector.

The sideband select function is easily accomplished with an HEF4053 CMOS analog switch. This triple double-pole switch drives the phase network discussed in the next section and also chooses one of two amplitude balance potentiometers, one for each sideband. Figure 14 illustrates this circuit. A buffer op amp is used

with the two sideband select sections to reduce THD, maintain amplitude integrity, and not change the filter network input resistance values. The gain distribution within both legs of the receiver was found to be very consistent (within 1dB), thus the amplitude balance pots may be eliminated in less demanding applications. The SA602s have excellent gain as well as phase integrity.

Audio Phase Shift Circuits

The two critical stages for the phasing method are a dual quadrature mixer and a broadband audio phase shifter (differentiator). There are several broadband, phase shift techniques available. Figure 15 shows an analog all-pass differential phase shift circuit. When the inputs are shorted and driven with a microphone circuit, the outputs will be 90 degrees out-of-phase over the 300 to 3000Hz band. This "splitting" and phase shift is necessary for the phasing generator. For phasing demodulation the two audio detectors are fed to the two inputs. The outputs are then summed to affect the sideband rejection and audio output.

Standard 1% values are shown for the resistors and capacitors, although better gain tolerances can be obtained with 0.1% laser-trimmed integrated resistors. Polystyrene capacitors are preferred for better value tolerance and audio performance. Two quad op amps fit nicely into this application. One op amp serves as a switch buffer and the other three form a phasing section. The SA5514 quad op amps perform well for this application. Careful attention to active filter configurations can yield highly linear and very high dynamic range circuits. Yet these characteristics are much easier to achieve at audio than the common IF RF frequencies. This fact, coupled with the lack of IF tuned circuits, shielding, and higher power requirements make audio IF systems attractive indeed.

Figure 16 shows a "tapped" analog delay circuit which uses weighted values of resistors to affect the phase shift. Excellent phase and amplitude balance are possible with this technique, but the price for components is high. It should be stressed that the audio phase shift accuracy and amplitude balance are the limiting factors for SSB rejection when using the phase method; thus the higher cost may be justified in some applications.

Audio Processing

The summing amplifier is a conventional, inverting op amp circuit. It may be useful to configure a low-pass filter around this amplifier, and thus help the sharp audio filters which follow. Audio filters are necessary to shape the desired bandpass. Steep slope audio bandpass filters can be built from switched capacitor filters or from active filters

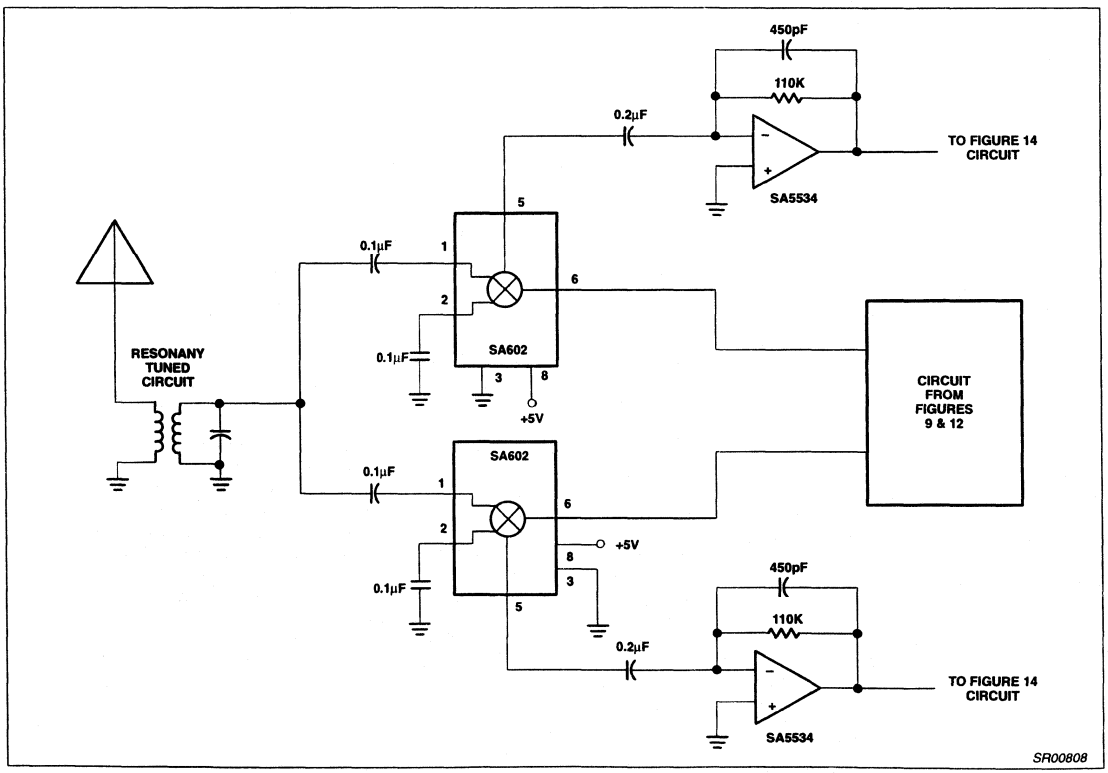


Figure 13. Phasing Method Detector for Direct Conversion Receiver

requiring more op amps. Switched capacitor filters have the disadvantage of requiring a clock frequency in the RF range. Harmonics can cause interference problems if careful design techniques are not used. Also, better dynamic range is obtained with

active filter techniques using "real" resistors although much work is being done with SCF's and performance is improving.

Direct conversion receivers rely heavily on audio filters for selectivity. Active analog or switched capacitor filters can produce the high Q and dynamic ranges necessary. Signal strength or "S-meters" can be constructed from the SA602's companion part, the SA604. The "RSSI" or "received signal strength indicator" function on the 604 provides a logarithmic response over a 90dB dynamic range and is easy to use at audio frequencies. Finally, the AGC (automatic gain control) function can also be performed in the audio section. Attack and delay times can be independently set with excellent distortion specifications with the SA572 compandor IC. The audio-derived AGC eliminates the need for gain controlling and RF stage, but relies on an excellent receiver front-end dynamic range. In ACSSB (Amplitude Compandored Single-Side Band) systems transmitter compression and receiver expansion are defined by individual system specifications.

Phasing-Filter Technique

High quality SSB radio specifications call for greater than 70dB sideband rejection. Using the circuits described in this paper for the phasing method, rejection levels of 35dB are obtainable with good reliability. Coupled with an inexpensive two-pole crystal or ceramic filter, the 70dB requirement is obtained. Also, the filtering ahead of the SA602 greatly improves the intermodulation performance of the receiver. Figure 17 shows a complete SSB receiver using the Phasing-Filter technique. The sensitivity of the SA602 allows low gain stages and low power consumption for the RF amplifier and first mixer. A new generation of low power CMOS frequency synthesizers is now available from several manufacturers including the TDD1742 and dual chip HEF4750/51 solutions.

Direct Conversion Receiver

The antenna can be connected directly to the input of the SA602 (via a bandpass filter) to form a direct conversion SSB receiver using the phasing method. 35dB sideband rejection is adequate for many applications, particularly where low power and portable battery operation are required. Figure 13 shows a typical circuit for direct conversion applications.

There are many other applications which can make use of SSB technology. Cordless telephones use FM almost exclusively. Eavesdropping could be greatly reduced for systems which employ SSB rather than FM. Furthermore, the better signal-to-noise ratio will extend the range, and battery life will be extended because no carrier is needed.

SSB is also used for subcarriers on microwave links and coaxial lines. Telephone communications networks that use SSB are called FDM or Frequency Domain Multiplex systems. The low power and high sensitivity of the SA602 can offer FDM designers new techniques for system configuration.

Weaver Method Receiver Techniques

The same quadrature dual mixer can be used for the first stage in both the phasing and Weaver method receiver. The subcarrier stage in the Weaver method receiver can use CMOS analog switches (HEF4066) for great power economy. Figure 18 shows a circuit for the subcarrier stage. A 1.8kHz subcarrier requires a 7.2kHz clock frequency. If switched capacitor filters are used for the low-pass and audio filters, a single clock generator can be used for all circuits with appropriate dividers. Furthermore, if the receiver is used as an IF circuit, the fixed LO signal could also be derived from the same clock. This has the added advantage that harmonics from the various circuits will not interfere with the received signal.

Results

The circuit shown in Figures 13, 14, and 15 has a 10dB S/N sensitivity of 0.5μV with a dynamic range of about 80dB. Single-tone audio harmonic distortion is below 0.05% with two-tone intermodulation products below 55dB at RF input levels only 5dB below the 1dB compression point. The sideband rejection is about 38dB at a 9MHz operating frequency. The good audio specifications are a side benefit to direct conversion receivers. When used with inexpensive ceramic or crystal filters, this circuit can provide these specifications with >70dB sideband rejection.

Conclusions

Single sideband offers many advantages over FM and full-carrier double-sideband modulation. These advantages include: more efficient spectrum use, better signal-to-noise ratios at low signal levels, and better transmitter efficiency. Many of the disadvantages can now be overcome by using old techniques and new state-of-the-art integrated circuits. Effective and inexpensive circuits can use direct conversion techniques with good results. 35dB sideband rejection with less than 1μV sensitivity is obtained with the SA602 circuits. 70dB sideband rejection and superior sensitivity are obtained by using phasing-filter techniques. Either the phasing or Weaver methods can be used in either the direct conversion or IF section applications. The filter and phase-filter methods can be used in only the IF application.

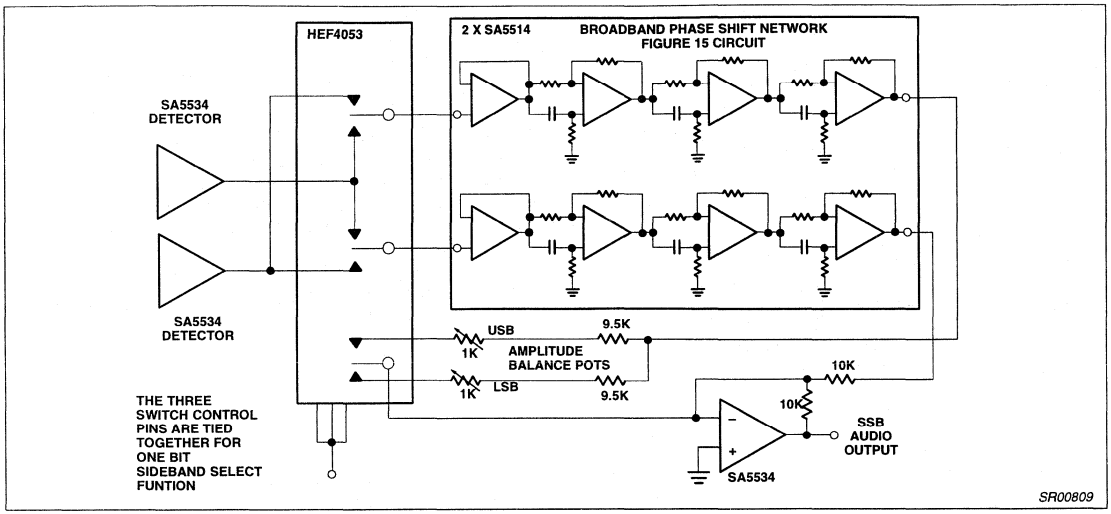


Figure 14. Sideband Select Switching Function

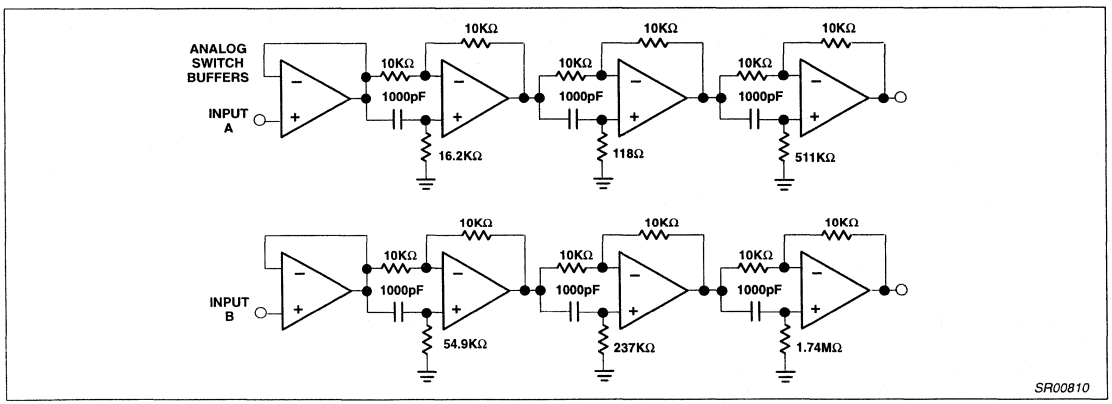


Figure 15.

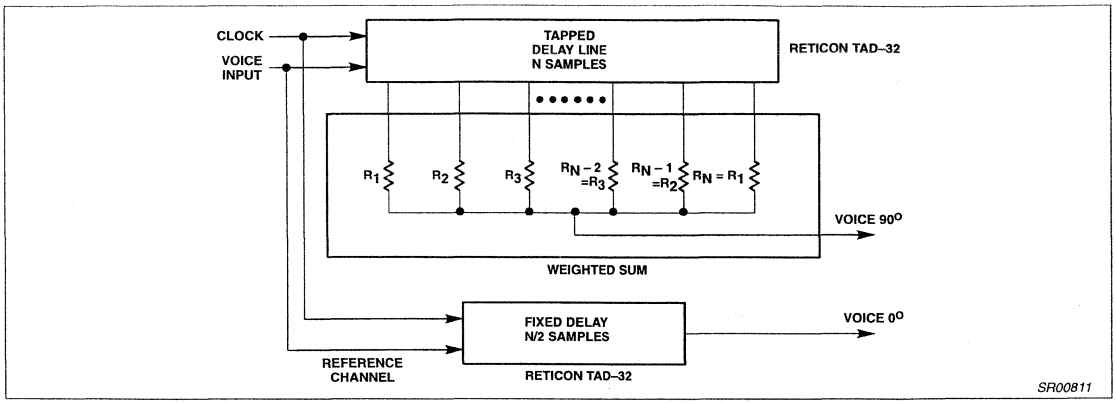


Figure 16. Broadband 90° Audio Phase Shift Technique Using Tapped Delay Line (Reference 4)

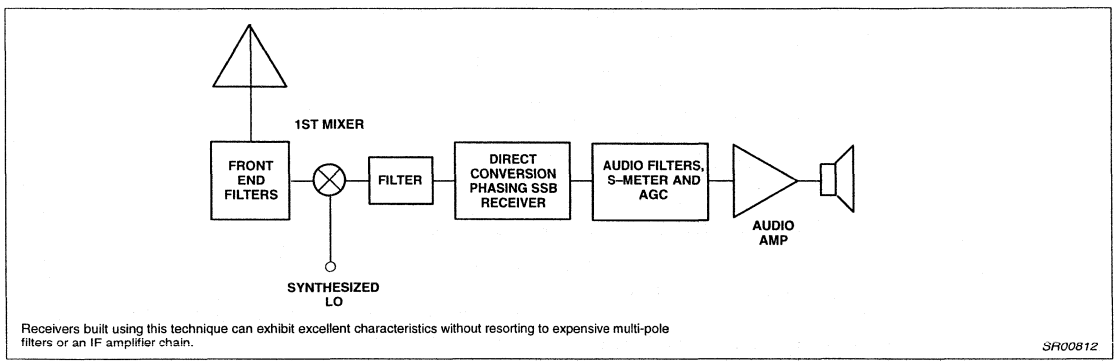


Figure 17. Complete Phasing-Filter Receiver

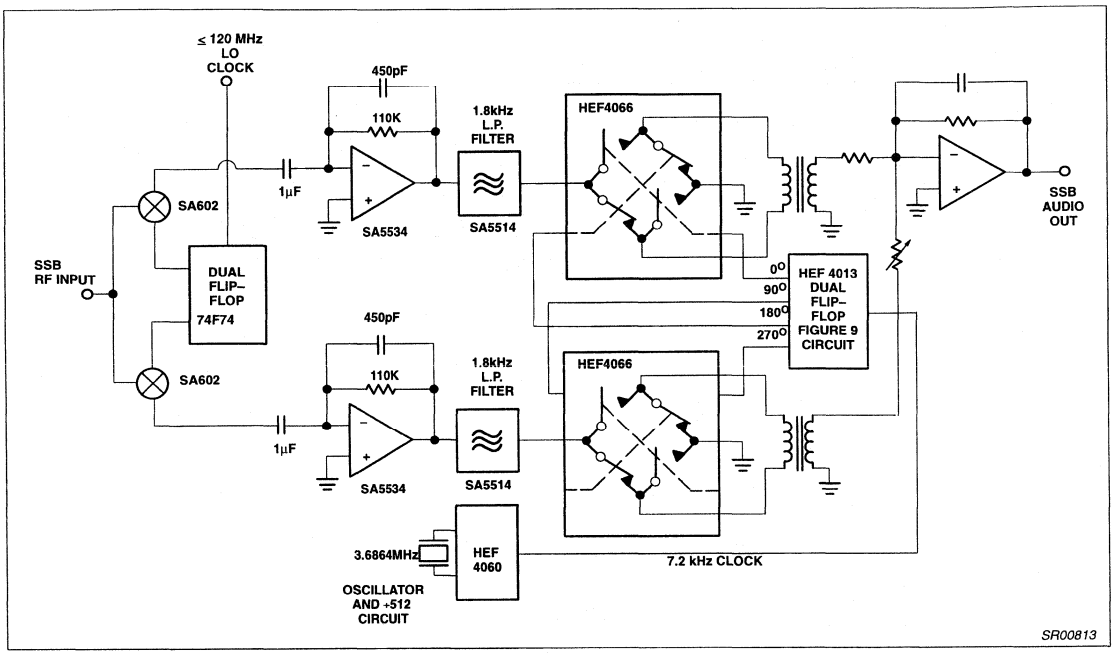


Figure 18. Weaver Method Receiver Concept Example for ≤ 30MHz Operation

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Applying the oscillator of the SA602 in low-power mixer applications

AN1982

Author: Donald Anderson

INTRODUCTION

For the designer of low power RF systems, the Philips Semiconductors SA602 mixer/oscillator provides mixer operation beyond 500MHz, a versatile oscillator capable of operation to 200MHz, and conversion gain, with only 2.5mA total current consumption. With a proper understanding of the oscillator design considerations, the SA602 can be put to work quickly in many applications.

DESCRIPTION

Figure 1 shows the equivalent circuit of the device. The chip is actually three subsystems: A Gilbert cell mixer (which provides differential input gain), a buffered emitter follower oscillator, and RF current and voltage regulation. Complete integration of the DC bias permits simple and compact application. The simplicity of the oscillator permits many configurations.

While the oscillator is simple, oscillator design isn't. This article will not address the rigors of oscillator design, but some practical guidelines will permit the designer to accomplish good performance with minimum difficulty.

Either crystal or LC tank circuitry can be employed effectively. Figure 2 shows the four most commonly used configurations in their most basic form.

In each case the Q of the tank will affect the upper frequency limits of oscillation: the higher the Q the higher the frequency. The SA602 is fabricated with a 6GHz process, but the emitter resistor from Pin 7 to ground is nominally 20k. With 0.25mA typical bias current, 200MHz oscillation can be achieved with high Q and appropriate feedback.

The feedback, of course, depends on the Q of the tank. It is generally accepted that a minimum amount of feedback should be used, so even if the choice is entirely empirical, a good trade-off between starting characteristics, distortion, and frequency stability can be quickly determined.

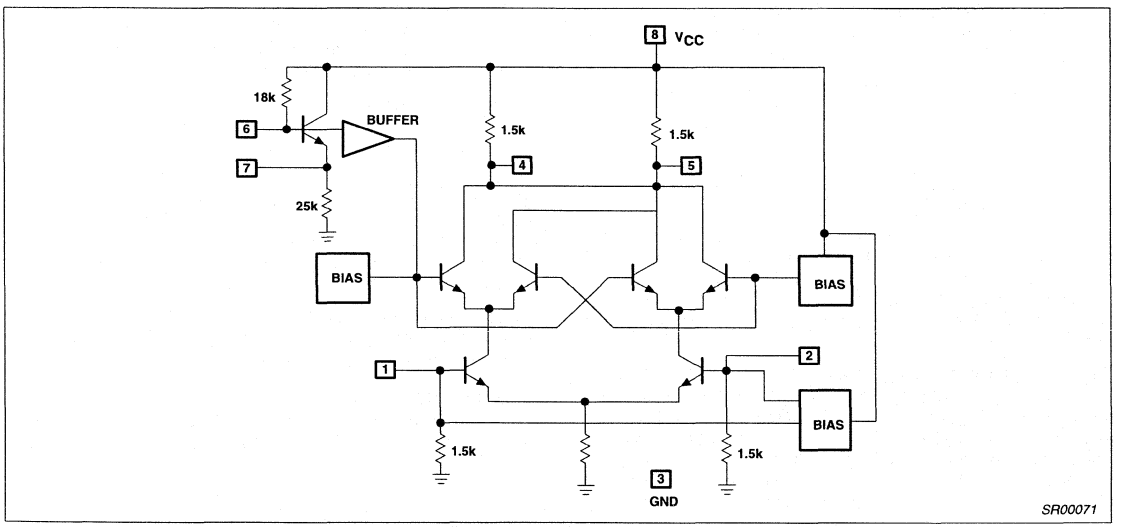


Figure 1. Equivalent Circuit

Applying the oscillator of the SA602 in low-power mixer applications

AN1982

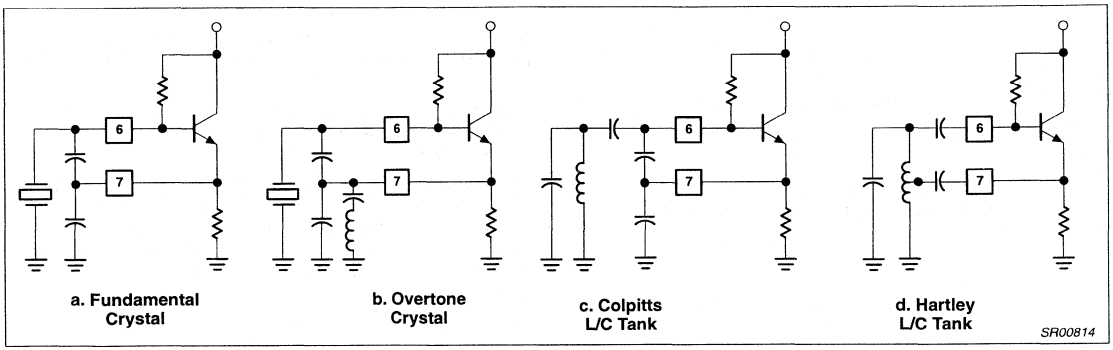


Figure 2.

Crystal Circuit Considerations

Crystal oscillators are relatively easy to implement since crystals exhibit higher Q's than LC tanks. Figure 3 shows a complete implementation of the SA602 (extended temperature version) for cellular radio with a 45MHz first IF and 455kHz second IF.

The crystal is a third overtone parallel mode with 5pF of shunt capacitance and a trap to suppress the fundamental.

LC Tank Circuits

LC tanks present a little greater challenge for the designer. If the Q is too low, the oscillator won't start. A trick which will help if all else fails is to shunt Pin 7 to ground with a 22k resistor. In actual applications this has been effective to 200MHz with high Q ceramic capacitors and a tank inductor of 0.08mH and a Q of 90. Smaller resistor value will upset DC bias because of inadequate base bias at the input of the oscillator. An external bias resistor could be added from VCC to Pin 6, but this will introduce power supply noise to the frequency spectrum.

The Hartley configuration (Figure 2D) offers simplicity. With a variable capacitor tuning the tank, the Hartley will tune a very large range since all of the capacitance is variable. Please note that the inductor must be coupled to Pin 7 with a low impedance capacitor. The Colpitts oscillator will exhibit a smaller tuning range since the fixed feedback capacitors limit variable capacitance range; however, the Colpitts has good frequency stability with proper components.

Synthesized Frequency Control

The SA602 can be very effective with a synthesizer if proper precautions are taken to minimize loading of the tank and the introduction of digital switching transients into the spectrum. Figure 4 shows a circuit suitable for aircraft navigation frequencies (108–118MHz) with 10.7MHz IF.

The dual gate MOSFET provides a high degree of isolation from prescaler switching spikes. As shown in Figure 4, the total current consumption of the SA602 and 3SK126 is typically 3mA. The MOSFET input is from the emitter of the oscillator transistor to avoid loading the tank. The Gate 1 capacitance of the MOSFET in series with the 2pF coupling capacitor adds slightly to the feedback capacitance ratio. Use of the 22k resistor at Pin 7 helps assure oscillation without upsetting DC bias.

For applications where optimum buffering of the tank, or minimum current are not mandatory, or where circuit complexity must be minimized, the buffers shown in Figure 5 can be considered.

The effectiveness of the MRF931 (or other VHF bipolar transistors) will depend on frequency and required input level to the prescaler. A bipolar transistor will generally provide the least isolation. At low frequencies the transistor can be used as an emitter follower, but by VHF the base emitter junction will start to become a bidirectional capacitor and the buffer is lost.

The 2N5484 has an IDSS of 5mA max. and the 2SK126 has IDSS of 6mA max. making them suitable for low parts count, modest current buffers. The isolation is good.

Injected LO

If the application calls for a separate local oscillator, it is acceptable to capacitively-couple 200 to 300mV at Pin 6.

Summary

The SA602 can be an effective low power mixer at frequencies to 500MHz with oscillator operation to 200MHz. All DC bias is provided internal to the device so very compact designs are possible. The internal bias sets the oscillator DC current at a relatively low level so the designer must choose frequency selective components which will not load the transistor. If the guidelines mentioned are followed, excellent results will be achieved.

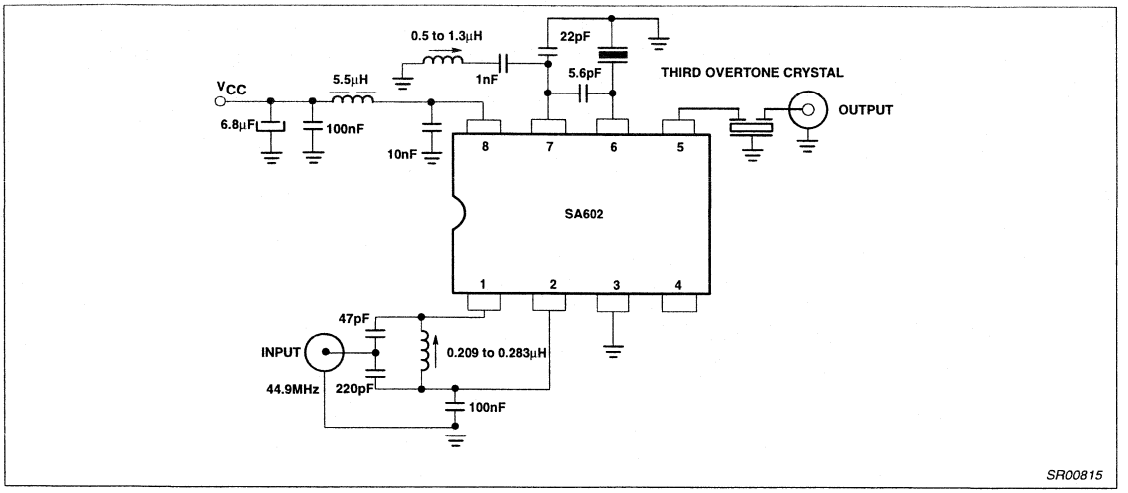


Figure 3. Cellular Radio Application

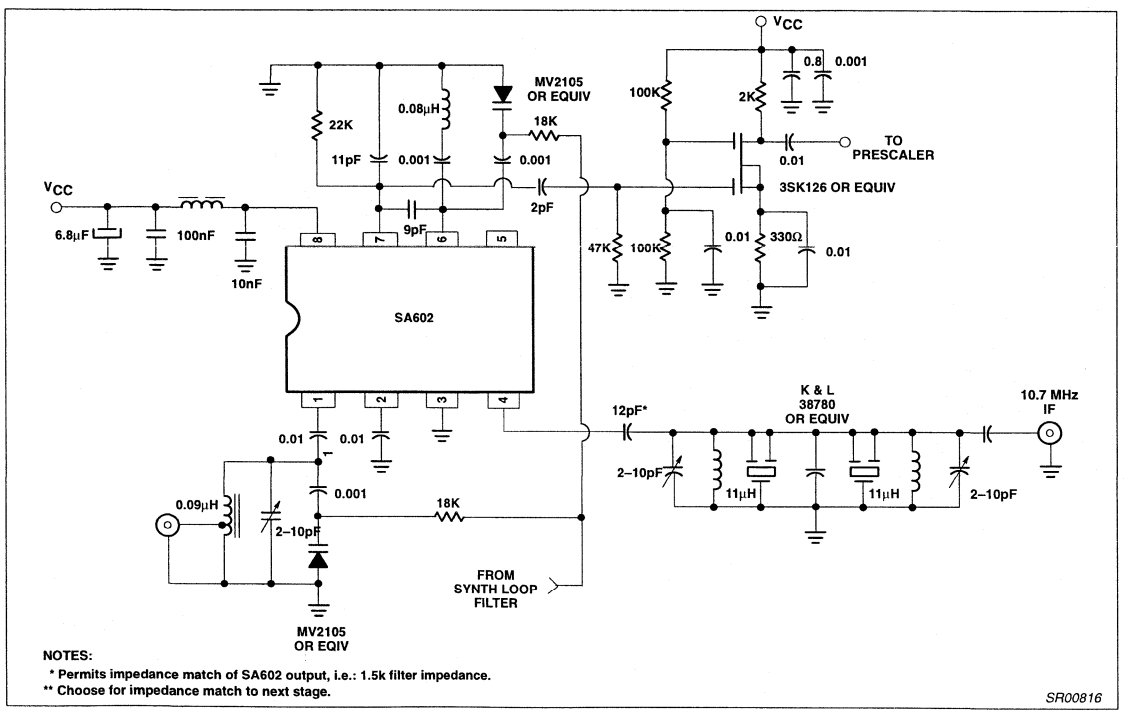
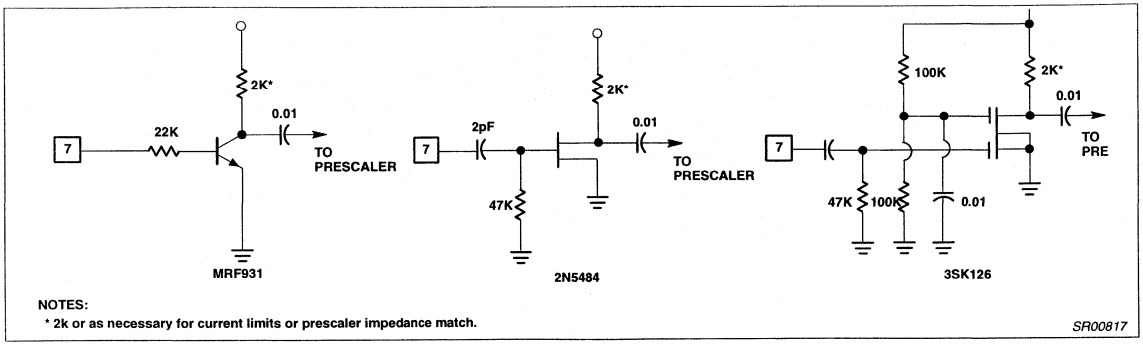


Figure 4.


2K*
0.01
22K
7
TO
PRESCALER
MRF931
2K*
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2N5484
100K
2K*
0.01
7
47K
100K
0.01
TO
PRE
3SK126
NOTES:
* 2k or as necessary for current limits or prescaler impedance match.
SR00817

Figure 5.

Audio decibel level detector with meter driver AN1991

Author: Robert J. Zavrel Jr.

DESCRIPTION

Although the SA604 was designed as an RF device intended for the cellular radio market, it has features which permit other design configurations. One of these features is the Received Signal Strength Indicator (RSSI). In a cellular radio, this function is necessary for continuous monitoring of the received signal strength by the radio's microcomputer. This circuit provides a logarithmic response proportional to the input signal level. The SA604 can provide this logarithmic response over an 80dB range up to a 15MHz operating frequency. This paper describes a technique which optimizes this useful function within the audio band.

A sensitive audio level indicator circuit can be constructed using two integrated circuits: the SA604 and SA532. This circuit draws very little power (less than 5mA with a single 6V power supply) making it ideal for portable battery operated equipment. The small size and low-power consumption belie the 80dB dynamic range and 10.5μV sensitivity.

The RSSI function requires a DC output voltage which is proportional to the $\log_{10}$ of the input signal level. Thus a standard 0-5 voltmeter can be linearly calibrated in decibels over a single 80dB range. The entire circuit is composed of 9 capacitors and two resistors along with the two ICs. No tuning or calibration is required in a manufacturing setting.

The Audio Input vs Output Graph shows that the circuit is within 1.5dB tolerance over the 80dB range for audio frequencies from 100Hz to 10kHz. Higher audio levels can be measured by placing an attenuator ahead of the input capacitor. The input impedance is high (about 50k), so lower impedance terminations (50 or 600Ω) will not be affected by the input impedance. If very accurate tracking is required (<0.5dB accuracy), a 40 or 50dB segment can be "selected". A range switch can then be added with appropriate attenuators if more than 40 or 50dB dynamic range is required.

There are two amplifier sections in the 604 with 2 and 3 stages in the first and second sections respectively. Each stage outputs a sample current to a summing circuit. The summing circuit has a current mirror which appears at Pin 5. This current is proportional to the $\log_{10}$ of the input audio signal. A voltage is dropped across the 100k resistor by the current, and a 0.1μF capacitor is used to bypass and filter the output signal. The 532 op amp is used as a buffer and meter driver, although a digital voltmeter could replace both the op amp and the meter shown. The rest of the capacitors are used for power supply and amplifier input bypassing.

The RC circuit between Pins 14 and 12 forms a low-pass filter which can be adjusted by changing the value of C1. Raising the capacitance will lower the cut-off frequency and also lower the zero signal output resting voltage (about 0.6V). Lowering the capacitance value will have the opposite effect with some reduction in dynamic range, but will raise the frequency response. The 2kΩ resistor value provides the near-ideal inter-stage loss for maximum RSSI linearity. C2 can also be changed. The trade-off here is between output damping and ripple. Most analog and digital metering methods will tend to cancel the effects of small or moderate ripple voltages through integration, but high ripple voltages should be avoided.

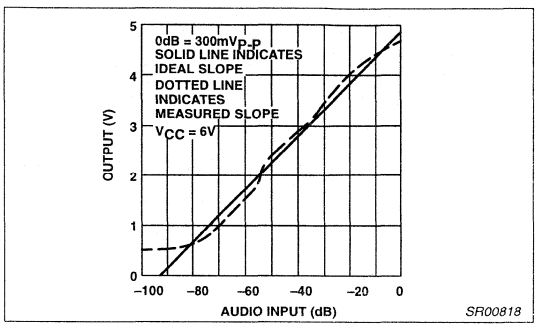

Figure 1.

A second op amp is used with an optional second filter. This filter has the advantage of a low impedance signal source by virtue of the first op amp. Again, a trade-off exists between meter damping and ripple attenuation. If very low ripple and low damping are both required, a more complex active low-pass filter should be constructed.

Some applications of this circuit might include:

1. Portable acoustic analyzer
2. Microphone tester
3. Audio spectrum analyzer
4. VU meters
5. S-meter for direct conversion radio receiver
6. Audio dynamic range testers
7. Audio analyzers (THD, noise, separation, response, etc.)

Audio decibel level detector with meter driver AN1991

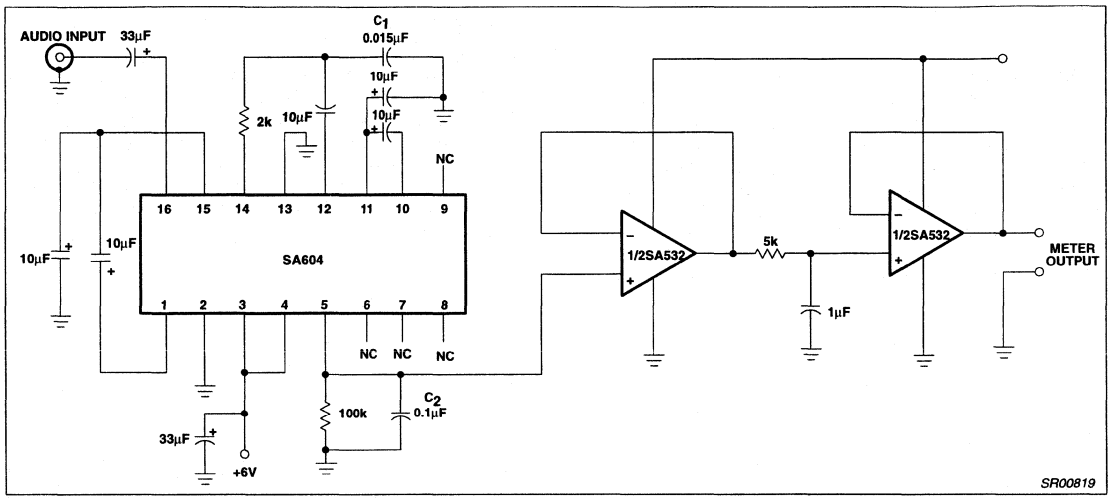

Figure 2.

High sensitivity applications of low-power RF/IF integrated circuits

AN1993

ABSTRACT

This paper discusses four high sensitivity receivers and IF (Intermediate Frequency) strips which utilize intermediate frequencies of 10.7MHz or greater. Each circuit utilizes a low-power VHF mixer and high-performance low-power IF strip. The circuit configurations are

1. 45 or 49MHz to 10.7MHz narrowband,
2. 90MHz to 21.4MHz narrowband,
3. 100MHz to 10.7MHz wideband, and
4. 152.2MHz to 10.7MHz narrowband.

Each circuit is presented with an explanation of component selection criteria, (to permit adaptation to other frequencies and bandwidths). Optional configurations for local oscillators and data demodulators are summarized.

INTRODUCTION

Traditionally, the use of 10.7MHz as an intermediate frequency has been an attractive means to accomplish reasonable image rejection in VHF/UHF receivers. However, applying significant gain at a high IF has required extensive gain stage isolation to avoid instability and very high current consumption to get adequate amplifier gain bandwidth. By enlightened application of two relatively new low power ICs, Philips Semiconductors SA602 and SA604A, it is possible to build highly producible IF strips and receivers with input frequencies to several hundred megahertz, IF frequencies of 10.7 or 21.4MHz, and sensitivity less than 2μV (in many cases less than 1μV). The Philips Semiconductors new SA605 combines the function of the SA602 and the SA604A. All of the circuits described in this paper can also be implemented with the SA605. The SA602 andSA604A were utilized for this paper to permit optimum gain stage isolation and filter location.

THE BASICS

First let's look at why it is relevant to use a 10.7 or 21.4MHz intermediate frequency. 455kHz ceramic filters offer good selectivity and small size at a low price. Why use a higher IF? The fundamental premise for the answer to this question is that the receiver architecture is a hetrodyne type as shown in Figure 1.

A pre-selector (bandpass in this case) precedes a mixer and local oscillator. An IF filter follows the mixer. The IF filter is only supposed to pass the difference (or sum) of the local oscillator (LO) frequency and the preselector frequency.

The reality is that there are always two frequencies which can combine with the LO: The pre-selector frequency and the "image" frequency. Figure 2 shows two hypothetical pre-selection curves. Both have 3dB bandwidths of 2MHz. This type of pre-selection is typical of consumer products such as cordless telephone and FM radio. Figure 2A shows the attenuation of a low side image with 10.7MHz. Figure 2B shows the very limited attenuation of the low side 455kHz image.

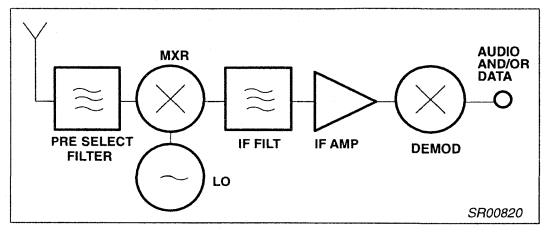

Figure 1. Basic Hetrodyne Receiver

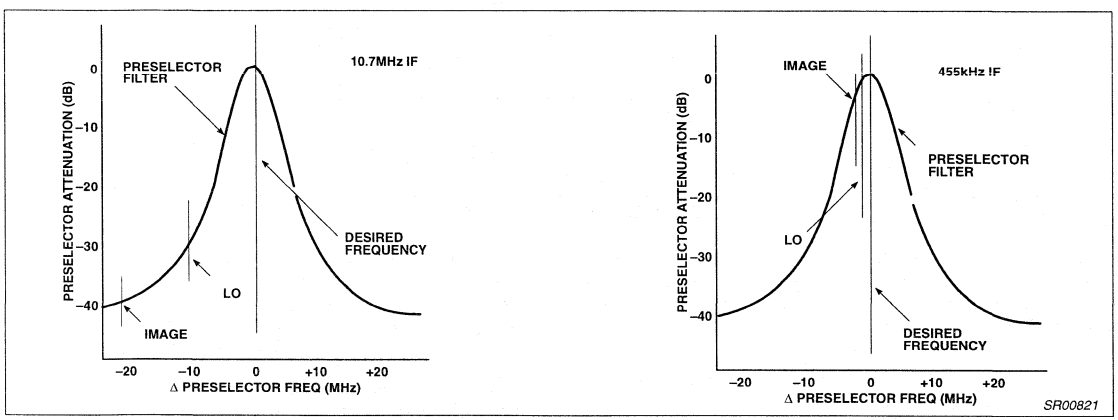

Figure 2. Effects of Preselection on Images

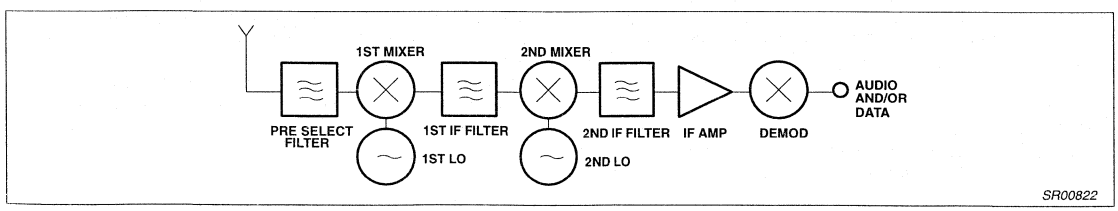

Figure 3. Dual Conversion

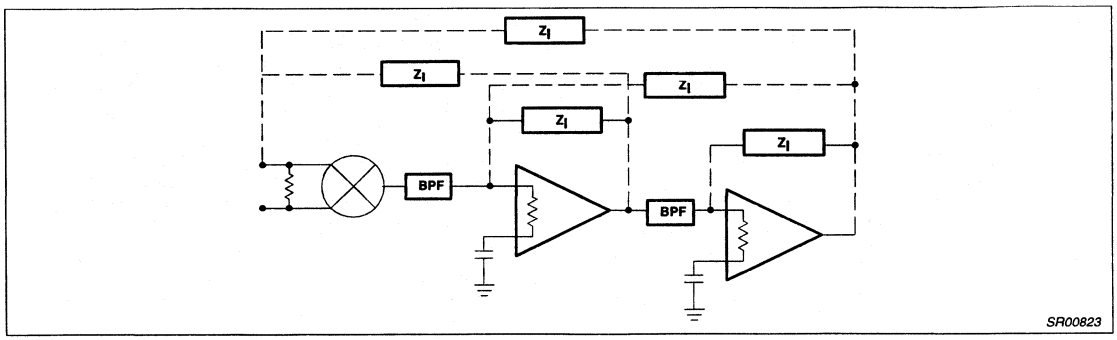

Figure 4. Feedback Paths

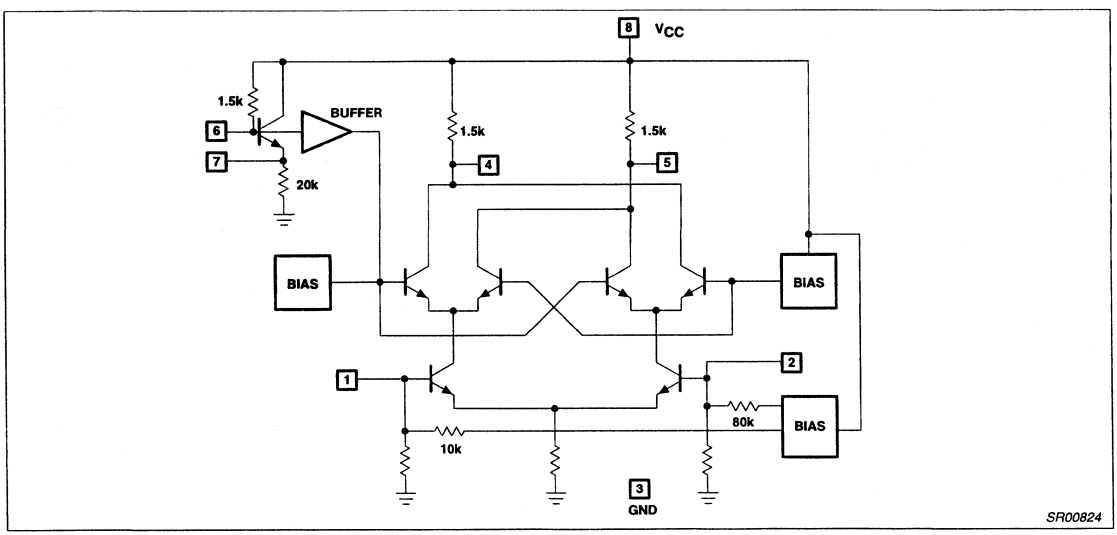

Figure 5. SA602 Equivalent Circuit

If the single conversion architecture of Figure 1 were implemented with a 455kHz IF, any interfering image would be received almost as well as the desired frequency. For this reason, dual conversion, as shown in Figure 3, has been popular.

In the application of Figure 3, the first IF must be high enough to permit the pre-selector to reject the images of the first mixer and must have a narrow enough bandwidth that the second mixer images and the intermod products due to the first mixer can be attenuated. There's more to it than that, but those are the basics. The multiple conversion hetrodyne works well, but, as Figure 3 suggests, compared to Figure 2 it is more complicated. Why, then, don't we use the approach of Figure 2?

THE PROBLEM

Historically there has been a problem: Stability! Commercially available integrated IF amplifiers have been limited to about 60dB of gain. Higher discrete gain was possible if each stage was carefully shielded and bypassed, but this can become a nightmare on a production line. With so little IF gain available, in order to receive signals of less than 10μV it was necessary to add RF gain and this, in turn, meant that the mixer must have good large signal handling capability. The RF gain added expense, the high level mixer added expense, both added to the potential for instabilities, so the multiple conversion started looking good again.

But why is instability such a problem in a high gain high IF strip? There are three basic mechanisms. First, ground and the supply line are potentially feedback mechanisms from stage-to-stage in any amplifier. Second, output pins and external components create fields which radiate back to inputs. Third, layout capacitances become feedback mechanisms. Figure 4 shows the fields and capacitances symbolically.

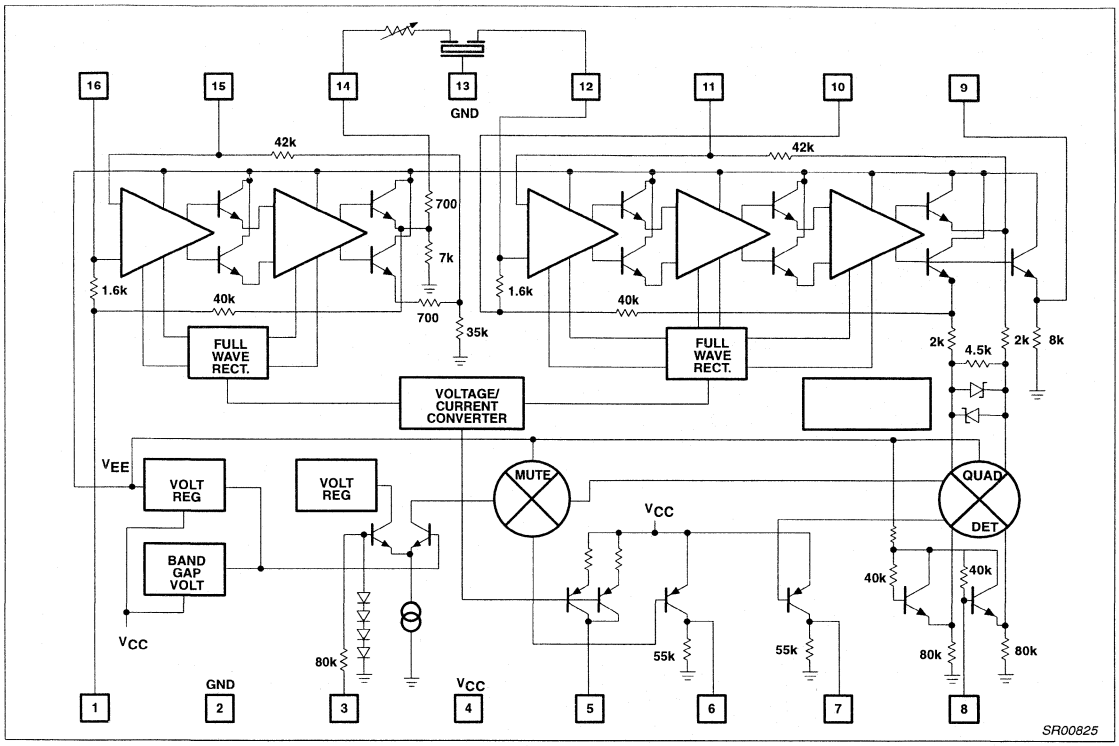

Figure 6. SA604A Equivalent Circuit

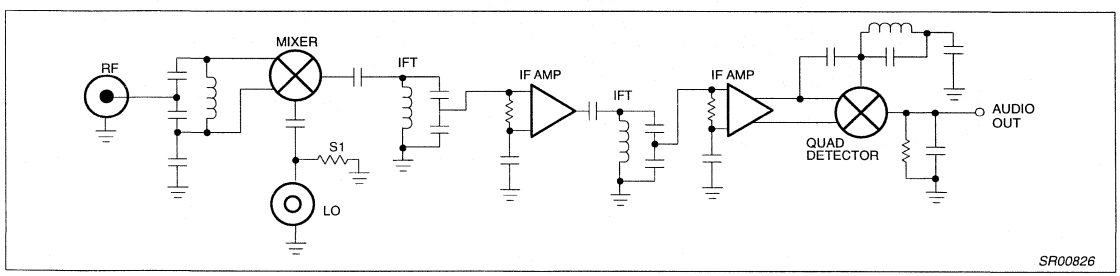

Figure 7. Symbolic Circuit

If Z_F represents the impedance associated with the circuit feedback mechanisms (stray capacitances, inductances and radiated fields), and Z_{IN} is the equivalent input impedance, a divider is created. This divider must have an attenuation factor greater than the gain of the amplifier if the amplifier is to remain stable.

- If gain is increased, the input-to-output isolation factor must be increased.
- As the frequency of the signal or amplifier bandwidth increases, the impedance of the layout capacitance decreases thereby reducing the attenuation factor.

The layout capacitance is only part of the issue. In order for traditional 10.7MHz IF amplifiers to operate with reasonable gain bandwidth, the amount of current in the amplifiers needed to be quite high. The CA3089 operates with 25mA of typical quiescent current. Any currents which are not perfectly differential must be carefully bypassed to ground. The higher the current, the more difficult the challenge. And limiter outputs and quadrature components make excellent field generators which add to the feedback scenario. The higher the current, the larger the field.

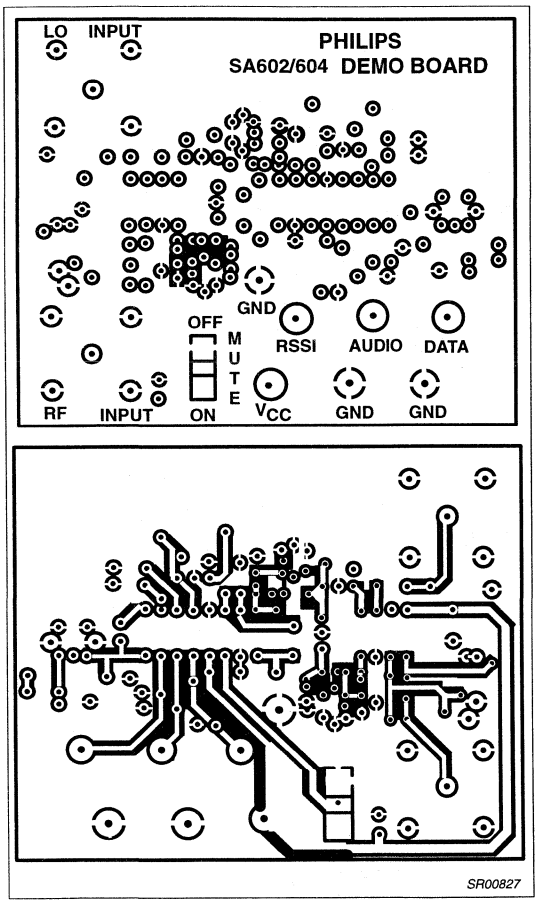

Figure 8. Circuit Board Layout

THE SOLUTION

The SA602 is a double balanced mixer suitable for input frequencies in excess of 500MHz. It draws 2.5mA of current. The SA604A is an IF strip with over 100dB of gain and a 25MHz small signal bandwidth. It draws 3.5mA of current. The circuits in this paper will demonstrate ways to take advantage of this low current and 75dB or more of the SA604A gain in receivers and IF strips that would not be possible with traditional integrated circuits. No special tricks are used, only good layout, impedance planning and gain distribution.

THE MIXER

The SA602 is a low power VHF mixer with built-in oscillator. The equivalent circuit is shown in Figure 5. The basic attributes of this mixer include conversion gain to frequencies greater than 500MHz, a noise figure of 4.6dB @ 45MHz, and a built-in oscillator which can be used up to 200MHz. LO can be injected.

For best performance with any mixer, the interface must be correct. The input impedance of the SA602 is high, typically 3kΩ in parallel with 3pF. This is not an easy match from 50Ω. In each of the examples which follow, an equivalent 50:1.5k match

was used. This compromise of noise, loss, and match yielded good results. It can be improved upon. Match to crystal filters will require special attention, but will not be given focus in this paper.

This oscillator is a single transistor with an internal emitter follower driving the mixer. For best mixer performance, the LO level needs to be approximately 220mV$_{RMS}$ at the base of the oscillator transistor (Pin 6). A number of oscillator configurations are presented at the end of this paper. In each of the prototypes for this paper, the LO source was a signal generator. Thus, a 51Ω resistor was used to terminate the signal generator. The LO is then coupled to the mixer through a DC blocking capacitor. The signal generator is set for 0dBm. The impedance at the LO input (Pin 6) is approximately 20kΩ. Thus, required power is very low, but 0dBm across 51Ω does provide the necessary 220mV$_{RMS}$.

The outputs of the SA602 are loaded with 1.5kΩ internal resistors. This makes interface to 455kHz ceramic filters very easy. Other filter types will be addressed in the examples.

THE IF STRIP

The basic functions of the SA604A are ordinary at first glance: Limiting IF, quadrature detector, signal strength meter, and mute switch. **However, the performance of each of these blocks is superb.** The IF has 100dB of gain and 25MHz bandwidth. This feature will be exploited in the examples. The signal strength indicator has a 90dB log output characteristic with very good linearity. There are two audio outputs with greater than 300kHz bandwidth (one can be muted greater than 70dB). The total supply current is typically 3.5mA. This is the other factor which permits high gain and high IF.

Figure 6 shows an equivalent circuit of the SA604A. Each of the IF amplifiers has a 1.6kΩ input impedance. The input impedance is achieved by splitting a DC feedback bias resistor. The input impedance will be manipulated in each of the examples to aid stability.

BASIC CONSIDERATIONS

In each of the circuits presented, a common layout and system methodology is used. The basic circuit is shown symbolically in Figure 7.

At the input, a frequency selective transformation from 50Ω to 1.5kΩ permits analysis of the circuit with an RF signal generator. A second generator provides LO. This generator second generator provides LO. This generator is terminated with a 51Ω resistor. The output of the mixer and the input of the first limiter are both high impedance (1.5Ω nominal). As indicated previously, the input impedance of the limiter must be low enough to attenuate feedback signals. So, the input impedance of the first limiter is modified with an external resistor. In most of the examples, a 430Ω external resistor was used to create a 330Ω input impedance (430//1.5kΩ). The first IF filter is thus designed to present 1.5kΩ to the mixer and 330Ω to the first limiter.

The same basic treatment was used between the first and second limiters. However, in each of the 10.7MHz examples, this interstage filter is not an L/C tank; it is a ceramic filter. This will be explained in the first example.

After the second limiter, a conventional quadrature detector demodulates the FM or FSK information from the carrier and a simple low pass filter completes the demodulation process at the audio outputs.

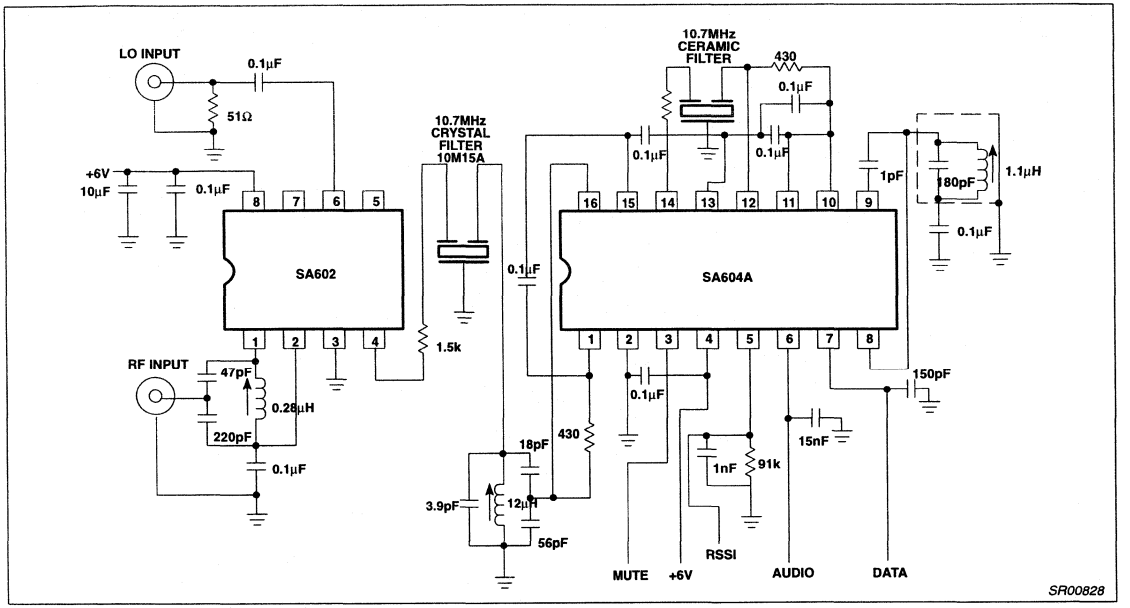

Figure 9. SA602/604A Demonstration Circuit with RF Input of 45MHz and IF of 10.7MHz ±7.5kHz

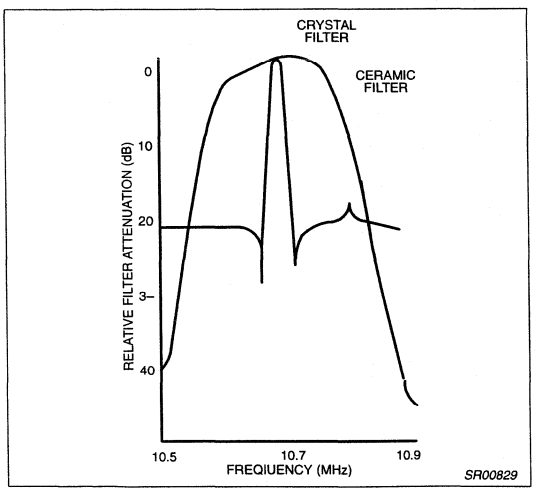

Figure 10. Passband Relationship

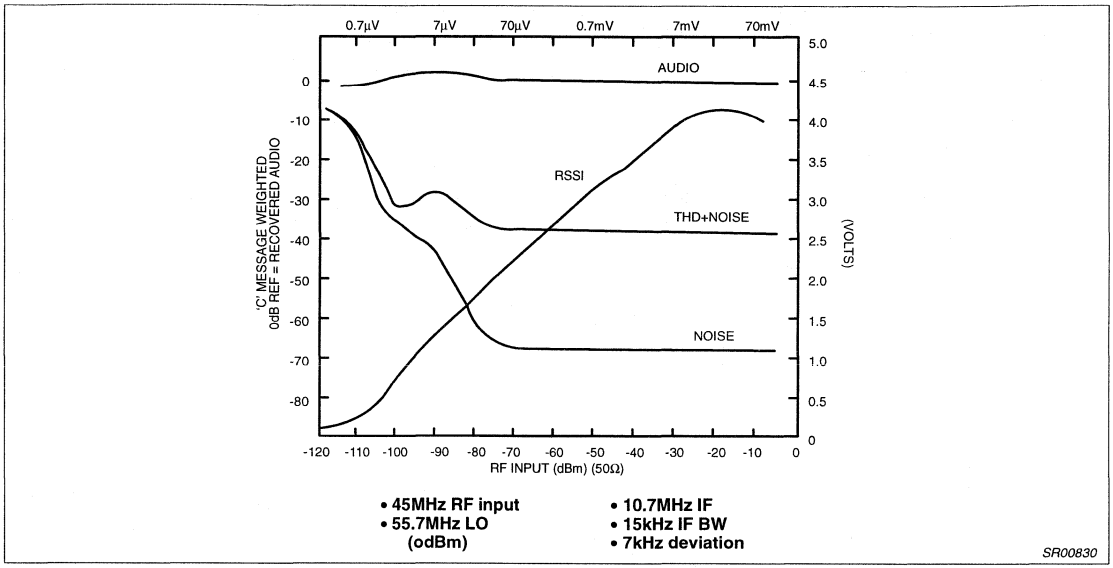

Figure 11. VHF or UHF 2nd Conversion (Narrow Band)

As mentioned, a single layout was used for each of the examples. The board artwork is shown in Figure 8. Special attention was given to: (1) Creating a maximum amount of ground plane with connection of the component side and solder side ground at locations all over the board; (2) careful attention was given to keeping a ground ring around each of the gain stages. The objective was to provide a shunt path to ground for any stray signal which might feed back to an input; (3) leads were kept short and relatively wide to minimize the potential for them to radiate or pick up stray signals; finally (and very important), (4) RF bypass was done as close as possible to supply pins and inputs, with a good (10µF) tantalum capacitor completing the system bypass.

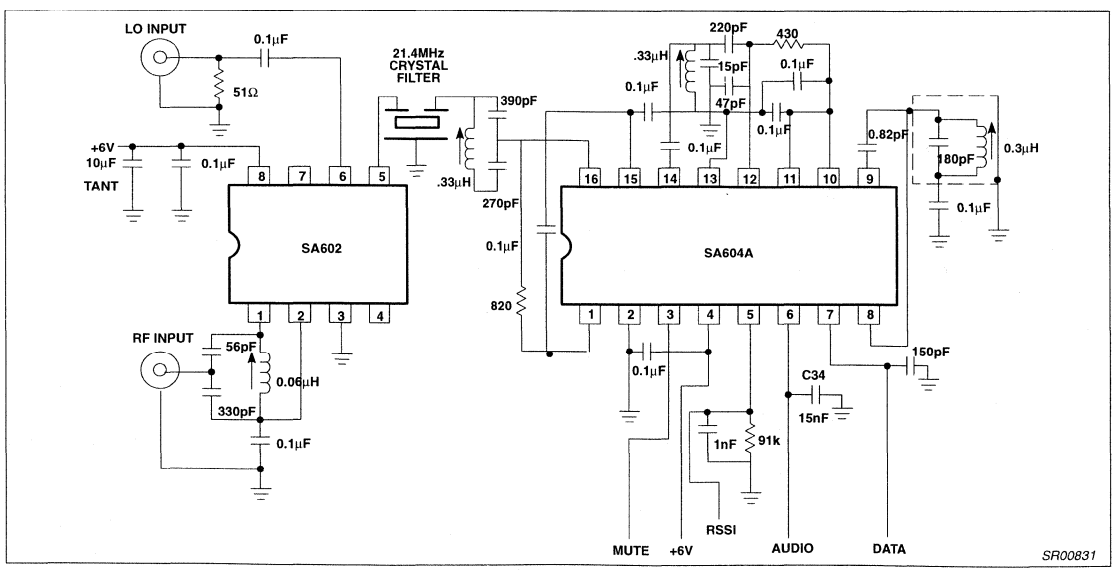

Figure 12. SA602/604A Demonstration Circuit with RF Input of 90MHz and IF of 21.4MHz ±7.5kHz

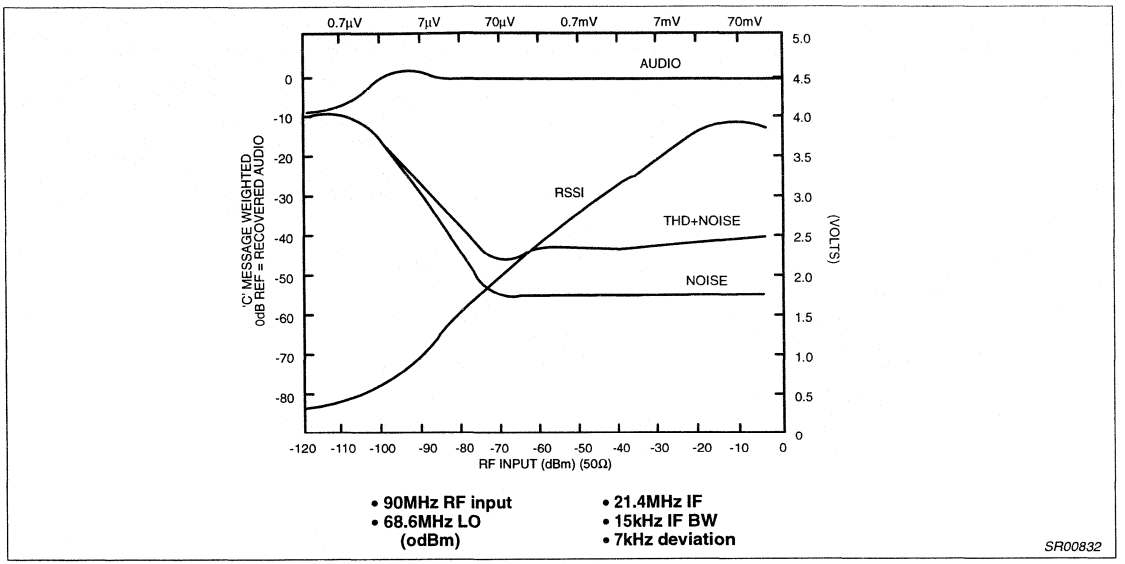

Figure 13. UHF Second Conversion (Narrow Band) or VHF Single Conversion (Narrow Band)

EXAMPLE: 45MHZ TO 10.7MHZ NARROWBAND

As a first example, consider conversion from 45MHz to 10.7MHz. There are commercially available filters for both frequencies so this is a realistic combination for a second IF in a UHF receiver. This circuit can also be applied to cordless telephone or short range communications at 46 or 49MHz. The circuit is shown in Figure 9.

The 10.7MHz filter chosen is a type commonly available for 25kHz channel spacing. It has a 3dB bandwidth of 15kHz and a termination requirement of 3kΩ/2pF. To present 3kΩ to the input side of the filter, a 1.5kΩ resistor was used between the SA602 output (which has a 1.5kΩ impedance) and the filter. Layout capacitance was close enough to 2pF that no adjustment was necessary. This series-resistance approach introduces an insertion loss which degrades the sensitivity, but it has the benefit of simplicity.

The secondary side of the crystal filter is terminated with a 10.7MHz tuned tank. The capacitor of the tank is tapped to create a transformer with the ratio for 3k:330. With the addition of the 430Ω resistor in parallel with the SA604A 1.6kΩ internal input resistor, the correct component of resistive termination is presented to the crystal filter. The inductor of the tuned load is adjusted off resonance enough to provide the 2pF capacitance needed. (Actual means of adjustment was for best audio during alignment).

If appropriate or necessary for sensitivity, the same type of tuned termination used for the secondary side of the crystal filter can also be used between the SA602 and the filter. If this is desired, the capacitors should be ratioed for 1.5k:3k. Alignment is more complex with tuned termination on both sides of the filter. This approach is demonstrated in the fourth example.

A ceramic filter is used between the first and second limiters. It is directly connected between the output of the first limiter and the input of the second limiter. Ceramic filters act much like ceramic capacitors, so direct connection between two circuit nodes with different DC levels is acceptable. At the input to the second limiter, the impedance is again reduced by the addition of a 430Ω external resistor in parallel with the internal 1.6kΩ input load resistor. This presents the 330Ω termination to the ceramic filter which the manufacturers recommend.

On the input side of the ceramic filter, no attempt was made to create a match. The output impedance of the first limiter is nominally 1kΩ. Crystal filters are tremendously sensitive to correct match. Ceramic filters are relatively forgiving. A review of the manufacturers' data shows that the attenuation factor in the passband is affected with improper match, but the degree of change is small and the passband stays centered. Since the principal selectivity for this application is from the crystal filter at the input of the first limiter, the interstage ceramic filter only has to suppress wideband noise. The first filter's passband is right in the center of the ceramic filter passband. (The crystal filter passband is less than 10% of the ceramic filter passband). This passband relationship is illustrated in Figure 10.

After the second limiter, demodulation is accomplished in the quadrature detector. Quadrature criteria is not the topic of this paper, but it is noteworthy that the choice of loaded Q will affect performance. The SA604A is specified at 455kHz using a quadrature capacitor of 10pF and a tuning capacitor of 180pF. (180pF gives a loaded Q of 20 at 455kHz). A careful look at the quadrature equations (Ref 3.) suggests that at 10.7MHz a value of about 1pF should be substituted for the 10pF at 455kHz.

The performance of this circuit is presented in Figure 11. The –12dB SINAD (ratio of Signal to Noise And Distortion) was achieved with a 0.6μV input.

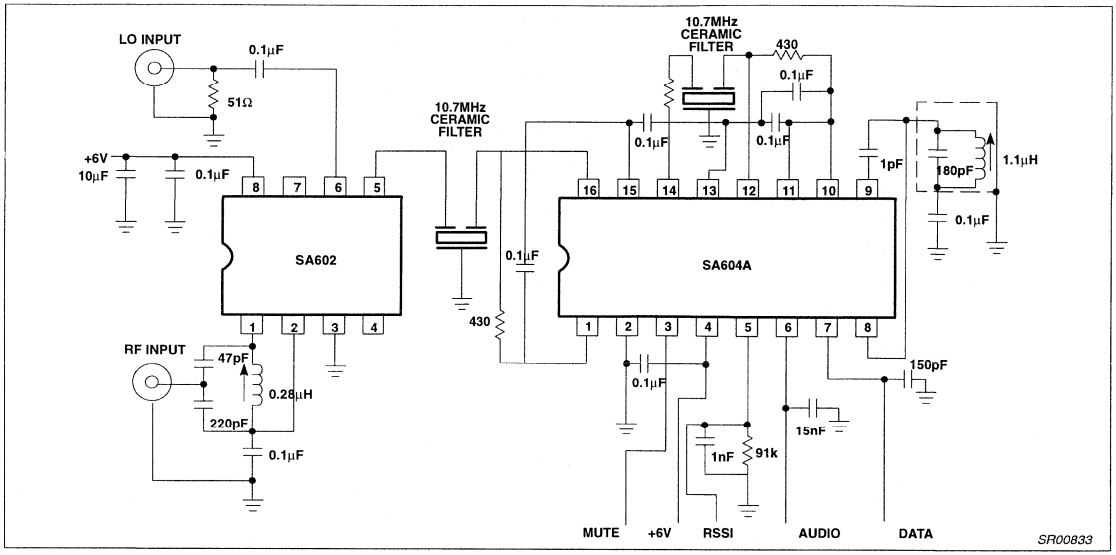

Figure 14. SA602/604A Demonstration Circuit with RF Input of ~100MHz and IF of 10.7MHz ±140kHz

EXAMPLE: 90MHZ TO 21.4MHZ NARROWBAND

This second example, like the first, used two frequencies which could represent the intermediate frequencies of a UHF receiver. This circuit can also be applied to VHF single conversion receivers if the sensitivity is appropriate. The circuit is shown in Figure 12.

Most of the fundamentals are the same as explained in the first example. The 21.4MHz crystal filter has a 1.5kΩ/2pF termination requirement so direct connection to the output of the SA602 is possible. With strays there is probably more than 2pF in this circuit, but the performance is good nonetheless. The output of the crystal filter is terminated with a tuned impedance-step-down transformer as in the previous example. Interstage filtering is accomplished with a 1kΩ:330 step-down ratio. (Remember, the output of the first limiter is 1kΩ and a 430Ω resistor has been added to make the second limiter input 330Ω). A DC blocking capacitor is needed from the output of the first limiter. The board was not laid out for an interstage transformer, so an "XACTO" knife was used to make some minor mods. Figure 13 shows the performance. The +12dB SINAD was with 1.6µV input.

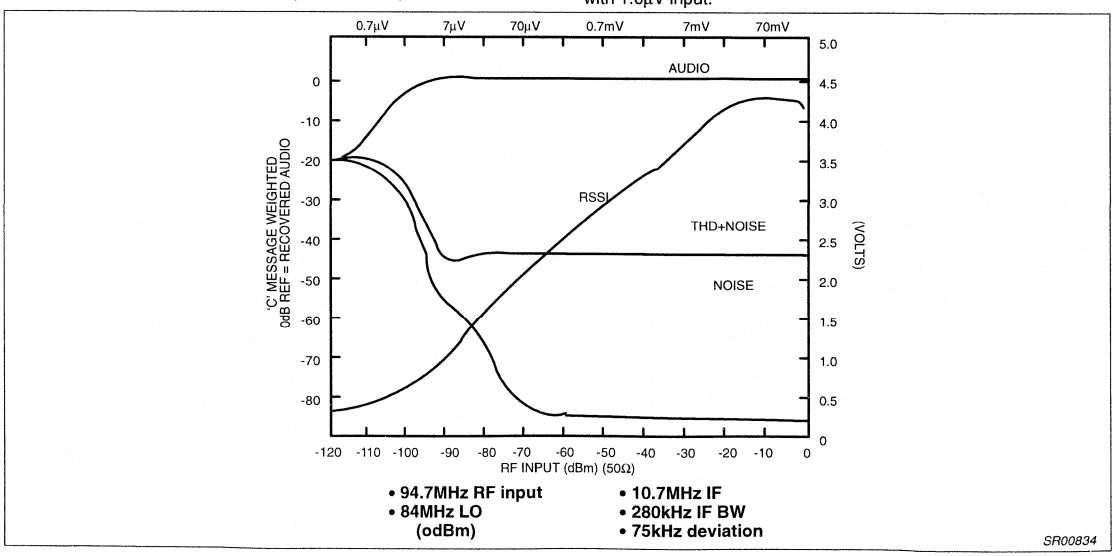

Figure 15. FM Broadcast Receiver (Wide Band)

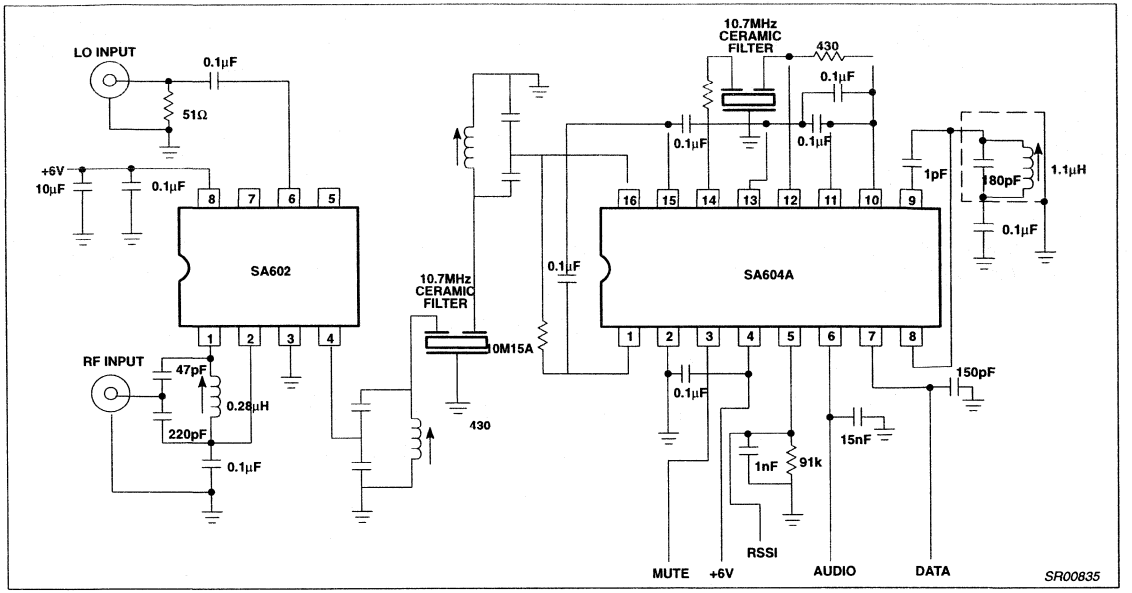

Figure 16. SA602/604A Demonstration Circuit with RF Input of 152.2MHz and IF of 10.7MHz ±7.5kHz

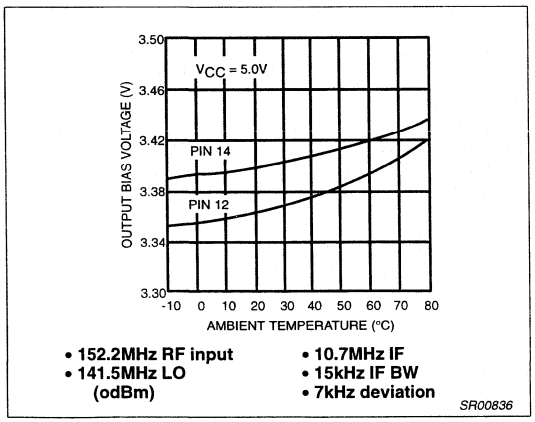

Figure 17. VHF Single Conversion (Narrow Band)

EXAMPLE: 100MHZ TO 10.7MHZ WIDEBAND

This example represents three possible applications: (1) low cost, sensitive FM broadcast receivers, (2) SCA (Subsidiary Communications Authorization) receivers and (3) data receivers. The circuit schematic is shown in Figure 14. While this example has the greatest diversity of application, it is also the simplest. Two 10.7MHz ceramic filters were used. The first was directly connected to the output of the SA602. The second was directly connected to the output of the first IF limiter. The secondary sides of both filters were terminated with 330Ω as in the two previous examples. While the filter bandpass skew of this simple single conversion receiver might not be tolerable in some applications, to a first order the results are excellent. (Please note that sensitivity is measured at +20dB in this wideband example.) Performance is illustrated in Figure 15. +20dB SINAD was measured with 1.8µV input.

EXAMPLE: 152.2MHZ TO 10.7MHZ NARROWBAND

In this example (see Figure 16) a simple, effective, and relatively sensitive single conversion VHF receiver has been implemented. All of the circuit philosophy has been described in previous examples. In this circuit, tuned-transformed termination was used on the input and output sides of the crystal filter. Performance is shown in Figure 17. The +12dB SINAD sensitivity was 0.9µV.

OSCILLATORS

The SA602 contains an oscillator transistor which can be used to frequencies greater than 200MHz. Some of the possible configurations are shown in Figures 18 and 19.

L/C

When using a synthesizer, the LO must be externally buffered. Perhaps the simplest approach is an emitter follower with the base connected to Pin 7 of the SA602. The use of a dual-gate MOSFET will improve performance because it presents a fairly constant capacitance at its gate and because it has very high reverse isolation.

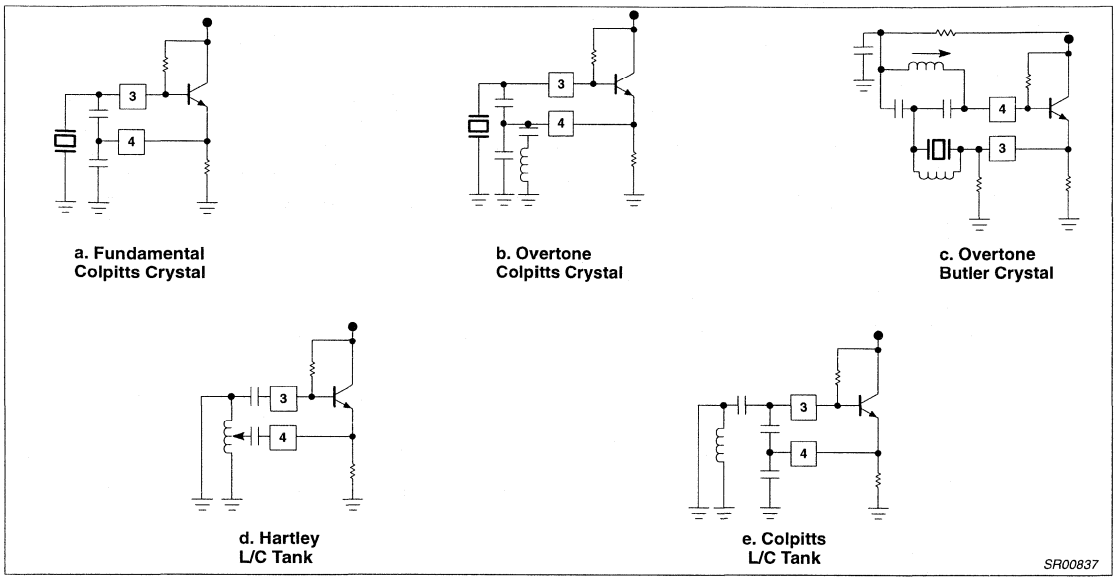

Figure 18. Oscillator Configurations

CRYSTAL

With both of the Colpitts crystal configurations, the load capacitance must be specified. In the overtone mode, this can become a sensitive issue since the capacitance from the emitter to ground is actually the equivalent capacitive reactance of the harmonic selection network. The Butler oscillator uses an overtone crystal specified for series mode operation (no parallel capacitance). It may require an extra inductor (L_o) to null out C_o of the crystal, but otherwise is fairly easy to implement (see references).

The oscillator transistor is biased with only 220µA. In order to assure oscillation in some configurations, it may be necessary to increase transconductance with an external resistor from the emitter to ground. 10kΩ to 20kΩ are acceptable values. Too small a resistance can upset DC bias (see references).

DATA DEMODULATION

It is possible to change any of the examples from an audio receiver to an amplitude shift keyed (ASK) or frequency shift keyed (FSK) receiver or both with the addition of an external op amp(s) or comparator(s). A simple example is shown in Figure 20. ASK decoding is accomplished by applying a comparator across the received signal strength indicator (RSSI). The RSSI will track IF level down to below the limits of the demodulator (–120dBm RF input in most of the examples). When an in-band signal is above the comparator threshold, the output logic level will change.

FSK demodulation takes advantage of the two audio outputs of the SA604A. Each is a PNP current source type output with 180° phase relationship. With no signal present, the quad tank tuned for the center of the IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the

IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the IF center, one output voltage will increase and the other will decrease by a corresponding absolute value. Thus, if a comparator is differentially connected across the two outputs, a frequency shift in one direction will drive the comparator output to one supply rail, and a frequency shift in the opposite direction will cause the comparator output to swing to the opposite rail. Using this technique, and L/C filtering for a wide IF bandwidth, NRZ data at rates greater than 4Mb have been processed with the new SA605.

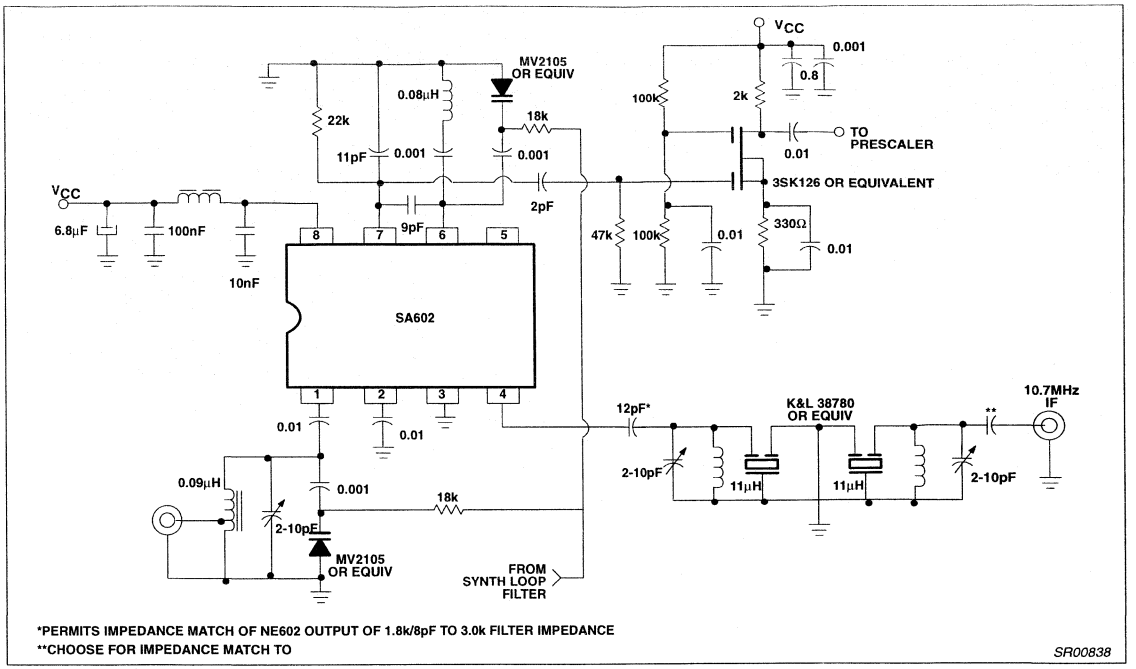

Figure 19. Typical Varactor Tuned Application

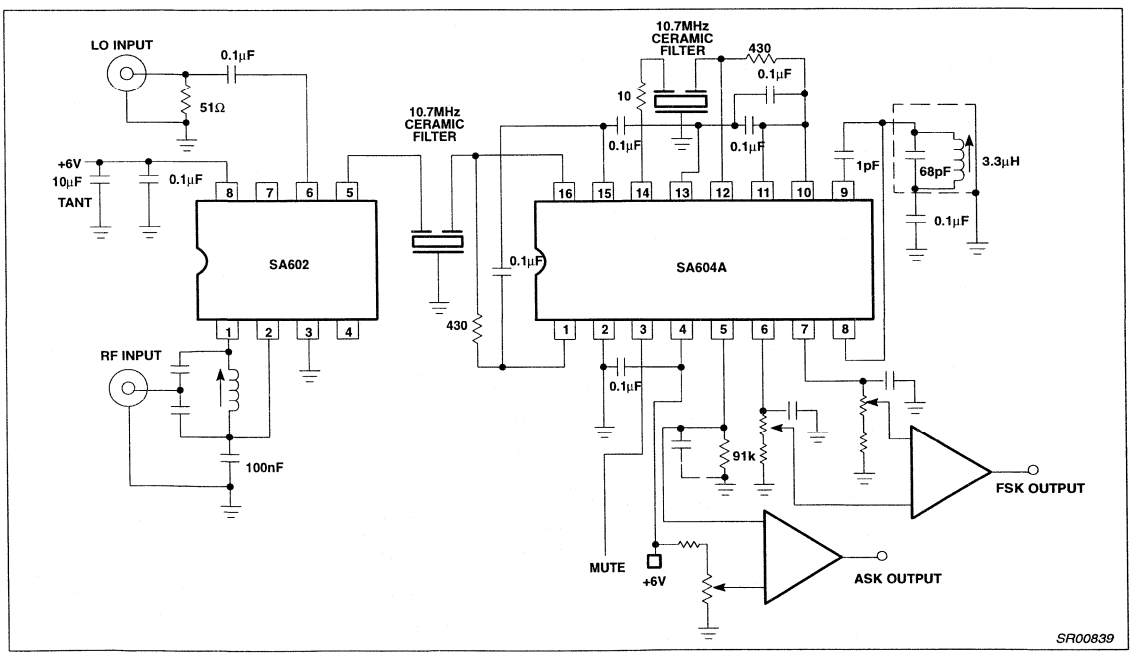

Figure 20. Basic SA602/604A Data Receiver

High sensitivity applications of low-power RF/IF integrated circuits

AN1993

SUMMARY

The SA602, SA604A and SA605 provide the RF system designer with the opportunity for excellent receiver or IF system sensitivity with very simple circuitry. IFs at 455kHz, 10.7MHz and 21.4MHz with 75 to 90dB gain are possible without special shielding. The flexible configuration of the built-in oscillator of the SA602/605 add to ease of implementation. Either data or audio can be recovered from the SA604A/605 outputs.

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3) Matthys, R.: "Survey of VHF Crystal Oscillator Circuits," RF Technology Expo Proceedings, pp 371-382, February, 1987.

4) Philips Semiconductors: "SA604A High Performance Low Power FM IF System", Linear Data and Applications Manual, Philips Semiconductors, 1987.

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6) Philips Semiconductors: "AN1982–Applying the Oscillator of the SA602 in Low Power Mixer Applications", Linear Data and Applications Manual, Philips Semiconductors, 1985.

Reviewing key areas when designing with the SA605 AN1994

Author: Alvin K. Wong

INTRODUCTION

This application note addresses key information that is needed when designing with the SA605. Since the SA602 and the SA604 are closely related to the SA605, a brief overview of these chips will be helpful. Additionally, this application note will divide the SA605 into four main blocks where a brief theory of operation, important parameters, specifications, tables and graphs of performance will be given. A question & answer section is included at the end. Below is an outline of this application note:

I. BACKGROUND

- History of the SA605
- Related app. notes

II. OVERVIEW OF THE SA605

- Mixer Section
  - RF section
  - Local osc. section
  - Output of mixer
  - Choosing the IF frequency
  - Performance graphs of mixer
- IF Section
  - IF amplifier
  - IF limiter
  - Function of IF section
  - Important parameters of IF section
    2. Limiting
    3. AM rejection
    4. AM to PM conversion
    5. Interstage loss
  - IF noise figure
  - Performance graphs of IF section
- Demodulator Section
- Output Section
  - Audio and unmuted audio
  - RSSI output
  - Performance graphs of output section

III.Question & Answers

I. BACKGROUND

History of the SA605

Before the SA605 was made, the SA602 (double-balanced mixer and oscillator) and the SA604 (FM IF system) existed. The combination of these two chips make up a high performance low cost receiver. Soon after the SA605 was created to be a one chip solution, using a newer manufacturing process and design. Since the newer process and design in the SA605 proved to be better in performance and reliability, it was decided to make the SA602 and the SA604 under this new process. The SA602A and the SA604A were created. To assist the cost-conscious customer, Philips Semiconductors also offered an inexpensive line of the same RF products: the SA612, SA614, and SA615.

Because the newer process and design proved to be better in performance and reliability, the older chips are going to be discontinued. Therefore, only the SA602A, SA612A, SA604A, SA614A, SA605 and SA615 will be available.

Figure 1 shows a brief summary of the RF chips mentioned above. Under the newer process, minor changes were made to improve the performance. A designer, converting from the SA602 to the SA602A, should have no problem with a direct switch. However, switching from the SA604 to the SA604A, might require more attention. This will depend on how good the original design was in the system. In the "Questions & Answers" section, the SA604 and SA604A are discussed in greater detail. This will help the designer, who used the SA604 in their original design, to switch to the "A" version. In general, a direct switch to the SA604A is simple.

Related Application Notes

There have been many application notes written on the SA602 and SA604A. Since the combination of those parts is very similar to the SA605, many of the ideas and applications still apply. In addition, many of the topics discussed here will also apply to the SA602A and SA604A.

Table 1 (see back of app note) shows the application notes available to the designer. They can be found in either the Philips Semiconductors Linear Data Manual, Volume 1, or the Philips Semiconductors RF Communications Handbook. Your local Philips Semiconductos sales representative can provide you with copies of these publications, or you can contact Philips Semiconductors Publication Services.

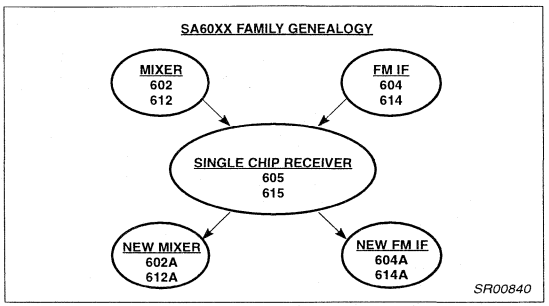


Figure 1. Overview of Selected RF Chips

II. OVERVIEW OF THE SA605

In Figure 2, the SA605 is broken up into four main areas; the mixer section, the IF section, the demodulator section and the output section. The information contained in each of the four areas focuses on important data to assist you with the use of the SA605 in any receiver application.

Mixer Section

There are three areas of interest that should be addressed when working with the mixer section. The RF signal, LO signal and the output. The function of the mixer is to give the sum/difference of the RF and LO frequencies to get an IF frequency out. This mixing of frequencies is done by a Gilbert Cell four quadrant multiplier. The Gilbert Cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell.

The RF input impedance of the mixer plays a vital role in determining the values of the matching network. Figure 3 shows the RF input impedance over a range of frequency. From this information, it can be determined that matching 50Ω at 45MHz requires matching to a 4.5kΩ resistor in parallel with a 2.5pF capacitor. An equivalent model can be seen in Figure 4 with its component values given for selected frequencies. Since there are many questions from the designer on how to match the RF input, an example is given below.

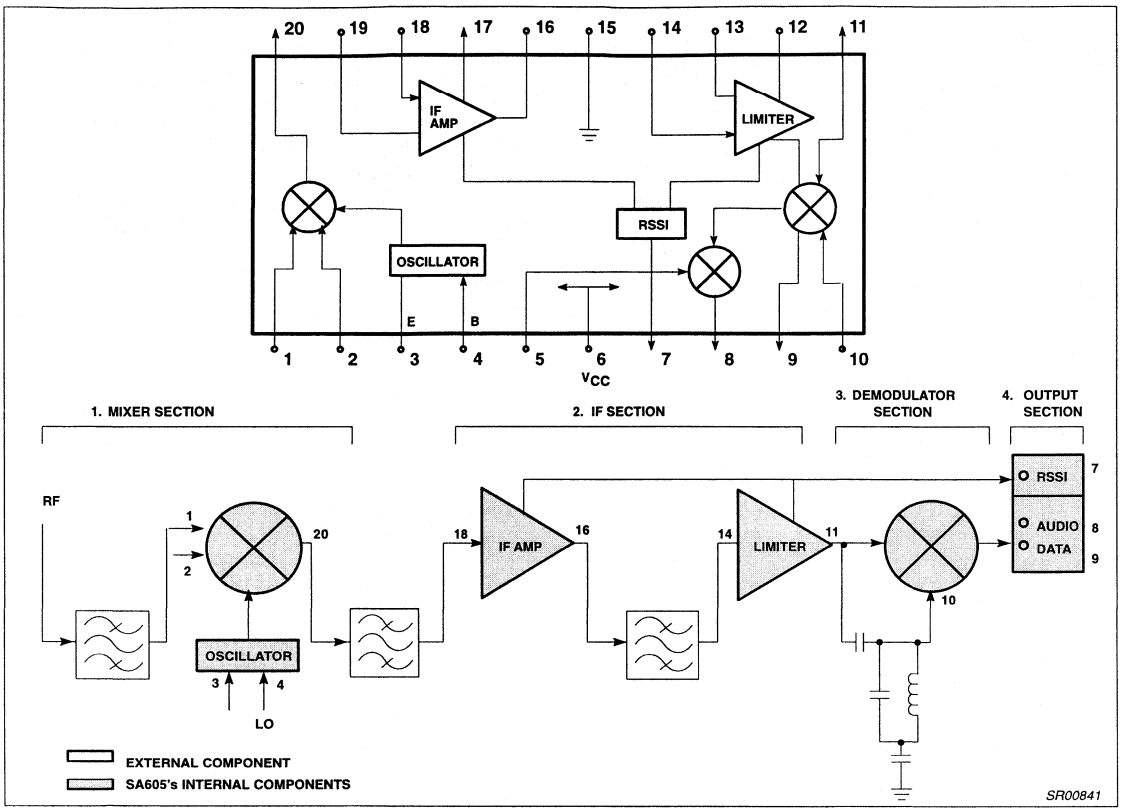


Figure 2. SA605 Broken Down into Four Areas

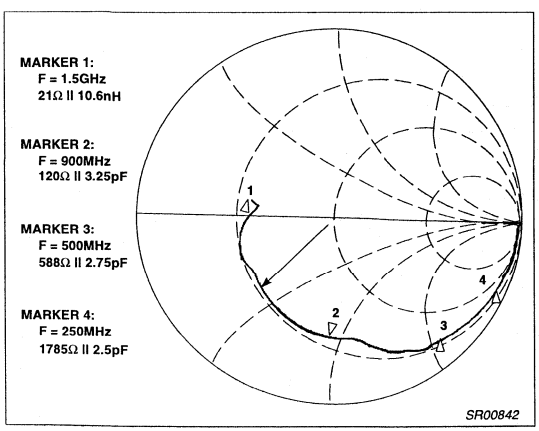


Figure 3. Smith Chart of SA605's RF Input Impedance (Pin 1 or 2)

RF Section of Mixer

The mixer has two RF input pins (Pin 1 and 2), allowing the user to choose between a balanced or unbalanced RF matching network. Table 2 (see back of app note) shows the advantages and disadvantages for either type of matching. Obviously, the better the matching network, the better the sensitivity of the receiver.

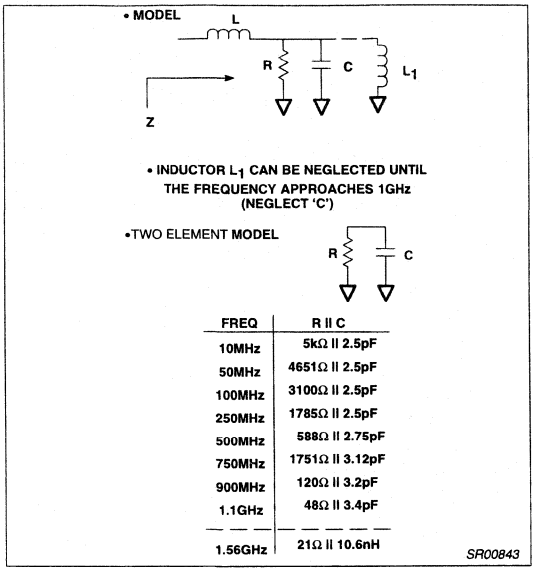


Figure 4. Equivalent Model of RF Input Impedance

Example: Using a tapped-C network, match a 50Ω source to the RF input of the SA605 at 45MHz. (refer to Figure 5)

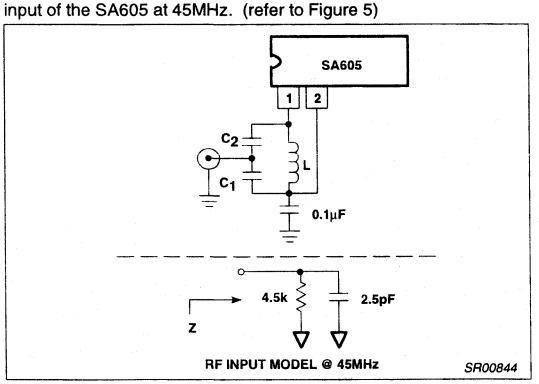


Figure 5. Tapped-C Network

Step 1. Choose an inductor value and its "Q" L = 0.22µH Q_P = 50 (specified by manufacturer)

Step 2. Find the reactance of the inductor

$X_P = 2\pi FL$

$= 2\pi\ (45MHz)\ (0.22\mu H)$

$\therefore\ X_P = 62.2\Omega$

Step 3. Then,

$R_P = Q_P X_P$

$= (50)(62.2)$

$\therefore\ R_P = 3.11k\Omega$ (the inductance resistance)

Step 4. $Q = R_{TOTAL}/X_P$

$= (R_S' // R_L // R_P) / X_P$

where $R_S' = R_L$

$= 4.5k // 4.5k // 3.11k / 62.2$

$= 21.39$

$\therefore\ Q \cong 21$ (the Q of the matching network)

where:

R_S = source resistance;

R_L = load resistance;

R_S' = what the source resistance should look like to match R_L;

R_P = inductance resistance

Step 5. $\frac{C1}{C2} = \sqrt{\frac{R_S'}{R_S}} - 1 = 8.6$

Step 6. $C_T = \frac{1}{X_P\ \omega} = \frac{1}{(62.2)\ 2\pi\ 45MHz}$

$= 56.86pF$

Step 7. using $C_T = \frac{C1C2}{C1 + C2}$

where $C_T = 56.86pF$, $\frac{C1}{C2} = 8.6$

$$C_T = \frac{C1}{\frac{C1}{C2} + 1}$$

$$\therefore\ C_1 = C_T\left(\frac{C1}{C2} + 1\right)$$

and $C_2 = \frac{C1}{8.6}$

thus...

C1 = 539pF

C2 = 64pF

L = 0.22µH (value started with)

Step 8. Frequency check

$$\omega = \frac{1}{\sqrt{LC}}$$

$$2\pi F = \frac{1}{\sqrt{LC}}$$

F = 45MHz (...so far so good)

Step 9. Taking care of the 2.5pF capacitor that is present at the RF input at 45MHz $\frac{C2_A}{C1_A} = \frac{64pF}{540pF}$ Eq. 1.

$$C_{TN} = \frac{C1_A C2_A}{C1_A + C2_A}$$ Eq. 2.

where $C_{TN} = C_T - 2.5pF$
(recall value of C_T from Step 6.)

Making use of Equations 1 and 2, the new values of C1 and C2 are:
$C1_A = 524pF$
$C2_A = 60.6pF$

[NOTE: At this frequency the 2.5pF capacitor could probably be ignored since its value at 45MHz has little effect on C1 and C2.]

Step 10. Checking the bandwidth $Q = \frac{F}{BW}$

$$BW = F_U - F_L$$

BW = bandwidth

F_U = upper 3dB frequency

F_L = lower 3dB frequency

Using the above formulas results in
F_U = 46MHz
F_L = 44MHz
BW = 2MHz

The above shows the calculations for a single-ended match to the SA605. For a balanced matching network, a transformer can be used. The same type of calculations will still apply once the input impedance of the SA605 is converted to the primary side of the transformer (see Figure 6). But before we transform the input impedance to the primary side, we must first find the new input impedance of the SA605 for a balanced configuration. Because we have a balanced input, the 4.5kΩ transforms to 9kΩ (4.5k + 4.5k = 9k) while the capacitor changes from 2.5pF to 1.3pF (2.5pF in series with 2.5pF is 1.3pF). Notice that the resistor values double while the capacitor values are halved. Now the 9kΩ resistor in parallel with the 1.3pF capacitor must be transformed to the primary side of the transformer (see Figure 6).

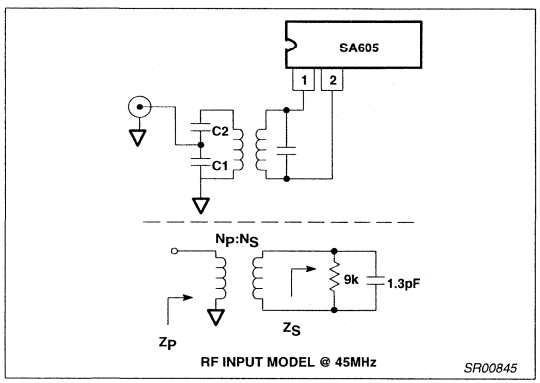


Figure 6. Using a Transformer to Achieve a Balanced Match

Procedure:

Step 1. $\frac{Z_P}{Z_S} = \left(\frac{N_P}{N_S}\right)^2$

where:
Z_P = impedance of primary side
Z_S = impedance of secondary side
N_P = number of turns on primary side
N_S = number of turns on secondary side

Step 2. Recall,

$Z_S = R \parallel X_C$
$Z_S = 9k \parallel j2.7k$
where
$R = 9k$ $X_C = \frac{1}{2\pi FC} = 2.7k$ at $F = 45MHz$

Step 3. Assume 1:N turns ratio for the transformer

$Z_P = \frac{Z_S}{N^2} = 2.25k \parallel j\ 680$

(assuming N = 2)

Step 4.

$\therefore C = \frac{1}{2\pi\ FX_C} = 5.2pF$

R = 2.25k
(these are the new values to match using the formulas in tapped-C)

Step 5. Because the transformer has a magnetization inductance L_M, (inductance presented by the transformer), we can eliminate the inductor used in the previous example and tune the tapped-C network with the inductance presented by the transformer.
Lets assume L_M = 0.22µH (Q=50) Therefore
C1 = 381pF
C2 = 66.8pF
F_U = 46.7MHz
F_L = 43.3MHz
BW = 3.4MHz
taking the input capacitor into consideration
C1 = 347pF
C2 = 61pF
L = 0.22µH (Q=50)

Because of leakage inductance, the transformer is far from ideal. All of these leakages affect the secondary voltage under load which will seem like the indicated turns ratio is wrong. The above calculations show one method of impedance matching. The values calculated for C1 and C2 do not take into account board parasitic capacitance, and are, therefore, only theoretical values. There are many ways to configure and calculate matching networks. One alternative is a tapped-L configuration. But the ratio of the tapped-C network is easier to implement than ordering a special inductor. The calculations of these networks can be done on the Smith Chart. Furthermore, there are many computer programs available which will help match the circuit for the designer.

Local Oscillator Section of Mixer

The SA605 provides an NPN transistor for the local oscillator where only external components like capacitors, inductors, or resistors need to be added to achieve the LO frequency. The oscillator's transistor base and emitter (Pins 4 and 3 respectively) are available to be configured in Colpitts, Butler or varactor controlled LC forms. Referring to Figure 7, the collector is internally connected directly to V_{CC}, while the emitter is connected through a 25kΩ resistor to ground. Base bias is also internally supplied through an 18kΩ resistor. A buffer/divider reduces the oscillator level by a factor of three before it is applied across the upper tree of the Gilbert Cell. The divider de-sensitizes the mixer to oscillator level variations with temperature and voltage. A typical value for the LO input impedance is approximately 10kΩ.

The highest LO frequency that can be achieved is approximately 300MHz with a 200mV_{RMS} signal on the base (Pin 4). Although it is possible to exceed the 300MHz LO frequency for the on-board oscillator, it is not really practical because the signal level drops too low for the Gilbert Cell. If an application requires a higher LO frequency, an external oscillator can be used with its 200mV_{RMS} signal injected at Pin 4 through a DC blocking capacitor. Table 3 (see back of app note) can be used as a guideline to determine which configuration is best for the required LO frequency.

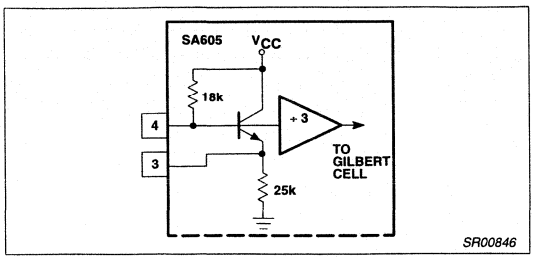


Figure 7. On-board NPN Transistor for Local Oscillator

Because the Colpitts configuration is for parallel resonance mode, it is important to know, when ordering crystals, that the load capacitance of the SA605 is 10pF. However, for the Butler configuration, the load capacitance is unimportant since the crystal will be in the series mode. Figure 8 shows the different types of LO configurations used with SA605.

If a person decides to use the Colpitts configuration in their design, they will probably find that most crystal manufacturers have their own set of standards of load capacitance. And in most cases, they are unwilling to build a special test jig for an individual's needs. If this occurs, the designer should tell them to go ahead with the design. But, the designer should also be ready to accept the crystal's frequency to be off by 200–300Hz from the specified frequency. Then a test jig provided by the designer and a 2nd iteration will solve the problem.

Output of Mixer

Once the RF and LO inputs have been properly connected, the output of the mixer supplies the IF frequency. Knowing that the mixer's output has an impedance of 1.5kΩ, matching to an IF filter should be trivial.

Choosing the Appropriate IF Frequency

Some of the standard IF frequencies used in industry are 455kHz, 10.7MHz and 21.4MHz. Selection of other IF frequencies is possible. However, this approach could be expensive because the filter manufacturer will probably have to build the odd IF filter from scratch.

There are several advantages and disadvantages in choosing a low or high IF frequency. Choosing a low IF frequency like 455kHz can provide good stability, high sensitivity and gain. Unfortunately, it can also present a problem with the image frequency (assuming single conversion). To improve the image rejection problem, a higher IF frequency can be used. However, sensitivity is decreased and the gain of the IF section must be reduced to prevent oscillations.

If the design requires a low IF frequency and good image rejection, it is best to use the double conversion method. This method allows the best of both worlds. Additionally, it is much easier to work with a lower IF frequency because the layout will not be as critical and will be more forgiving in production. The only drawback to this method is that it will require another mixer and LO. But, a transistor can be used for the first mixer stage (which is an inexpensive approach) and the SA605 can be used for the second mixer stage. The SA602A can also be used for the first conversion stage if the transistor approach does not meet the design requirements.

If the design requires a high IF frequency, good layout and RF techniques must be exercised. If the layout is sound and instability still occurs, refer to the "RSSI output" section which suggests solutions to these types of problems.

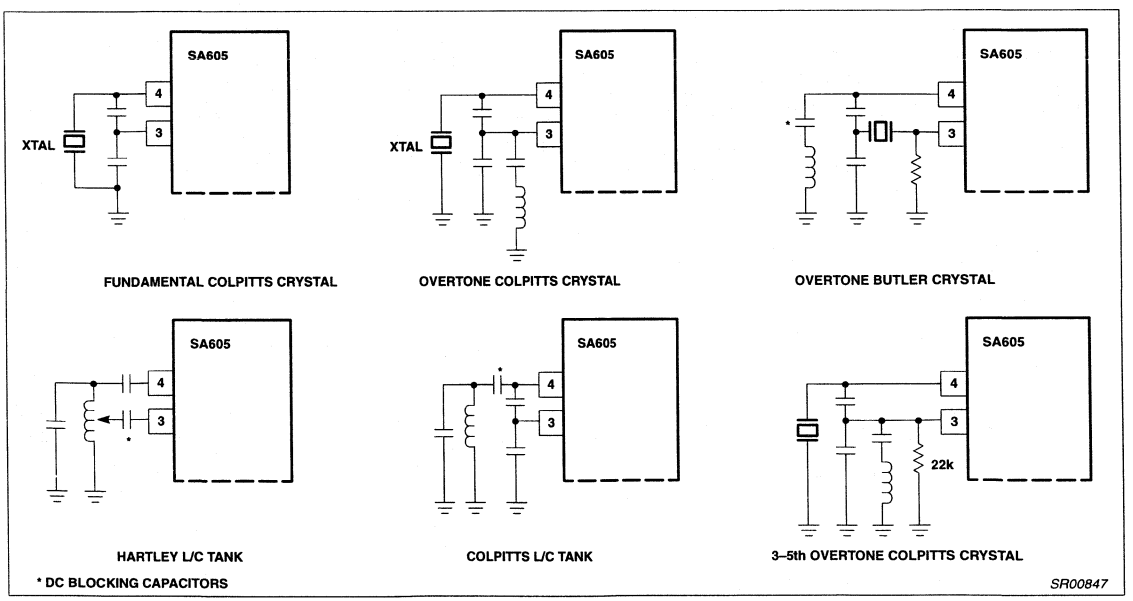


Figure 8. Oscillator Configurations

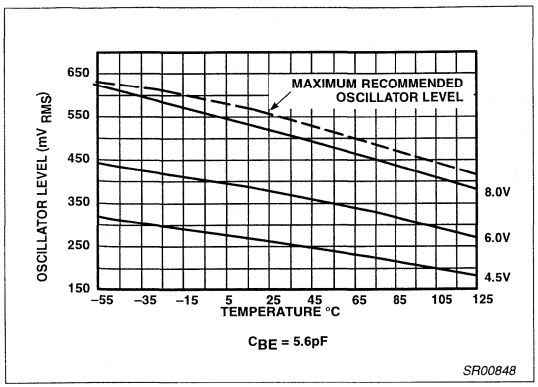


Figure 9. SA605 Application Oscillator Level

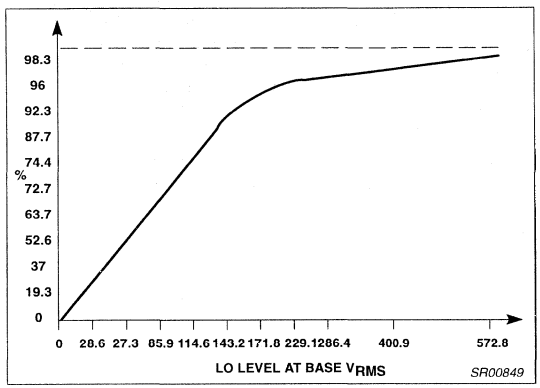


Figure 10. Mixer Efficiency vs Normalized LO Level

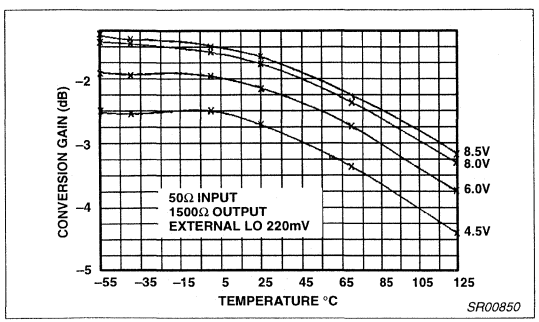


Figure 11. 50Ω Conversion Gain

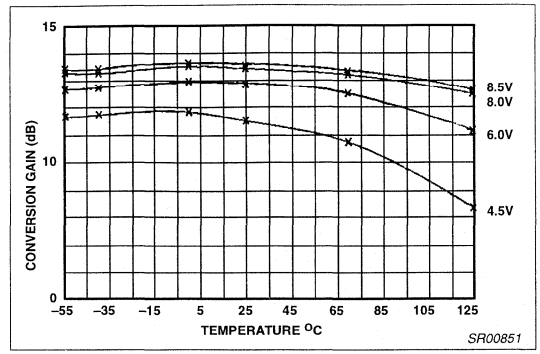


Figure 12. Single-Ended Matched Input Conversion Gain (50Ω to 1.5kΩ, 14.5dB Matching Step-up Network)

Performance Graphs of Mixer

Fig.	Description
9	Oscillator Levels vs. Temperature with Different Supply Voltages for the 44.545MHz Crystal Colpitts Applications
10	LO Efficiency vs. Normalized Peak Level at the Base of the Oscillator Transistor
11	50Ω Conversion Gain vs. Temperature with Different Supply Voltages Using an External LO
12	Mixer Matched Input Conversion Gain vs. Temperature with Different Supply Voltages
13	IF Output Power vs. RF Input Level (3rd-order Intercept Point) 1st mixer = diode mxr, 2nd mixer = 605 mxr
14	SA605 and Diode Mixer Test Set Up
15	SA605 LO Power Requirements vs. Diode Mixer
16	SA605 Conversion Gain vs. Diode Mixer
17	Comparing Intercept Points with Different Types of Mixers

Another issue to consider when determining an IF frequency is the modulation. For example, a narrowband FM signal (30kHz IF bandwidth) can be done with an IF of 455kHz. But for a wideband FM signal (200kHz IF bandwidth), a higher IF is required, such as 10.7MHz or 21.4MHz.

IF Section

The IF section consists of an IF amplifier and IF limiter. With the amplifier and limiter working together, 100dB of gain with a 25MHz bandwidth can be achieved (see Figure 18). The linearity of the RSSI output is directly affected by the IF section and will be discussed in more detail later in this application note.

IF Amplifier

The IF amplifier is made up of two differential amplifiers with 40dB of gain and a small signal bandwidth of 41MHz (when driven by a 50Ω source). The output is a low impedance emitter follower with an

output resistance of about 230Ω, and an internal series build out of 700Ω to give a total of 930Ω. One can expect a 6dB loss in each amplifier's input since both of the differential amplifiers are single-ended.

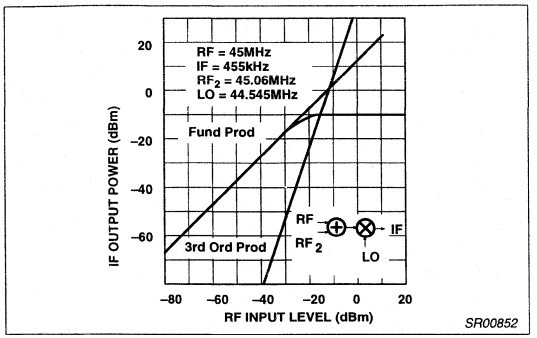


Figure 13. Third-Order Intercept and Compression

The basic function of the IF amp is to boost the IF signal and to help handle impulse noise. The IF amp will not provide good limiting over a wide range of input signals, which is why the IF limiter is needed.

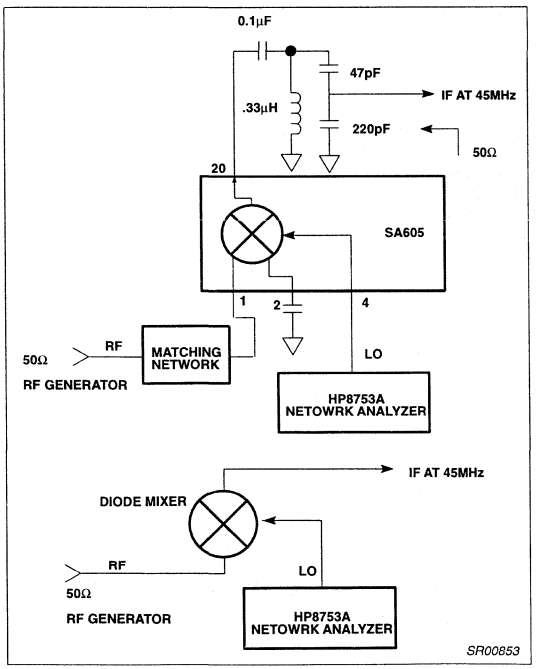


Figure 14. Test Circuits for SA605 Mixer vs Diode Mixer

IF Limiter

The IF limiter is made up of three differential amplifiers with a gain of 63dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. The IF limiter's output resistance is about 260Ω with no internal build-out. The limiter's output signal (Pin 9 onSA604A, Pin 11 on SA605) will vary from a good approximation of a square wave at lower IF frequencies like 455kHz, to a distorted sinusoid at higher IF frequencies, like 21.4MHz.

The basic function of the IF limiter is to apply a tremendous amount of gain to the IF frequency such that the top and bottom of the waveform are clipped. This helps in reducing AM and noise presented upon reception.

Function of IF Section

The main function of the IF section is to clean up the IF frequency from noise and amplitude modulation (AM) that might occur upon reception of the RF signal. If the IF section has too much gain, then one could run into instability problems. This is where crucial layout and insertion loss can help (also addressed later in this paper).

Important Parameters for the IF Section

Limiting: The audio output level of an FM receiver normally does not change with the RF level due to the limiting action. But as the RF signal level continues to decrease, the limiter will eventually run out of gain and the audio level will finally start to drop. The point where the IF section runs out of gain and the audio level decreases by 3dB with the RF input is referred to as the –3dB limiting point.

In the application test circuit, with a 5.1kΩ interstage resistor, audio suppression is dominated by noise capture down to about the –120dBm RF level at which point the phase detector efficiency begins to drop (see Interstage Loss section below).

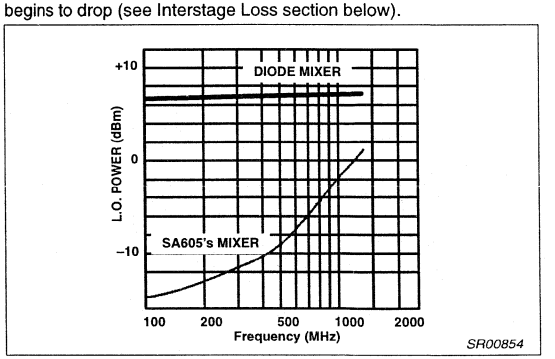


Figure 15. LO Power Requirements (Matched Input)

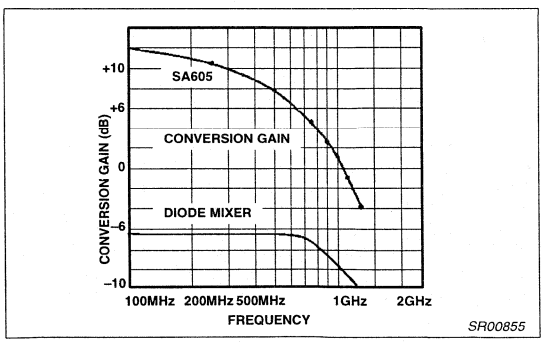


Figure 16. SA605 Conversion Gain vs. Diode Mixer

The audio drop that occurs is a function of two types of limiting. The first type is as follows: As the input signal drops below a level which is sufficient to keep the phase detector compressed, the efficiency of the detector drops, resulting in premature audio attenuation. We will call this "gain limiting". The second type of limiting occurs when there is sufficient amount of gain without de-stabilizing regeneration (i.e. keeping the phase detector fully limited), the audio level will eventually become suppressed as the noise captures the receiver. We will call this "limiting due to noise capture".

Figure 19 shows the 3dB drop in audio at about $0.26\mu V_{RMS}$, with a –118.7dBm/50Ω RF level for the SA605. Note that the level has not improved by the 11dB gain supplied by the mixer/filter since noise capture is expected to slightly dominate here.

AM rejection: The AM rejection provided by the SA605/604A is extremely good even for 80% modulation indices as depicted in Figures 20a through 20d. This performance results from the 370mV peak signal levels set at the input of each IF amplifier and limiter stage. For this level of compression at the inputs, even better performance could be expected except that finite AM to PM conversion coefficients limit ultimate performance for high level inputs as indicated in Figure 20b.

Low level AM rejection performance degrades as each stage comes out of limiting. In particular as the quadrature phase detector input drops below 100mV peak, all limiting will be lost and AM modulation will be present at the input of the quad detector (See Figure 20d).

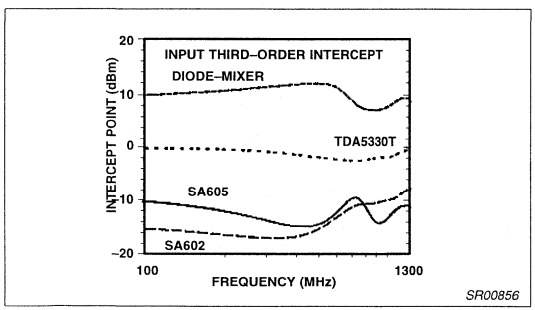


Figure 17. Comparing Different Types of Mixers

AM to PM conversion: Although AM rejection should continue to improve above –95dBm IF inputs, higher order effects, lumped under the term AM to PM conversion, limit the application rejection to about 40dB. In fact this value is proportional to the maximum frequency deviation. That is lower deviations producing lower audio outputs result directly in lower AM rejection. This is consistent with the fact that the interfering audio signal produced by the AM/PM conversion process is independent of deviation within the IF bandwidth and depends to a first estimate on the level of AM modulation present. As an example reducing the maximum frequency deviation to 4kHz from 8kHz, will result in 34dB AM rejection. If the AM modulation is reduced from 80% to 40%, the AM rejection for higher level IFs will go back to 40dB as expected. AM to PM conversion is also not a function of the quad tank Q, since an increase in Q increases both the audio and spurious AM to PM converted signal equally.

As seen above, these relationships and the measured results on the application board (Figure 36) can be used to estimate high level IF AM rejection. For higher frequency IFs (such as 21.4MHz), the limiter's output will start to deviate from a true square wave due to lack of bandwidth. This causes additional AM rejection degradation.

Interstage Loss: Figure 21 plots the simulated IF RSSI magnitude response for various interstage attenuation. The optimum interstage loss is 12dB. This has been chosen to allow the use of various types of filters, without upsetting the RSSI's linearity. In most cases, the filter insertion loss is less than 12dB from point A to point B. Therefore, some additional loss must be introduced externally. The easiest and simplest way is to use an external resistor in series with the internal build out resistor (Pin 14 in the SA604A, Pin 16 in the SA605). Unfortunately, this method mismatches the filter which might be important depending on the design. To achieve the 12dB insertion loss and good matching to the filter, an L-pad configuration can be used. Figure 22 shows the different set-ups.

Below is an example on how to calculate the resistors values for R_{EXT} in Figure 22A.

$$X_{dB} = 20\log\frac{\sqrt{(960 + R_{EXT})\,R_{FLT}}}{960 + R_{EXT} + R_{FLT}} - FIL\ [dB]$$

where
X = the insertions loss wanted in dB
R_{EXT} = the external resistor
R_{FLT} = the filter's input impedance
FIL = insertion loss of filter in dB

For the application board:
X=12dB
R_{FLT} = 1.5k
FIL = 3dB
Therefore, using the above eq. gives
R_{EXT} = 5.1K

Below are the design equations for calculating R_{SERIES} and R_{SHUNT} in Figure 22b.

$$R_{SERIES} = \left| 960 - \frac{R_{FLT}}{2 \times 10^{\left(\frac{-X_{dB}}{20}\right)}} \right|$$

$$R_{SHUNT} = \frac{R_{FLT}}{1 - 2 \times 10^{\left(\frac{-X_{dB}}{20}\right)}}$$

In this case, lets assume: FIL = 2dB therefore, X_{dB} = +10, R_{FLT} = 1.5k. The results are: R_{SERIES} = 1.41k, R_{SHUNT} = 4.08k

IF noise figure

The IF noise figure of the receiver may be expected to provide at best a 7.7dB noise figure in a 1.5kΩ environment from about 25kHz to 100MHz. From a 25Ω source the noise figure can be expected to degrade to about 15.4db.

Performance Graphs of IF Section

Fig.	Description
24	IF Amp Gain vs. Temperature with Various Supply Voltages
25	IF Limiter Gain vs. Temperature with Various Supply Voltages
26	IF Amp 20MHz Response vs. Temperature
27	IF Limiter 20MHz Response vs. Temperature

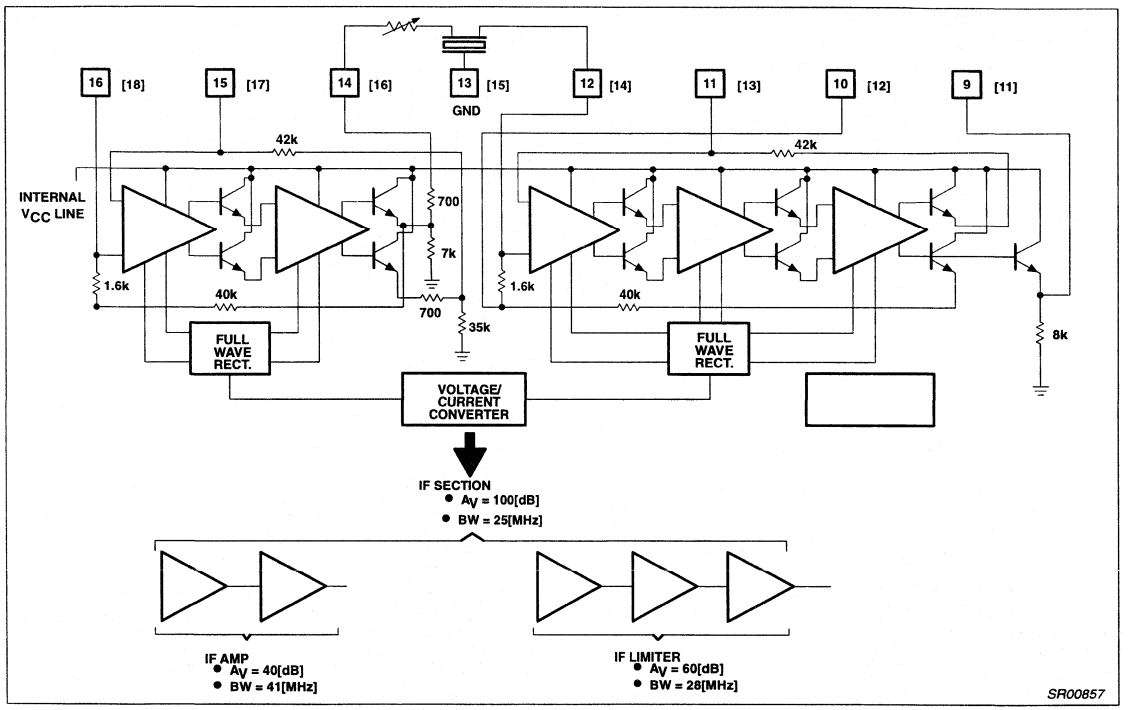


Figure 18. IF Section of SA604A [SA605]

Demodulator Section

Once the signal leaves the IF limiter, it must be demodulated so that the baseband signal can be separated from the IF signal. This is accomplished by the quadrature detector. The detector is made up of a phase comparator (internal to theSA605) and a quadrature tank (external to the SA605).

The phase comparator is a multiplier cell, similar to that of a mixer stage. Instead of mixing two different frequencies, it compares the phases of two signals of the same frequency. Because the phase comparator needs two input signals to extract the information, the IF limiter has a balanced output. One of the outputs is directly connected to the input of the phase comparator. The other signal from the limiter's output (Pin 11) is phase shifted 90 degrees (through external components) and frequency selected by the quadrature tank. This signal is then connected to the other input of the phase comparator (Pin 10 of the SA605). The signal coming out of the quadrature detector (phase detector) is then low-passed filtered to get the baseband signal. A mathematical derivation of this can be seen in the SA604A data sheet.

The quadrature tank plays an important role in the quality of the baseband signal. It determines the distortion and the audio output amplitude. If the "Q" is high for the quadrature tank, the audio level will be high, but the distortion will also be high. If the "Q" is low, the

distortion will be low, but the audio level will become low. One can conclude that there is a trade-off.

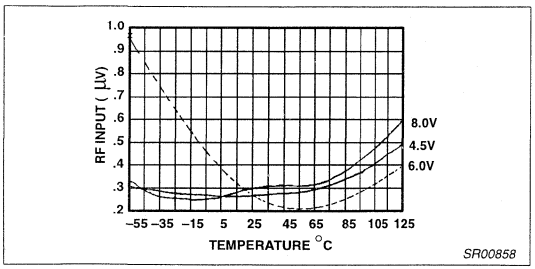


Figure 19. SA605 Application Board, –3dB Limiting (Drop in Audio)

Output Section

The output section contains an RSSI, audio, and data (unmuted audio) outputs which can be found on Pins 7, 8, and 9, respectively, on the SA605. However, amplitude shift keying (ASK), frequency shift keying (FSK), and a squelch control can be implemented from these pins. Information on ASK and FSK can be found in Philips Semiconductors application note AN1993.

Although the squelch control can be implemented by using the RSSI output, it is not a good practice. A better way of implementing squelch control is by comparing the bandpassed audio signal to high frequency colored FM noise signal from the unmuted audio. When no baseband signal is present, the noise coming out of the unmuted audio output will be stronger, due to the nature of FM noise. Therefore, the output of the external comparator will go high (connected to Pin 5 of the SA605) which will mute the audio output. When a baseband signal is present, the bandpassed audio level will dominate and the audio output will now unmute the audio.

Audio and Unmuted Audio (Data)

The audio and unmuted audio outputs (Pin 8 and 9, respectively, on the SA605) will be discussed in this section because they are basically the same. The only difference between them is that the unmuted audio output is always "on" while the audio output can either be turned "on" or "off". The unmuted audio output (data out) is for signaling tones in systems such as cellular radio. This allows the tones to be processed by the system but remain silent to the user. Since these tones contain information for cellular operation, the unmuted audio output can also be referred to as the "data" output. Grounding Pin 5 on the SA605 mutes the audio on Pin 8 (connecting Pin 5 to V_{CC} unmutes it).

Both of these outputs are PNP current-to-voltage converters with a 55kΩ nominal internal load. The nominal frequency response of the audio and data outputs are 300kHz. However, this response can be increased with the addition of an external resistor (<58kΩ) from the output pins to ground. This will affect the time constant and lower the audio's output amplitude. This technique can be applied to SCA receivers and data transceivers (as mentioned in the SA604A data sheet).

RSSI Output

RSSI (Received Signal Strength Indicator) determines how well the received signal is being captured by providing a voltage level on its output. The higher the voltage, the stronger the signal.

The RSSI output is a current-to-voltage converter, similar to the audio outputs. However, a 91kΩ external resistor is needed to get an output characteristic of 0.5V for every 20dB change in the input amplitude.

As mentioned earlier, the linearity of the RSSI curve depends on the 12dB insertion loss between the IF amplifier and IF limiter. The reason the RSSI output is dependent on the IF section is because of the V/I converters. The amount of current in this section is monitored to produce the RSSI output signal. Thus, the IF amplifier's rectifier is internally calibrated under the assumption that the loss is 12dB.

Because unfiltered signals at the limiter inputs, spurious products, or regenerated signals will affect the RSSI curve, the RSSI is a good indicator in determining the stability of the board's layout. With no signal applied to the front end of the SA605, the RSSI voltage level should read 250mV_{RMS} or less to be a good layout. If the voltage output is higher, then this could indicate oscillations or regeneration in the design.

Referring to the SA604A data sheet, there are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can be accomplished by adding attenuation between stages. More details on regeneration and stability considerations can be found in the SA604A data sheet.

Performance Graphs of Output Section

Fig.	Description
28	51kΩ Thermistor in Series with 100kΩ Resistor Across Quad Tank (Thermistor Quad Q Compensation)
29a	SA605 Application Board at –55°C
29b	SA605 Application Board at –40°C
29c	SA605 Application Board at +25°C
29d	SA605 Application Board at +85°C
29e	SA605 Application Board at +125°C
30a	SA604A for –68dBm RSSI Output vs. Temperature at Different Supply Voltages
30b	SA604A for –18dBm RSSI Output vs. Temperature at Different Supply Voltages
30c	SA605 for –120dBm RSSI Output vs. Temperature at Different Supply Voltages
30d	SA605 for –76dBm RSSI Output vs. Temperature at Different Supply Voltages
30e	SA605 for –28dBm RSSI Output vs. Temperature at different Supply Voltages
31	SA605 Audio level vs. Temperature and Supply Voltage
32	SA605 Data Output at –76dBm vs. Temperature

III. QUESTIONS & ANSWERS:

Q.–Bypass. How important is the effect of the power supply bypass on the receiver performance?

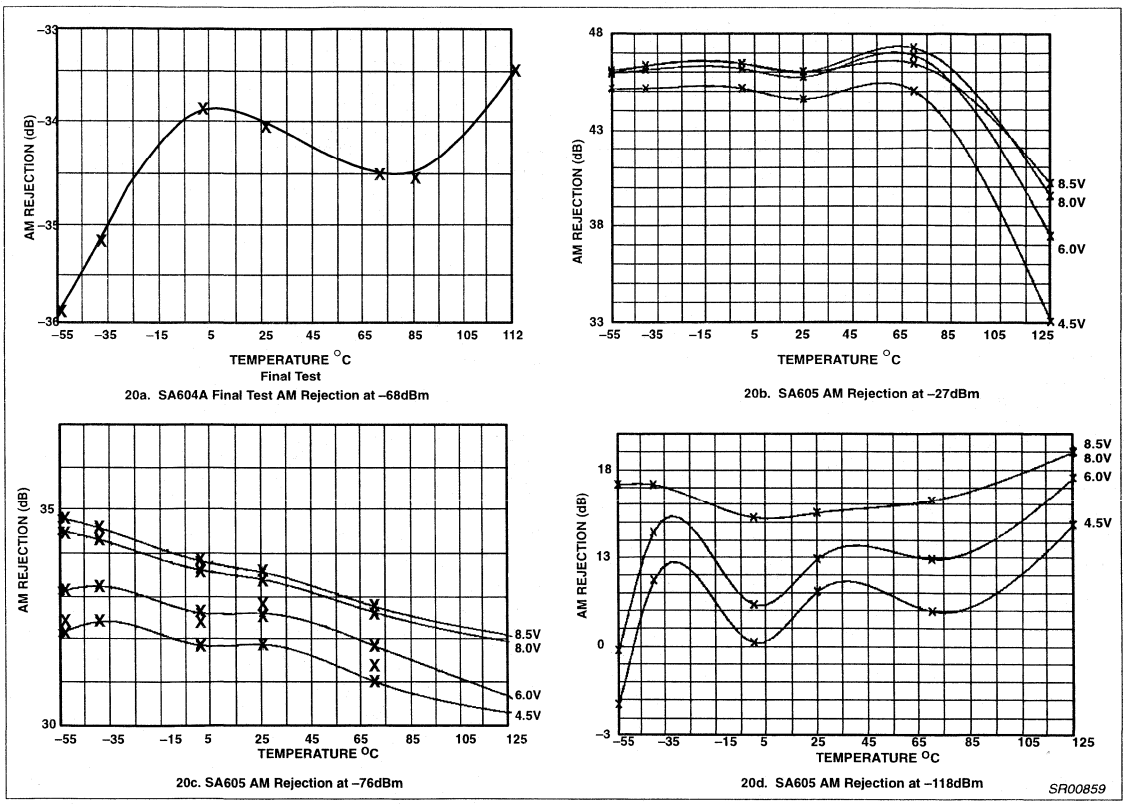
A. While careful layout is extremely critical, one of the single most neglected components is the power supply bypass in applications of SA604A or SA605. Although increasing the value of the tantalum capacitor can solve the problem, more careful testing shows that it is actually the capacitor's ESR (Equivalent Series Resistance) that needs to be checked. The simplest way of screening the bypass

capacitor is to test the capacitor's dissipation factor at a low frequency (a very easy test, because most of the low frequency capacitance meters display both C, and Dissipation factor).

Q.–On-chip oscillator. We cannot get the SA605 on-chip oscillator to work. What is the problem?

A. The on board oscillator is just one transistor with a collector that is connected to the supply, an emitter that goes to ground through a 25k resistor, and a base that goes to the supply through an 18k resistor. The rest of the circuit is a buffer that follows the oscillator from the transistor base (this buffer does not affect the performance of the oscillator).

Fundamental mode Colpitts crystal oscillators are good up to 30MHz and can be made by a crystal and two external capacitors. At higher frequencies, up to about 90MHz, overtone crystal oscillators (Colpitts) can be made like the one in the cellular application circuit. At higher frequencies, up to about 170MHz, Butler type oscillators (the crystal is in series mode) have been successfully demonstrated. Because of the 8GHz peak f_T of the transistors, LC Colpitts oscillators have been shown to work up to 900MHz. The problem encountered above 400MHz is that the on-chip oscillator level is not sufficient for optimum conversion gain of the mixer. As a result, an external oscillator should be used at those frequencies.



20a. SA604A Final Test AM Rejection at –68dBm

20b. SA605 AM Rejection at –27dBm

20c. SA605 AM Rejection at –76dBm

20d. SA605 AM Rejection at –118dBm

Figure 20. AM Rejection Results at Different Input Levels

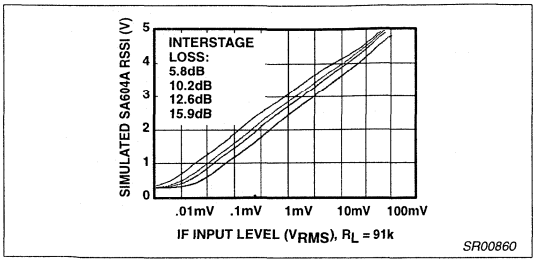


Figure 21. SA604A's RSSI Curve at Different Interstage Losses

Generally, about 220mV$_{RMS}$ is the oscillator level needed on Pin 4 for maximum conversion gain of the mixer. An external oscillator driving Pin 4 can be used throughout the band. Finally, since the SA605's oscillator is similar to the SA602, all of the available application notes on SA602 apply to this case (assuming the pin out differences are taken into account by the user).

Below are a couple of points to help in the oscillator design. The oscillator transistor is biased around 250μA which makes it very hard to probe the base and emitter without disturbing the oscillator (a high impedance, low capacitance active FET probe is desirable). To solve these problems, an external 22k resistor (as low as 10k) can be used from Pin 3 to ground to double the bias current of the oscillator transistor. This external resistor is put there to ensure the start up of the crystal in the 80MHz range, and to increase the f_T of the transistor for above 300–400MHz operation. Additionally, this resistor is required for operations above 80–90MHz. When a 1k resistor from Pin 1 to ground is connected on the SA605, half of the mixer will shut off. This causes the mixer to act like an amplifier. As a result, Pin 20 (the mixer, now amplifier output) can be probed to measure the oscillator frequency. Furthermore, the signal at Pin 20 relates to the true oscillator level . This second resistor is just for optimizing the oscillator of course. Without the 1k resistor, the signal at Pin 20 will be a LO feedthrough which is very small and frequency dependent.

Finally in some very early data sheets, the base and emitter pins of the oscillator were inadvertently interchanged. The base pin is Pin 4, and the emitter pin is Pin 3. Make sure that your circuit is connected correctly.

Q.–Sensitivity at higher input frequencies. We cannot get good sensitivity like the 45MHz case at input frequencies above 70MHz. Do you have any information on sensitivity vs. input frequency?

A. The noise figure and the gain of the mixer degrade by less than 0.5dB, going from 50 to 100MHz. Therefore, this does not explain the poor degradation in sensitivity. If other problems such as layout, supply bypass etc. are already accounted for, the source of the problem can be regeneration due to the 70MHz oscillator. What is probably happening is that the oscillator signal is feeding through the IF, getting mixed with the 455kHz signal, causing spurious regeneration. The solution is to reduce the overall gain to stop the regeneration.

This gain reduction can be done in a number of places. Two simple points are the attenuator network before the second filter and the LO level (see Figure 22). The second case will reduce the mixer's noise figure which is not desirable. Therefore, increasing the Interstage loss, despite minimal effect on the RSSI linearity, is the correct solution. As the Interstage loss is increased, the regeneration problem is decreased, which improves sensitivity, despite lowering of the over-all gain (the lowest RSSI level will keep decreasing as the regeneration problem is decreased). For an 81MHz circuit it was found that increasing the Interstage loss from 12dB to about 17dB produced the best results (–119dBm sensitivity). Of course, adding any more Interstage loss will start degrading sensitivity.

Conversely, dealing with the oscillator design, low LO levels could greatly reduce the mixer conversion gain and cause degradation of the sensitivity. For the 81MHz example, a 22k parallel resistor from Pin 3 to ground is required for oscillator operation where a Colpitts oscillator like the one in the cellular application circuit is used. The LO level at Pin 4 should be around 220mV$_{RMS}$ for good operation. Lowering the LO level to approximately 150mV$_{RMS}$ may be a good way of achieving stability if increasing Interstage attenuation is not acceptable. In that case the 22k resistor can be made a thermistor to adjust the LO level vs. temperature for maintaining sensitivity and ensuring crystal start-up vs. temperature. At higher IF frequencies (above 30MHz), the interstage gain reduction is not needed. The bandwidth of the IF section will lower the overall gain. So, the possibility of regeneration decreases.

Q.–Mixer noise figure. How do you measure the mixer noise figure in SA605, and SA602?

A. We use the test circuit shown in the SA602 data sheet. The noise figure tester is the HP8970A. The noise source we use is the HP346B (ENR = 15.46dB). Note that the output is tuned for 10.7MHz. From that test circuit the NF-meter measures a gain of approximately 15dB and 5.5dB noise figure.

More noise figure data is available in the paper titled "Gilbert-type Mixers vs. Diode Mixers" presented at RF Expo '89 in Santa Clara, California. (Reprints available through Philips Semiconductors Publication Services.)

Q.– What is the value of the series resistor before the IF filter in the SA605 or SA604A applications?

A. A value of 5.1kΩ has been used by us in our demo board. This results in a maximally straight RSSI curve. A lower value of about 1k will match the filter better. A better solution is to use an L pad as discussed earlier in this application note.

Q.– What is the low frequency input resistance of the SA605?

A. The data sheets indicated a worst case absolute minimum of 1.5k. The typical value is 4.7k.

Q.– What are BE-BC capacitors in the SA605 oscillator transistor?

A. The oscillator is a transistor with the collector connected to the supply and the emitter connected to the ground through a 25k resistor. The base goes to the supply through an 18k resistor. The junction capacitors are roughly about 24fF (fempto Farads) for CJE (Base-emitter capacitors), and 44fF for CJC (Collector-base capacitors). There is a 72fF capacitor for CJS (Collector-substrate capacitor). This is all on the chip itself. It should be apparent that the parasitic packaging capacitors (1.5–2.5pF) are the dominant values in the oscillator design.

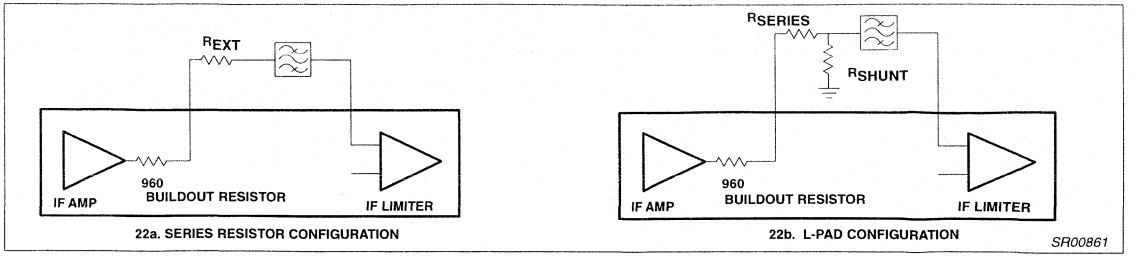


Figure 22. Implementing the 12dB Insertion Loss

Summary of Differences for SA604/604A

	SA604	SA604A
RSSI	No temperature compensation	Internally temperature compensated
IF Bandwidth	15MHz	25MHz
IF Limiter Output	No buffer	Emitter follower buffer output with 8k in the emitter
Current Drain	2.7mA	3.7mA

Q.– What are the differences between the SA604 and SA604A? (see Table below)

A. The SA604A is an improved version of the SA604. Customers, who have been using the SA604 in the past, should have no trouble doing the conversion.

The main differences are that the small signal IF bandwidth is 25MHz instead of 15MHz, and the RSSI is internally temperature compensated. If external temperature compensation was used for the SA604, the designer can now cut cost with the SA604A. The designer can either get rid of these extra parts completely or replace the thermistor (if used in original temperature compensated design) with a fixed resistor.

Those using the SA604 at 455kHz should not see any change in performance. For 10.7MHz , a couple of dB improvement in performance will be observed. However, there may be a few cases where instability will occur after using SA604A. This will be the case if the PC-board design was marginal for the SA604 in the first place. This problem, however, can be cured by using a larger than 10µF tantalum bypass capacitor on the supply line, and screening the capacitors for their ESR (equivalent series resistance) as mentioned earlier. The ESR at 455kHz should be less than 0.2Ω. Since ESR is a frequency dependent value, the designer can correlate good performance with a low frequency dissipation factor, or ESR measurement, and screen the tantalum capacitors in production. There are some minor differences as well. The SA604A uses about 1mA more current than the SA604. An emitter follower has been added at the limiter output to present a lower and more stable output impedance at Pin 9. The DC voltage at the audio and data outputs is approximately 3V instead of 2V in the SA604, but that should not cause any problems. The recovered audio level, on the other hand, is slightly higher in the SA604A which should actually be desirable. Because of these changes, it is now possible to design 21.4MHz IFs using the SA604A, which was not possible with the SA604.

The two chips are identical, otherwise. The customers are encouraged to switch to the SA604A because it is a more advanced bipolar process than the previous generation used in the SA604. As a result we get much tighter specifications on the SA604A.

Q.– How does the SA605 mixer compare with a typical double balanced diode mixer?

A. Some data on the comparison of the conversion gain and LO power requirements are shown in this application note. These two parameters reveal the advantages in using the SA605 mixer.

The only drawback of the SA605 may seem to be its lower third-order intercept point in comparison to a diode mixer. But, this is inherent in the SA605 as a result of the low power consumption. If one compares the conversion gain of the SA605 with the conversion loss of a low cost diode mixer, it turns out that the third-order intercept point, referred to the output, is the same or better in the SA605. Another point to take into account is that a diode mixer cannot be used in the front end of a receiver without a preamp due to its poor noise figure. A third-order intercept analysis shows that the intercept point of the combination of the diode mixer and preamp will be degraded at least by the gain of the preamp. A preamp may not be needed with SA605 because of its superior noise figure.

For more detailed discussion of this topic please refer to the paper titled "Gilbert-type Mixers vs. Diode Mixers").

Q.– How can we use the SA605 for SCA FM reception?

A. The 10.7MHz application circuit described in AN1993 can be used in this case. The LO frequency should be changed and the RF front-end should be tuned to the FM broadcast range. The normal FM signal, coming out of Pin 8 of the SA605, could be expected to have about 1.5µV (into 50Ω) sensitivity for 20dB S/N. This signal should be band-pass filtered and amplified to recover the SCA sub-carrier. The output of that should then go to a PLL SCA decoder, shown on the data sheet of Philips Semiconductors SA565 phase lock loop, to demodulate the base-band audio. The two outputs of the SA605 Pins 8 and 9 can be used to receive SCA data as well as voice, or features such as simultaneous reception of both normal FM, and SCA. The RSSI output, with its 90dB dynamic range, is useful for monitoring signal levels.

Q.– What is the power consumption of the SA605 or SA604A vs. temperature and V_{CC}?

A. The SA605 consumes about 5.6mA of current at 6V. This level is slightly temperature and voltage dependent as shown in Figure 33. Similar data for the SA604A is shown in Figure 34.

Q.– How can you minimize RF and LO feedthroughs

A. The RF and LO feedthroughs are due to offset voltages at the input of the mixer's differential amplifiers and the imbalance of the parasitic capacitors. A circuit, such as the one shown in Figure 35, can be used to adjust the balance of the differential amplifiers. The circuit connected to Pins 1 and 2 will minimize RF feedthrough while the circuit shown connected to Pin 6 will adjust the LO feedthrough. The only limitation is that if the RF and LO frequencies are in the 100MHz range or higher, these circuits will probably be effective for a narrow frequency range.

Q.– Distortion vs. RF input level. We get a good undistorted demodulated signal at low RF levels, but severe distortion at high RF levels. What is happening?

A. This problem usually occurs at 10.7MHz or at higher IF's. The IF filters have not been properly matched on both sides causing a sloping IF response. The resulting distortion can be minimized by adjusting the quad tank at the FM threshold where the IF is out of limiting. As the RF input increases, the IF stages will limit and make the IF response flat again. At this point, the effect of the bad setting of the quad tank will show itself as distortion. The solution is to always tune the quad tank for distortion at a medium RF level, to make sure that the IF is fully limited. Then, to avoid excessive distortion for low RF levels, one should make sure that the IF filters are properly matched.

Q.–The most commonly asked questions: "Why doesn't the receiver sensitivity meet the specifications?"; "Why is the RSSI dynamic range much less than expected?"; "Why does the RSSI curve dip at 0.9V and stay flat at 1V as the RF input decreases?"; "Why does the audio output suddenly burst into oscillation, or output wideband noise as the RF input goes down, instead of dying down slowly?"; "When looking at the IF output with a spectrum analyzer, why do high amplitude spurs become visible near the edge of the IF band as the RF level drops?"

A. These are the most widely observed problems with the SA605. They are all symptoms of the same problem; instability. The instability is due to bad layout and grounding.

Regenerative instability occurs when the limiter's output signals are radiated and picked up by the high impedance inputs of the mixer and IF amp. This signal is amplified by both the IF amp and limiter. Positive feedback causes the signal to grow until the signal at the limiter's output becomes limited. Due to the nature of FM, this instability will dominate any low RF input levels and capture the receiver (see Figure 23).

Since the receiver behaves normally for high RF inputs, it misleads the designer into believing that the design is okay. Additionally the RSSI circuit cannot determine whether the signal being received is coming from the antenna or the result of regenerative instability. Therefore, RSSI will be a good instability indicator in this instance because the RSSI will stay at a high level when the received signal decreases. Looking at the IF spectrum (Pin 11 for 605, Pin 9 for 604A) with the RF carrier present (no modulation), the user will see a shape as shown below. When regenerative instability occurs, the receiver does not seem to have the ultimate sensitivity of which it is capable.

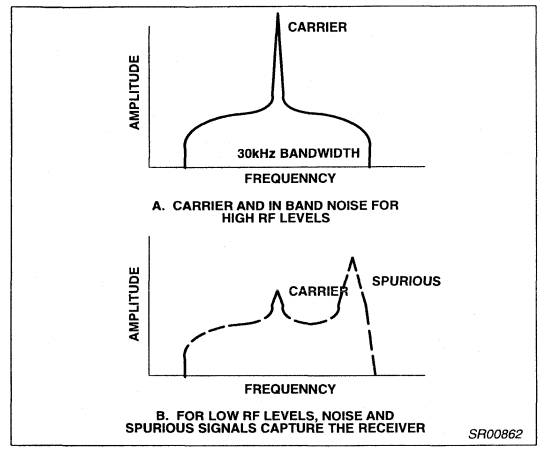


Figure 23.

Make sure that a double sided layout with a good ground plane on both sides is used. This will have RF/IF loops on both sides of the board. Follow our layouts as faithfully as you can. The supply bypass should have a low ESR 10–15μF tantalum capacitor as discussed earlier. The crystal package, the inductors, and the quad tank shields should be grounded. The RSSI output should be used as a progress monitor even if is not needed as an output. The lowest RSSI level should decrease as the circuit is made more stable. The overall gain should be reduced by lowering the input impedance of the IF amplifier and IF limiter, and adding attenuation after the IF amplifier, and before the 2nd filter. A circuit that shows an RSSI of 250mV or less with no RF input should be considered close to the limit of the performance of the device. If the RSSI still remains above 250mV, the recommendations mentioned above should be revisited.

Q.– Without the de-emphasis network at the audio output, the –3dB bandwidth of the audio output is limited to only 4.5kHz. The maximum frequency deviation is 8kHz, and the IF bandwidth is 25kHz. What is the problem?

A. What is limiting the audio bandwidth in this case is not the output circuit, but the IF filters. Remember that Carson's rule for FM IF bandwidth requires the IF bandwidth to be at least:

2(Max frequency Dev. + Audio frequency)

With a 25kHz IF bandwidth and 8kHz frequency deviation, the maximum frequency that can pass without distortion is approximately 4.5kHz. 2(8kHz + 4.5kHz) is 25kHz as expected.

Q.–What are the equivalent RF input impedances for the SA606 given the equivalent circuit model of Figure 4.

A. The SA606 input impedance vs. frequency is . . .

FREQ	RIIC
10MHZ	7.5KΩII2.4pF
50MHZ	7.5KΩII2.7pF
100MHZ	6.25KΩII2.7pF
150MHZ	5.5KΩII2.7pF
200MHz	5.0KΩII2.8pF

The input matching technique discussed in this note is applicable for the SA606.

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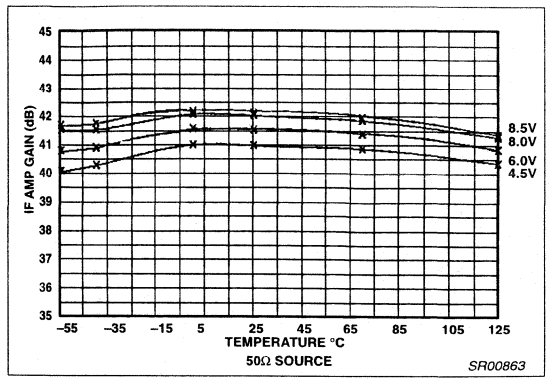


Figure 24. IF Amplifier Gain

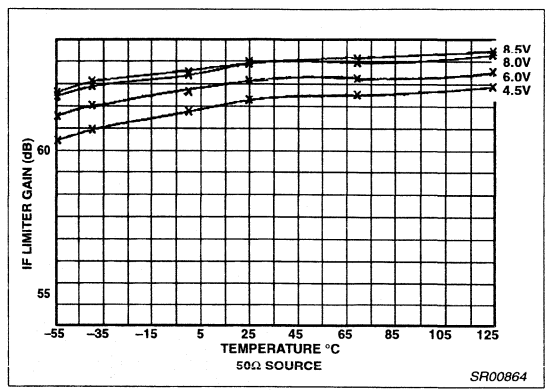


Figure 25. IF Limiter Gain

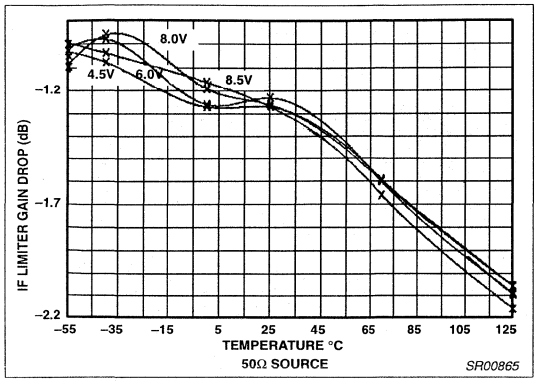


Figure 26. IF Amplifier Gain Drop, 20MHz Response

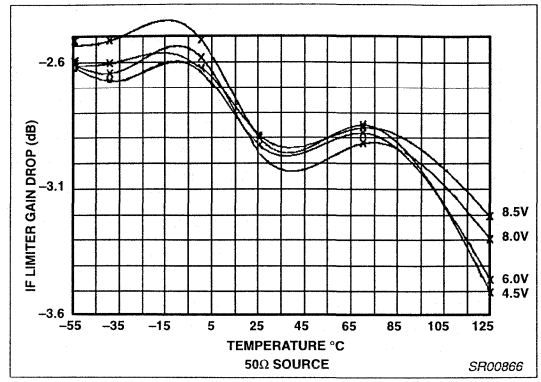


Figure 27. IF Limiter Drop, 20MHz Response

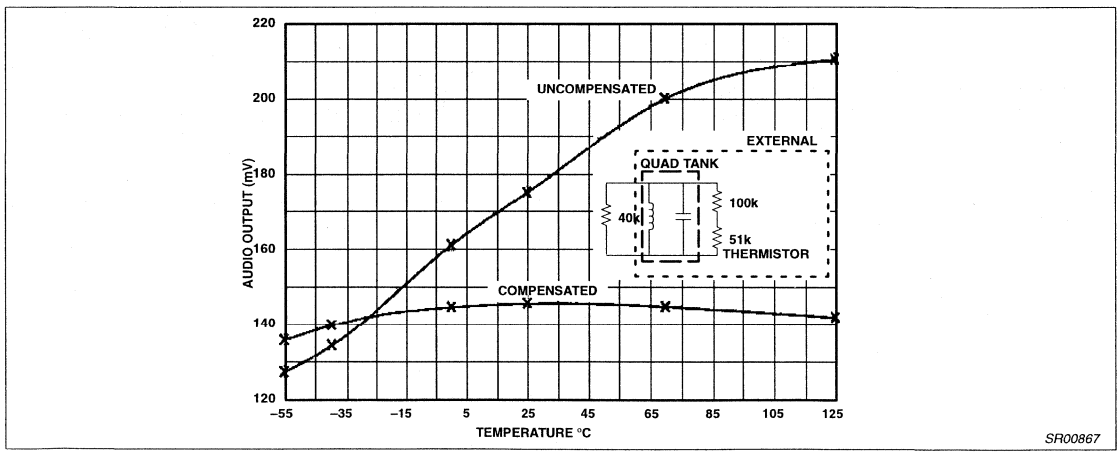


Figure 28. Audio Output: Compensated vs Uncompensated

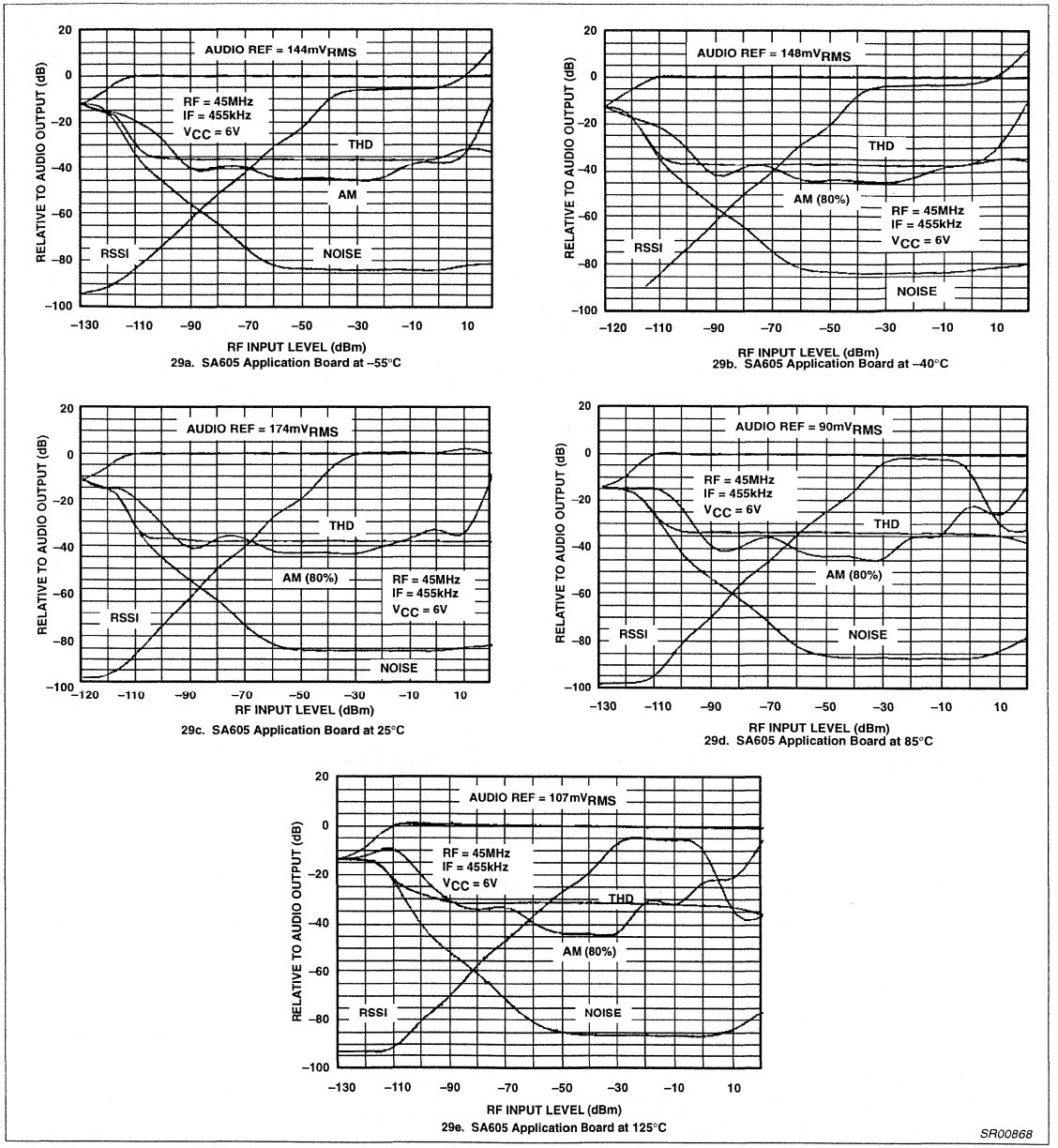
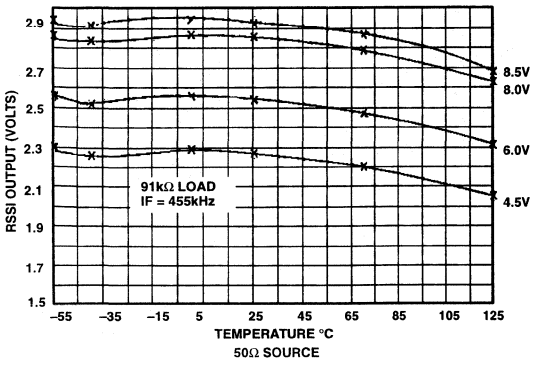
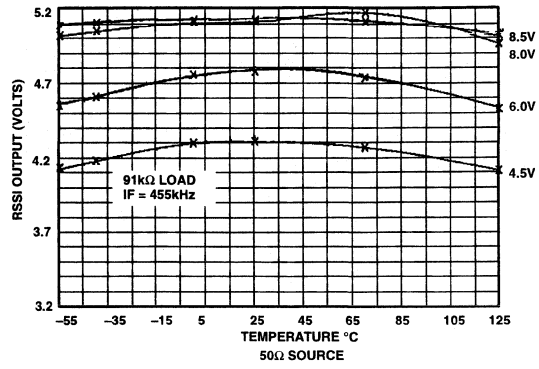


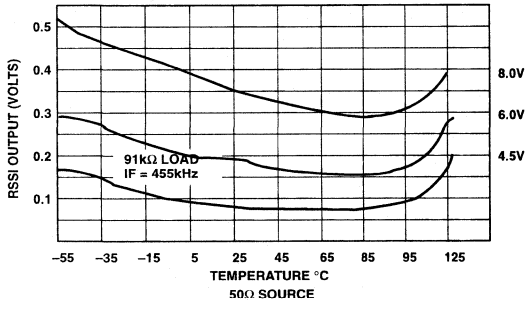
Figure 29. Performance of the SA605 Application Board at Different Temperatures



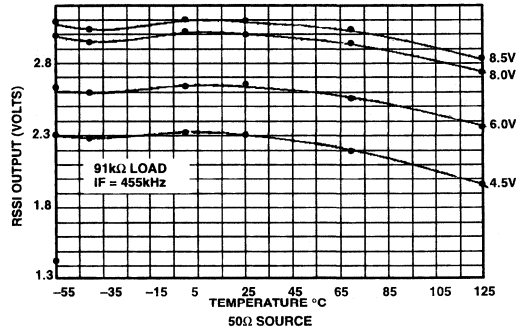
30a. SA604A for –68dBm, RSSI Output



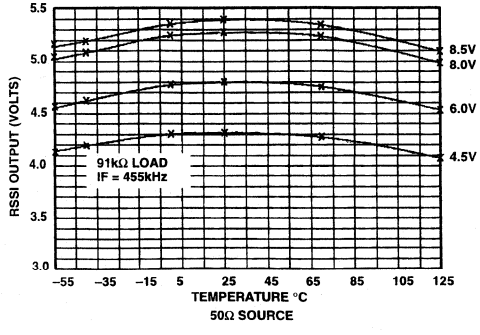
30b. SA604A for –18dBm, RSSI Output



30c. SA605 RSSI at –120dBm



30d. SA605 RSSI, –76dBm



30e. SA605 RSSI at –28dBm

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Figure 30. RSSI Response for Different Inputs

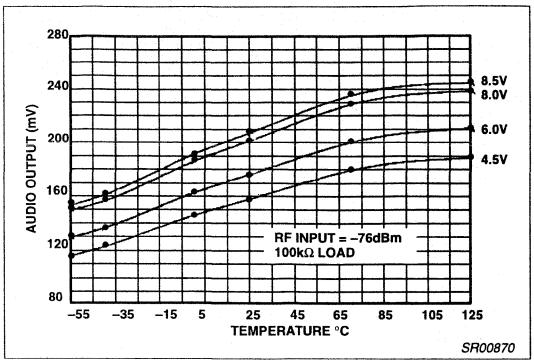


Figure 31. Audio Level vs Temperature and Supply Voltage

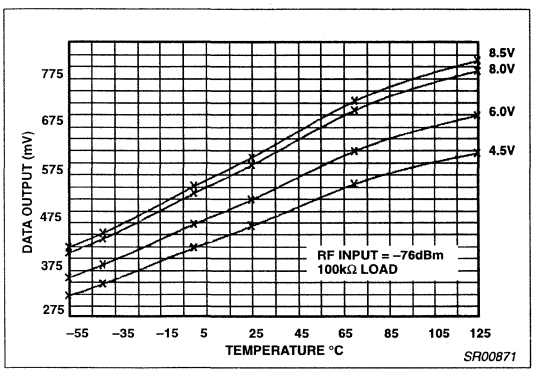


Figure 32. Data Level vs Temperature and Supply Voltage

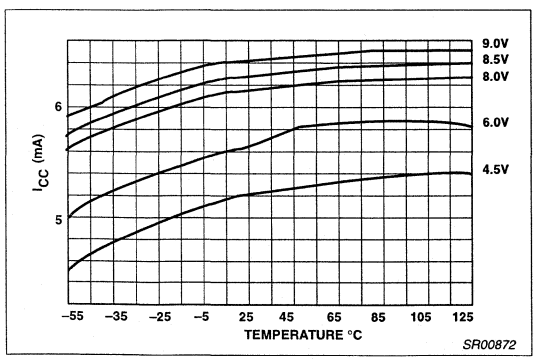


Figure 33. SA605 I_{CC} vs Temperature

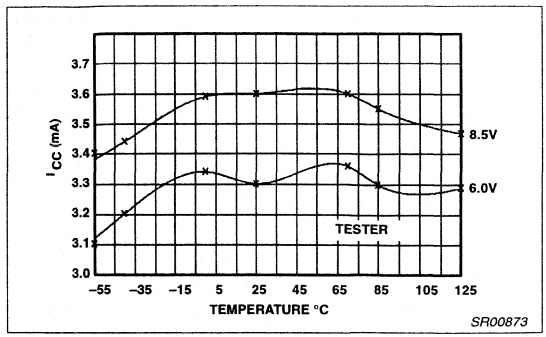


Figure 34. SA604A I_{CC} vs Temperature

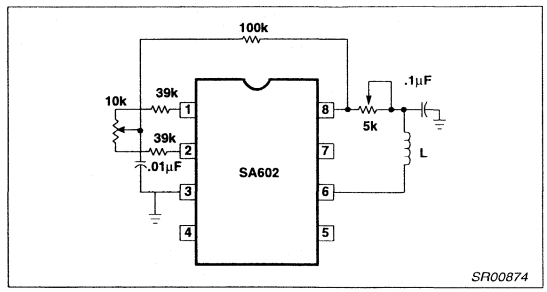
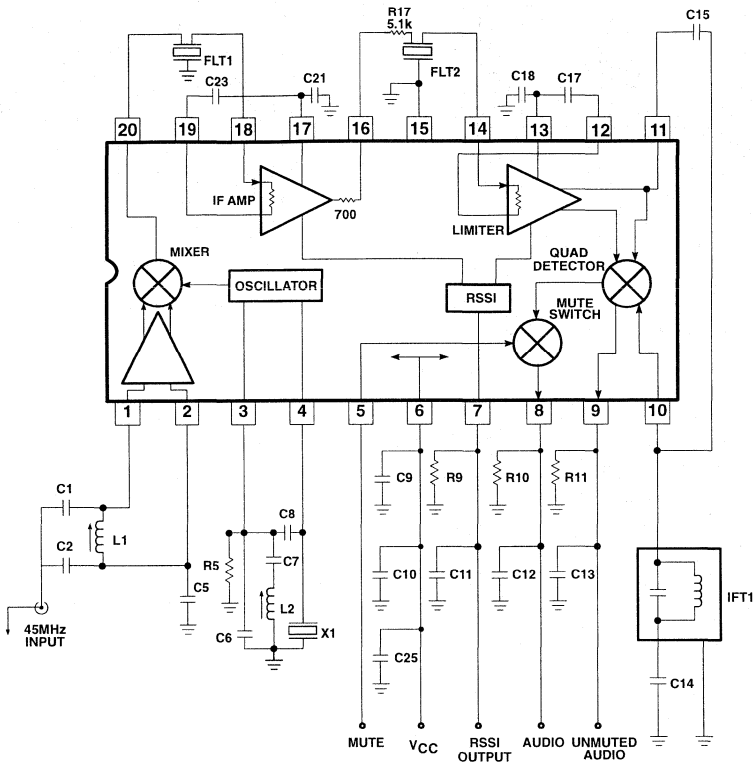


Figure 35. Minimizing RF and LO Feedthrough



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	3.3μH nominal Toko 292CNS–T1046Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

* NOTE: This value can be reduced when a battery is the power source.

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Figure 36. SA605 45MHz Application Circuit

Table 1. Related Application Notes

App. Note	Date	Title	Main Topics
AN198	Feb. 1987	Designing with the SA602	– Advantages/Disadvantages to single-ended or balanced matching
AN1981	Dec. 1988	New Low Power Single Sideband Circuits	– General discussion on SSB circuits – Audio processing – Phasing-filter technique
AN1982	Dec. 1988	Applying the Oscillator of the SA602 in Low Mixer Applications	– Oscillator configurations
AN199	Feb. 1987	Designing with the SA604	Circuits of: – AM synchronous det. – Temp. compensated RSSI circuit – Field strength meter – Product detector
AN1991	Dec. 1988	Audio Decibel Level Detector with Meter Driver	– Uses of the 604 in application
AN1993	Dec. 1988	High Sensitivity Application Low-Power RF/IF Integrated Circuits	– An overview of the SA602 and SA604 in typical applications – Good information before getting started

Table 2. Comparing Balanced vs Unbalanced Matching

SA605 or SA602	Matching	Advantages	Disadvantages
Pins 1 and 2 (RF input)	Single-ended (unbalanced)	– Very simple circuit – No sacrifice in 3rd-order performance	– Increase in 2nd-order products
	Balanced	– Reduce 2nd-order products	– Impedance match difficult to achieve

Table 3. LO Configurations

LO (MHz)	Suggested Configuration Using On-board Oscillator
0 - 30	Fundamental mode, use Colpitts
30 - 70	3rd overtone mode, use Colpitts
70 - 90	3-5th overtone mode, use Colpitts with 22kΩ resistor connected from the emitter pin to ground
90 - 170	Use Butler, crystal in series mode, and a 22kΩ resistor connected from the emitter pin to ground
170 - 300	LC configuration

Evaluating the SA605 SO and SSOP demo-board AN1995

Author: Alvin K. Wong

INTRODUCTION

With the increasing demand for smaller and lighter equipment, designers are forced to reduce the physical size of their systems. There are several approaches to solving the size problem. A designer needs to look for sophisticated integrated single chip solutions, chips that are smaller in size, and chips that require minimum external components.

Philips Semiconductors offers all of these solutions in their SA605. The SA605 single-chip receiver converts the RF signal to audio and is available in three packages: DIP,SO, and SSOP. This offers total flexibility for layout considerations. The SSOP package is the smallest 20 pin package available in the market today, and allows the designer the flexibility to reduce the overall size of a layout.

When working with a smaller and tighter layout in a receiver design, it becomes important to follow good RF techniques. This application note shows the techniques used in the SO and SSOP demo-board. It does not cover the basic functionality of the SA605 but instead focuses more on the layout constraints. This application note also has a trouble-shooting chart to aid the designer in evaluating the SO and SSOP demo-board. For a complete explanation of the SA605, please refer to application note AN1994 which describes the basic block diagrams, reviews the common problems encountered with the SA605, and suggests solutions to them. Reading AN1994 is highly recommended before attempting the SO and SSOP layout.

The recommended layout demonstrates how well the chip can perform. But it should be pointed out that the combination of external parts with their tolerances plays a role in achieving maximum sensitivity.

The minimum and maximum 12dB SINAD measurement for both boards is -118dBm and -119.7dBm, respectively. A typical reading taken in the lab for both SO and SSOP demo-boards is -119dBm.

There were two different design approaches for both layouts. For the SO layout, there are inductive tuning elements (except for the LO section); for the SSOP layout there are capacitive tuning elements. This approach was taken to show the designer that both ways can be used to achieve the same 12dB SINAD measurement. However, it is worth mentioning that capacitive tuning elements are less expensive than the inductive tuning elements.

Packages Available

As mentioned above, there are three packages available for the SA605. See the "Package Outline" section of the Philips Semiconductors 1992 RF Handbook for the physical dimensions of all three packages. Notice that the DIP package is the largest of the three in physical size; the SSOP is the smallest. The recommended layout and performance graphs for the DIP package are shown in the SA605 data sheet and AN1994. But the SO and SSOP recommended layout and performance graphs are shown in this application note.

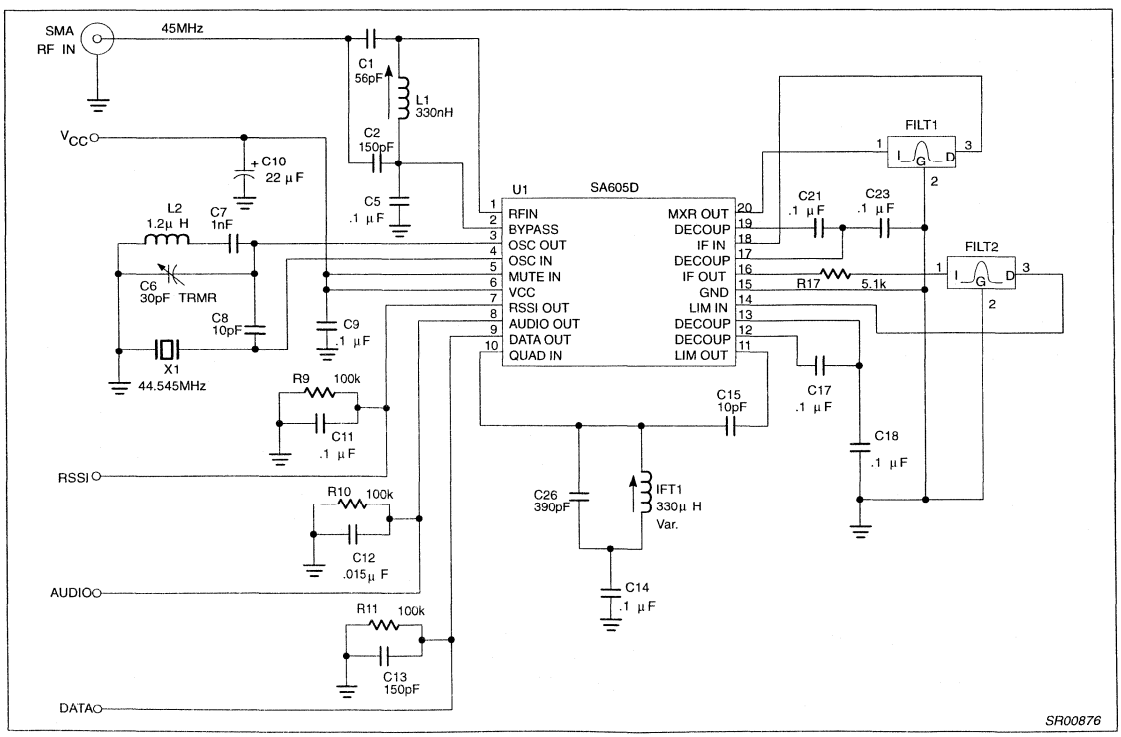


Figure 1. SA605 Schematic for the SO Layout

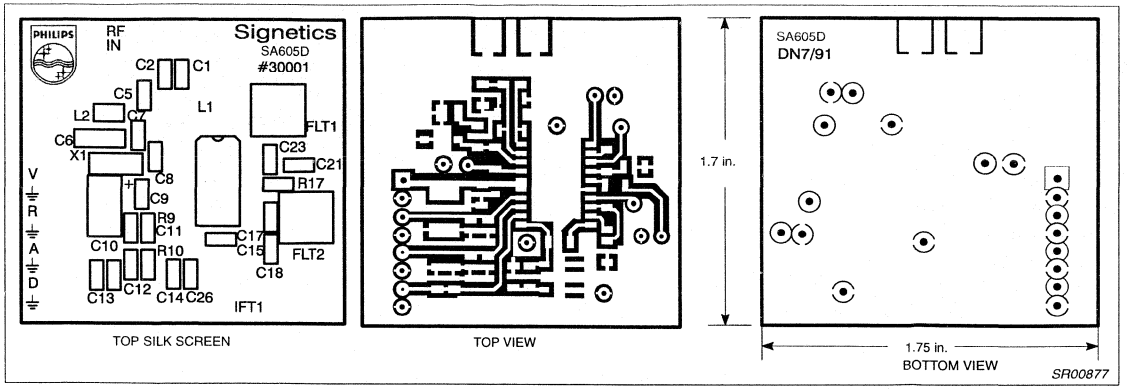


Figure 2. SA605 SO Demo-board Layout (Not Actual Size)

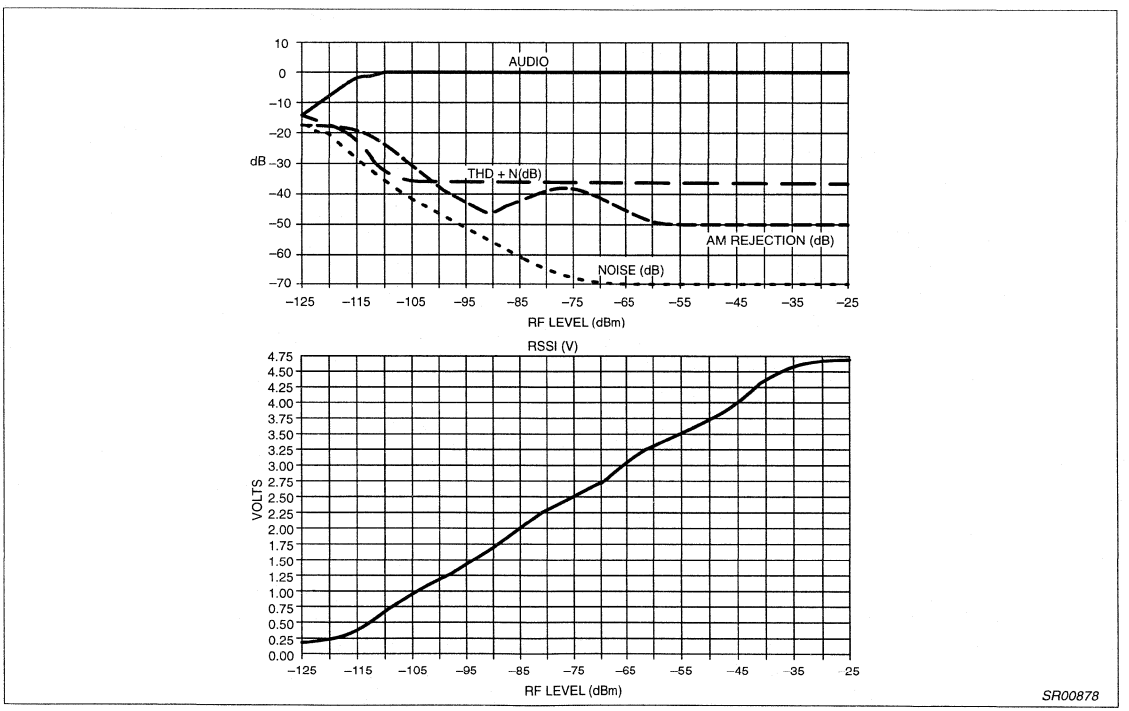


Figure 3. SA605 SO Performance Curves

SO LAYOUT:

Figure 1 shows the schematic for the SO layout. Listed below are the basic functions of each external component for Figure 1.

C1 – Part of the tapped-C network to match the front-end

C2 – Part of the tapped-C network to match the front-end

C5 – Used as an AC short to Pin 2

C6 – Used to tune the LO for the Colpitts oscillator

C7 – Used as part of the Colpitts oscillator

C8 – Used as part of the Colpitts oscillator

C9 – Supply bypassing

C10 – Supply bypassing

C11 – Used as filter

C12 – Used as filter

C13 – Used as filter
C14 – Used to AC ground the Quad tank
C15 – Used to provide the 90° phase shift to the phase detector
C17 – IF limiter decoupling cap
C18 – IF limiter decoupling cap
C21 – IF amp decoupling cap
C23 – IF amp decoupling cap
C26 – Quad tank component
L1 – Part of tapped-C network to match the front-end TOKO 5CB-1320Z
L2 – Part of the Colpitts oscillator Coilcraft 1008CS-122
R9 – Used to convert the current into the RSSI voltage
R10 – Converts the audio current to a voltage
R11 – Converts the data current to a voltage
R17 – Used to achieve the –12dB insertion loss
IFT1 – Inductor for the Quad tank TOKO 303LN-1130
FILT1 – Murata SFG455A3 455kHz bandpass filter
FILT2 – Murata SFG455A3 455kHz bandpass filter
X1 – Standard 44.545MHz crystal in QC38 package

The recommended SO layout can be found in Figure 2 and should be used as an example to help designers get started with their projects.

The SO SA605 board performance graphs can be found in Figure 3.

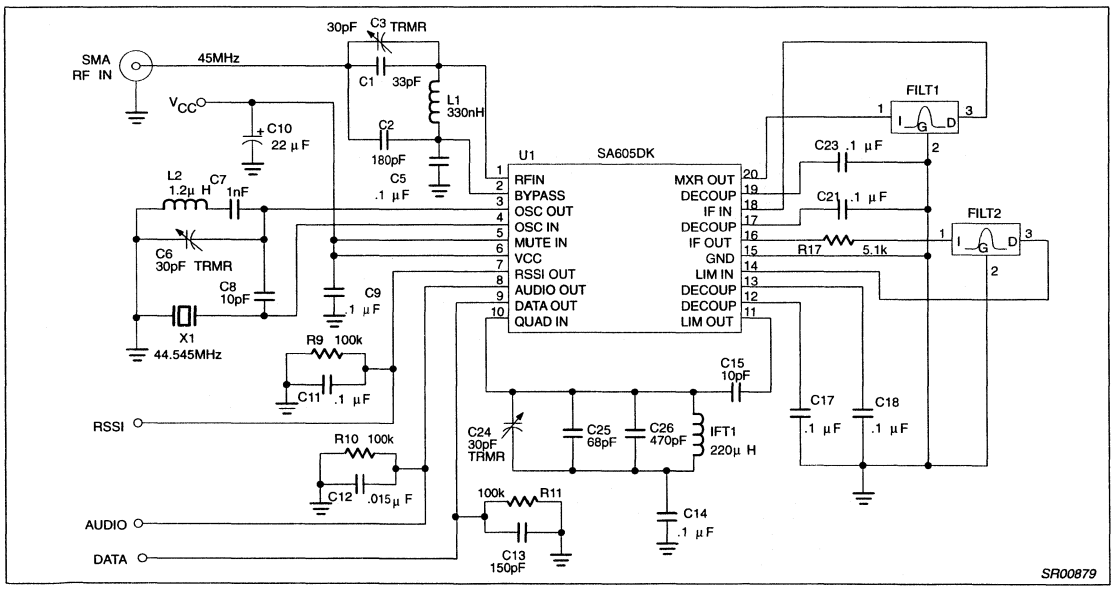


Figure 4. SA605 Schematic for the SSOP Layout

SSOP LAYOUT:

Figure 4 shows the schematic for the SSOP layout.

C1 – Part of the tapped-C network to match the front-end
C2 – Part of the tapped-C network to match the front-end
C3 – Part of the tapped-C network to match the front-end
C5 – Used as an AC short to Pin 2
C6 – Used to tune the LO for the Colpitts oscillator
C7 – Used as part of the Colpitts oscillator
C8 – Used as part of the Colpitts oscillator
C9 – Supply bypassing
C10 – Supply bypassing
C11 – Used as filter
C12 – Used as filter
C13 – Used as filter
C14 – Used to AC ground the Quad tank
C15 – Used to provide the 90° phase shift to the phase detector
C17 – IF limiter decoupling cap
C18 – IF limiter decoupling cap
C21 – IF amp decoupling cap
C23 – IF amp decoupling cap
C24 – Part of the Quad tank
C25 – Part of the Quad tank
C26 – Part of the Quad tank
L1 – Part of tapped-C network to match the front-end Coilcraft 1008CS-331
L2 – Part of the Colpitts oscillator Coilcraft 1008CS-122
R9 – Used to convert the current into the RSSI voltage
R10 – Converts the audio current to a voltage

R11 – Converts the data current to a voltage

R17 – Used to achieve the –12dB insertion loss

IFT1 – Inductor for the Quad tank Mouser ME435-2200

FILT1 – Murata SFGCC455BX 455kHz bandpass filter

FILT2 – Murata SFGCC455BX 455kHz bandpass filter

X1 – Standard 44.545MHz crystal

The SSOP layout can be found in Figure 5. The SSOP SA605 board performance graphs can be found in Figure 6.

The main difference between the SO and SSOP demo-boards is that the SSOP demo-board incorporates the low profile 455kHz Murata ceramic filter. It has an input and output impedance of 1.0kΩ. This presents a mismatch to our chips, but we have found that the overall performance is similar to that when we use the "blue" Murata filters that have the proper 1.5kΩ input and output impedance.

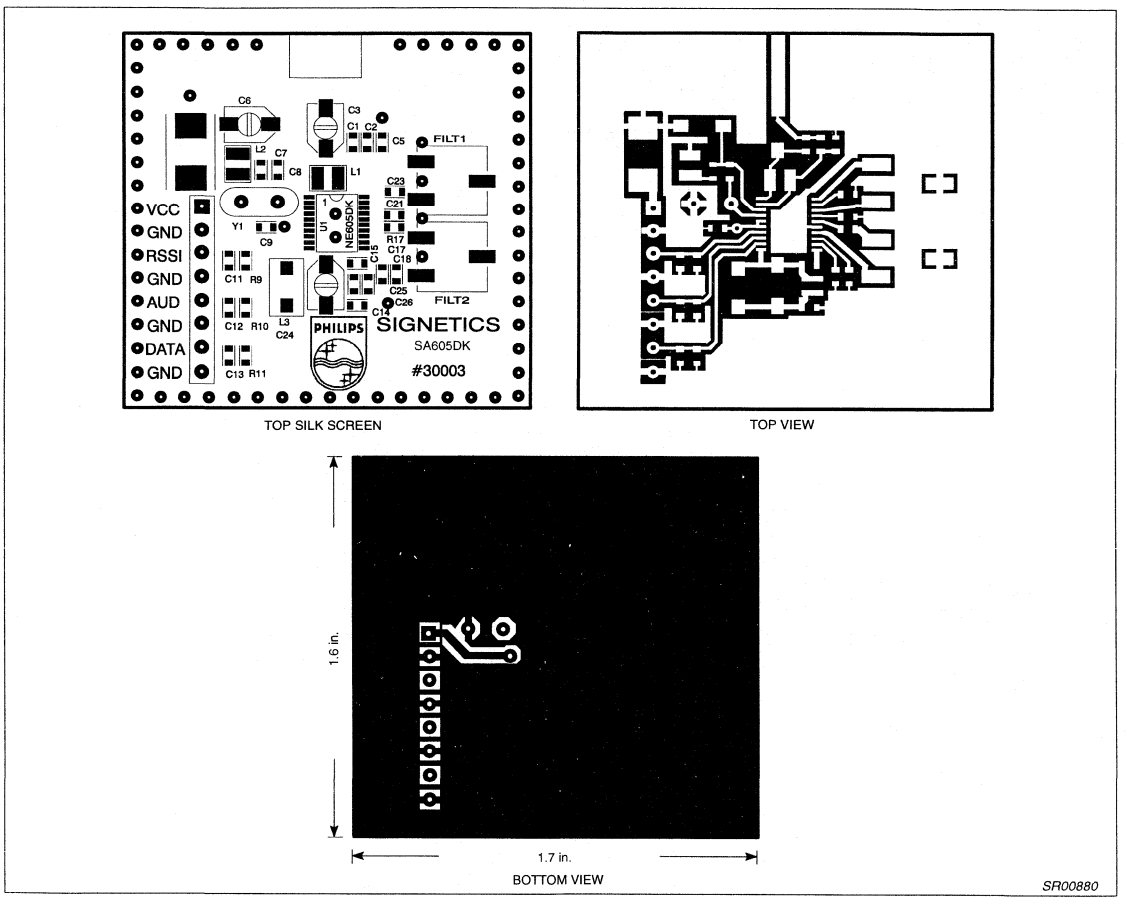


Figure 5. SA605 SSOP Demo-board Layout (Not Actual Size)

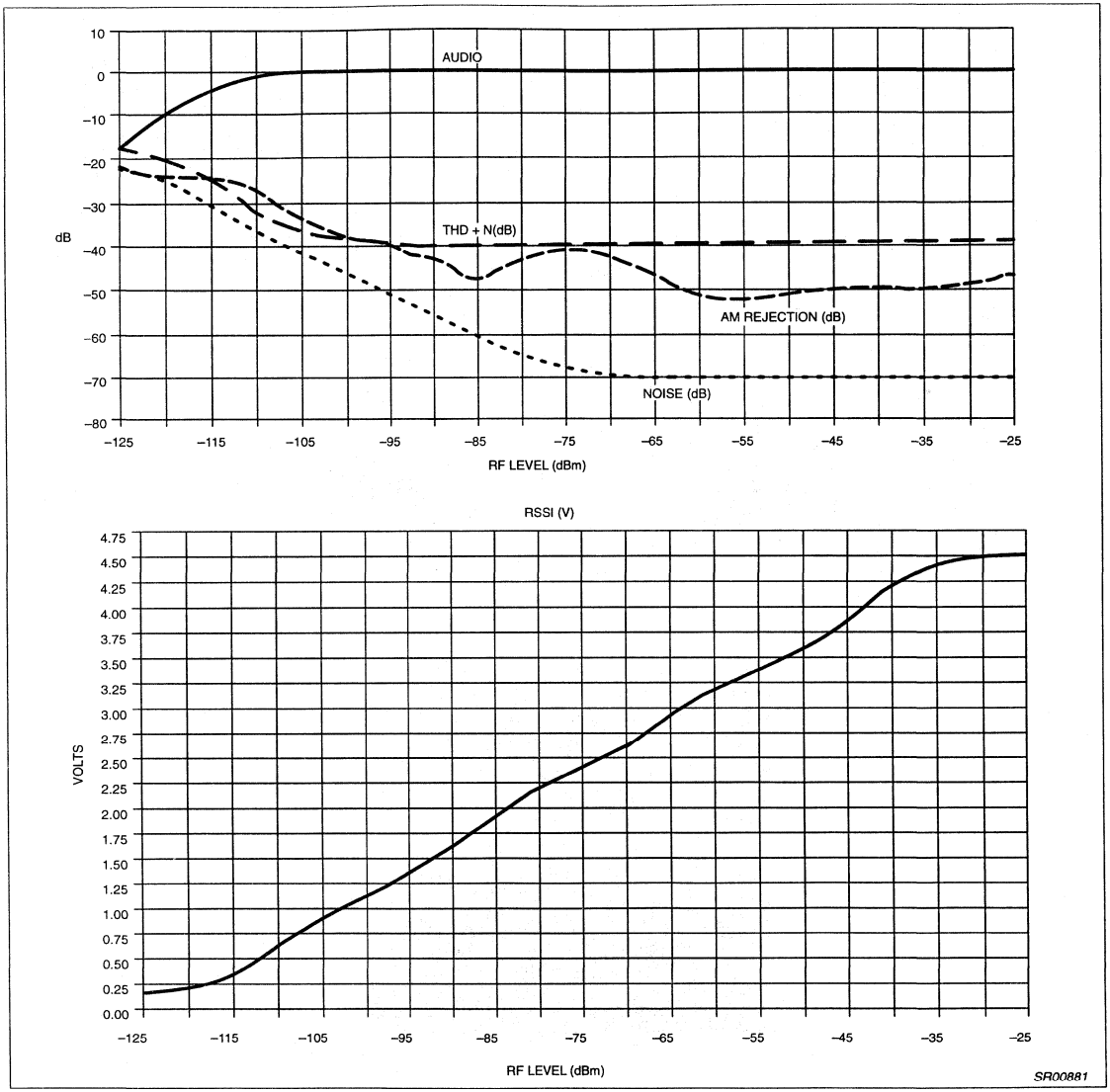


Figure 6. SA605 SSOP Performance Graphs

HOW TO TUNE THE SA605 DEMO-BOARD

Figure 7 shows a trouble-shooting chart for the SA605. It can be used as a general guide to tune the DIP, SO, and SSOP demo-boards. Below are some of the highlights from the trouble shooting chart that are explained in more detail.

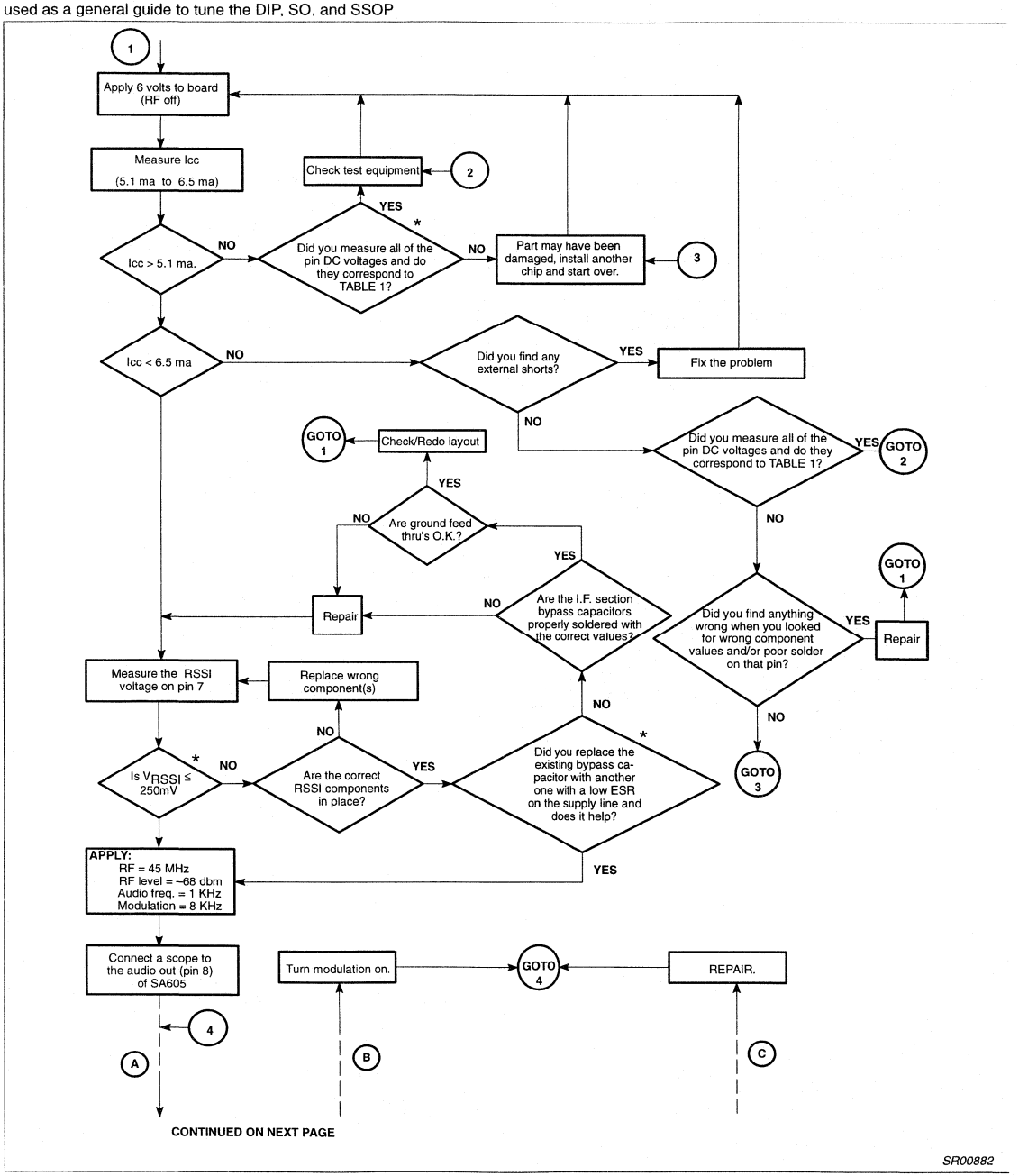
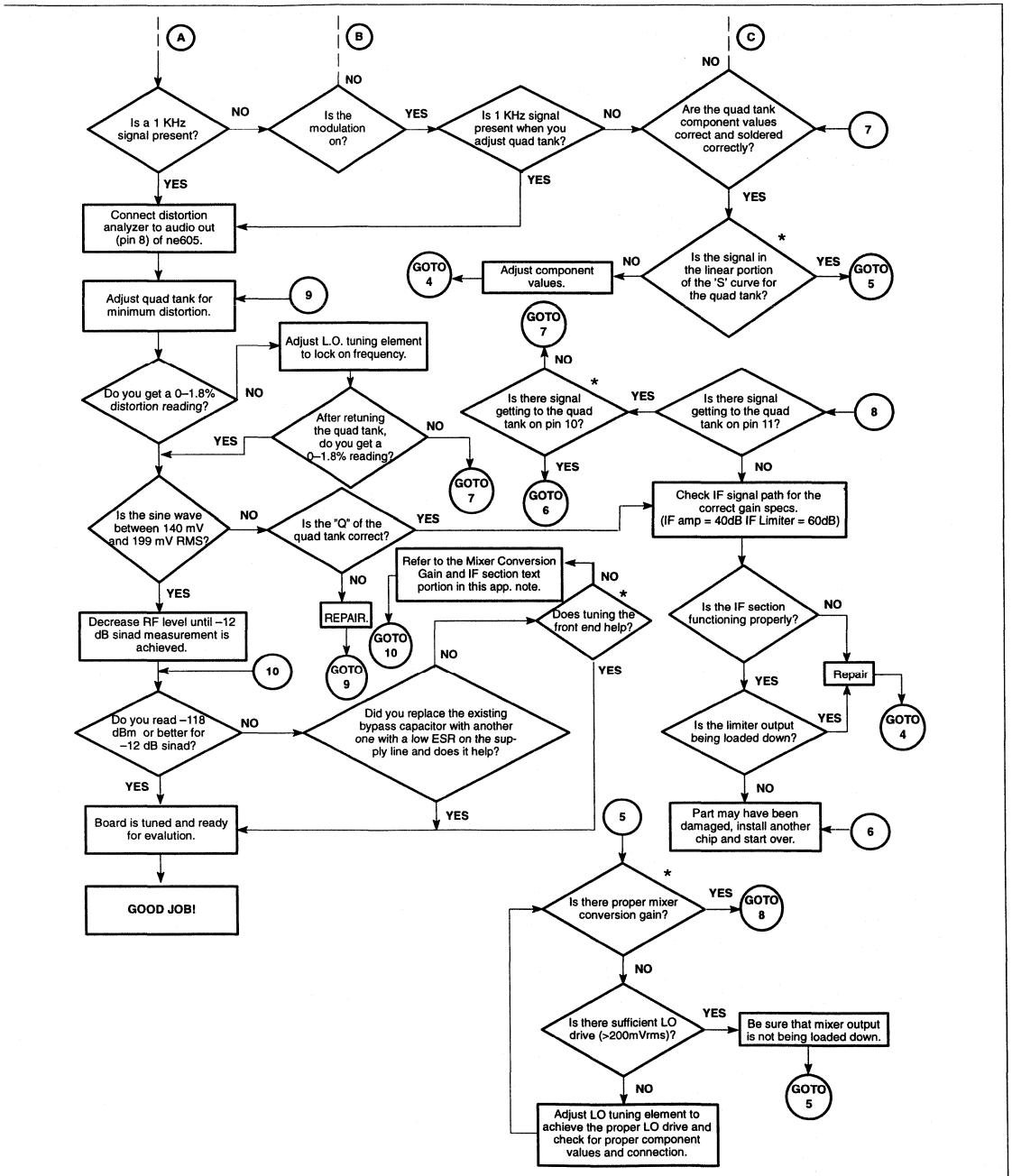


Figure 7. Trouble-shooting Chart for the SA605 Demo-board

Evaluating the SA605 SO and SSOP demo-board AN1995



*NOTE: Refer to the appropriate text section of the app. note for further details.

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Evaluating the SA605 SO and SSOP demo-board AN1995

How to tell when a part is damaged

Since most SO and SSOP sockets hinder the maximum performance of the SA605, it is advisable to solder the packages directly to the board. By this approach, one will be able to evaluate the part correctly. However, it can be a tedious chore to switch to another part using the same layout. Therefore, to be absolutely certain that the chip is damaged, one can measure the DC voltages on the SA605. Table 9 shows the DC voltages that each pin should roughly have to be a good part.

Table 9. Approximate DC Voltages for the SA605

Pin Number	DC Voltage (V)
1	1.37
2	1.37
3	5.16
4	5.94
5	N/A
6	6.00 (V_{CC})
7	N/A
8	2.00
9	2.00
10	3.49
11	1.59
12	1.59
13	1.59
14	1.65
15	0.00 (GND)
16	1.60
17	1.60
18	1.60
19	1.60
20	4.87

Note: The DC voltage on Pin 5 is not specified because it can either be V_{CC} or ground depending if the audio is muted or not (Connecting ground on Pin 5 mutes the audio on Pin 8, while V_{CC} on Pin 5 unmutes the audio).

The DC voltage on Pin 7 is not specified because its DC voltage depends on the strength of the RF signal getting to the input of the SA605. It also can be used as a stability indicator.

If any of the DC voltages are way off in value, and you have followed the trouble-shooting chart, the part needs to be changed.

RSSI Indicator

The next important highlight is using the RSSI pin as a stability indicator. With power connected to the part and no RF signal applied to the input, the DC voltage should read 250mV or less on Pin 7. Any reading higher than 250mV, indicates a regeneration problem. To correct for the regeneration problem, one should check for poor layout, poor bypassing, and/or poor solder joints. Bypassing the SA605 supply line with a low equivalent series resistance (ESR) capacitor to reduce the RSSI reading can improve the 12dB SINAD measurement by 8dB, as found in the lab. If the regeneration problem still exists, read AN1994.

Quad tank and S-Curve

As briefly mentioned in the chart, it is important to measure the Q of the quad tank if a distortion reading of 1.8% or less cannot be measured. Recall that if the Q of the quad tank is too high for the deviation, then premature distortion will occur. However, if the Q is too low for the deviation, the audio level will be too low. The audio level coming out of the audio pin should be 140mV$_{RMS}$ to 190mV$_{RMS}$.

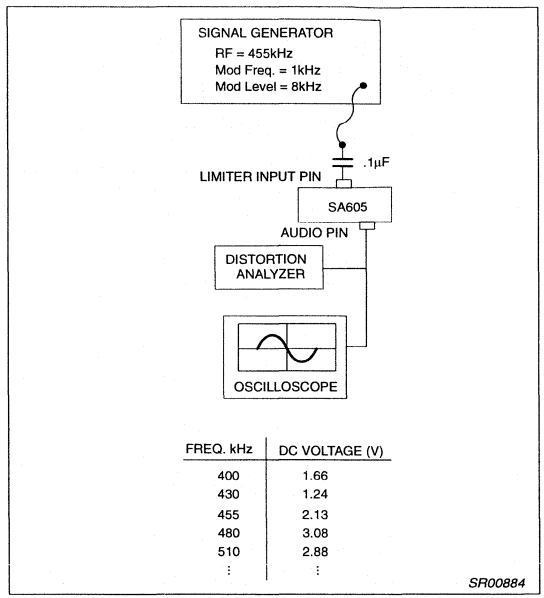

Figure 8. Test Set-up to Measure S-Curve of the Quad Tank

If the distortion reading is too high and/or the audio level is too low, then it is important to measure and plot the S-curve of the quad tank. The test set-up used in the lab can be seen in Figure 8.

The following steps were taken to measure the S-curve for the SO and SSOP demo-boards.

Step 1. Remove the second IF ceramic filter from the demo-board.

Step 2. Connect a signal generator to the limiters input through a DC blocking capacitor.

Step 3. Connect a DC voltmeter and an oscilloscope to the audio output pin.

Step 4. Set the signal generator to a 455kHz signal and be sure that the modulation is on (RF=455kHz Mod Freq = 1kHz Mod Level=8kHz). Apply this 455Khz signal to the limiter input such that there is a sinewave on the oscilloscope screen. Adjust the quad tank for maximum sinewave amplitude on the oscilloscope or for lowest distortion. Additionally, adjust the supply input signal to the SA605 such that the 1kHz sinewave reaches its maximum amplitude.

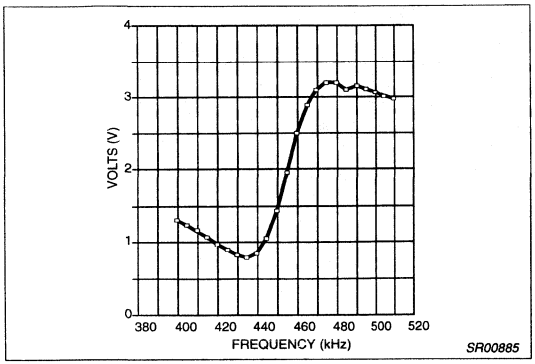

Figure 9. S-Curve for SA605 SO Demo-board

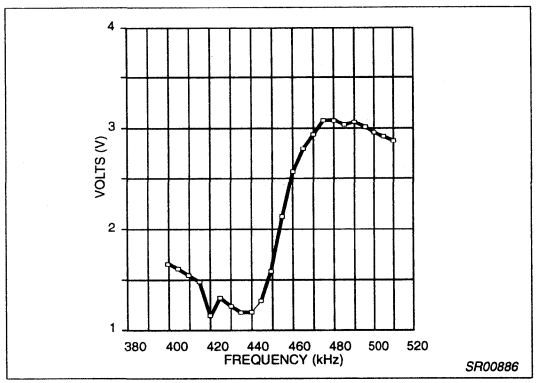

Figure 10. S-Curve for SA605 SSOP Demo-board

Step 5. Turn off the modulation and start taking data. Measure the Frequency vs DC voltage. Vary the frequency incrementally and measure the DC voltage coming out of the audio pin. Remember that once the modulation is turned off, the sine-wave will disappear from the oscilloscope screen.

Step 6. Plot the S-curve.

Figures 9 and 10 show the S-curve measurements for the SO and SSOP demo-boards. Notice that the center of the S-curve is at 455kHz. The overall linearity determines how much deviation is allowed before premature distortion. Since our application requires ±8kHz of deviation, our S-curve is good because it exceeds the linear range of 447kHz to 463kHz.

If the Q of the quad tank needs to be lowered, a designer should put a resistor in parallel with the inductor. The lower the resistor value, the more the Q will be lowered. If the Q needs to be increased, choose a higher Q component. More information on the Quad tank can be found in the SA604A data sheet.

If the linear section of the S-curve is not centered at 455kHz, the quad tank component values need to be recalculated. The way to determine the component values is by using $F + \frac{1}{2\pi\sqrt{LC}}$ where F should be the IF frequency. In the case of the demo-boards, the IF = 455kHz.

Front End Tuning

The best way to tell if the front end of the SA605 is properly matched is to use a network analyzer in a S11 setting. The lower the dip, the greater the absorption of the wanted frequency. Figures 11 and 12 show the S11 dip for the front end matching of the SO and SSOP demo-boards, respectively.

We have found in the lab that a -8dB to -10dB dip is usually sufficient to get the maximum signal transfer such that a good 12dB SINAD reading is met. The front end circuit uses a tapped-C impedance transformation circuit which matches the 50Ω source with the input impedance of the mixer.

In the process of matching the front end, we have found that the ratio of the two capacitors play an important role in transferring the signal from the source to the mixer input. There should be approximately a 4:1 or 5:1 ratio.

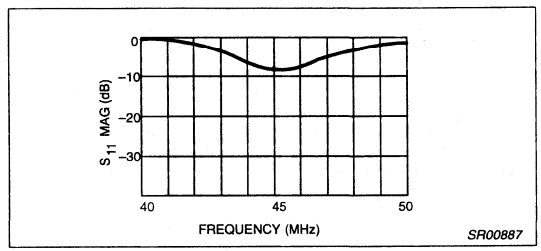

Figure 11. S11 Front-End Response for SO Demo-board

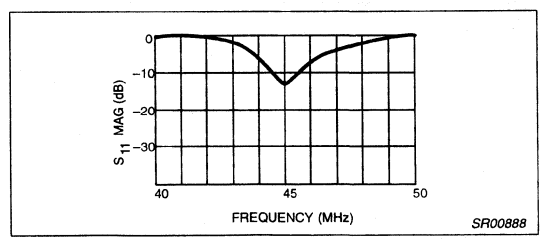

Figure 12. S11 Front-End Response for SSOP Demo-board

Checking the Conversion Gain of the Mixer

Once the front end has been properly matched, a designer should check the conversion gain if there are problems with the SINAD measurement. Be sure to turn off the modulation when making this measurement.

The method of measuring conversion gain on the bench is fairly simple. For our demo-boards, measure the strength of the 455kHz signal on the matching output network of the mixer with a FET probe. Then measure the 45MHz RF input signal on the matching input network of the mixer. Subtract the two numbers and the measured conversion gain should be around 13dB. Make sure that the input and output matching networks for the mixer have the same impedance since we are measuring voltage gain to get power gain ($P = V^2/R$). Of course this conversion gain value will change if there is a different RF input. In AN1994, Figure 16 shows how the conversion gain varies with different RF input frequencies.

Evaluating the SA605 SO and SSOP demo-board AN1995

Checking the gains in the IF Section

If the IF section does not give 100dB of gain, then the -118dBm SINAD measurement cannot be achieved. In fact some symptoms of low or no audio level can be due to the IF section.

One way of checking the function of the IF section is to check the gain of the IF amplifier and the IF limiter. The IF amplifier gain should be around 40dB and the IF limiter gain should be around 60dB.

To check this, connect a FET probe to the output of the amplifier. Apply a strong input signal with no modulation and then slowly lower the input signal and wait for the output of the amplifier to decrease. Measure the strength of the output signal in dB and then subtract from it the strength of the input signal in dB. This resulting number indicates the maximum gain of that section. (This method assumes matched input and output impedance.)

If a designer finds one of the sections with lower gain, then one area to check are the IF bypass capacitors. Be sure that the IF bypass capacitors have a good solid connection to the pad. It was also found in the lab that the RSSI stability reading improves when the IF bypass is properly installed.

QUESTION & ANSWER SECTION

Q: When I measure the bandpass response of the IF filters on the SSOP demo-board, it appears to have a little hump compared to the SO demo-board which has a flat filter response. Why is there a difference in the bandpass response when the SO and SSOP 605 chips are similar?

A: The answer has to do with the ceramic filters and not the package of the SA605. The reason why the SO demo-board has a flat bandpass response is because it is matched properly with the filter. The SSOP demo board uses the new Murata low profile ceramic 455kHz filter. Unfortunately, the input and output impedance is now 1kΩ instead of 1.5kΩ. This presents an impedance mismatch which creates the hump to occur in the bandpass response. But one does not have to worry too much about this response because the situation does not affect the overall performance that much. Additionally, the 12 SINAD measurement is similar whether using the "blue" (1.5kΩ) or "white" (1.0kΩ) Murata filters.

If you are worried about this, then switch to the correct "blue" Murata filters. The SSOP package will work with those filters as well. But if your design has strict height requirements, the white filters are a good solution.

Q: How much LO signal do you see at the RF port?

A: The worst LO leakage seen at the RF input on the SO and SSOP demo-board is -40dBm/441mV. This seems to vary with the LO level into the base of the on board transistor. This measurement will also vary with different LO frequencies. The SA605 SO and SSOP demo-boards have a LO frequency of 44.545MHz. Since there are so many variables, a designer needs to measure his/her own board for an accurate LO-RF isolation measurement.

There are several ways to improve the LO leakage from getting to the antenna. One can choose a higher IF frequency and tighten up the bandwidth of the front-end filter. Another solution is to add a low noise amplifier between the antenna and the mixer, and/or design a double conversion receiver and make sure the 1st mixer has a LO-RF isolation which meets the system specifications.

Q: On the SO and SSOP demo-board, the LO oscillator circuit is tunable with a variable capacitor. Is this a requirement?

A: No. The variable capacitor is used to tune the LO freq., but one can use a fixed value. The advantage of going with a fixed value capacitor is that it is a cheaper component part and there is no need for tuning. The only advantage with a tunable LO is that a designer can optimize the performance of the receiver.

Q: I know that the IF bandwidth of the SA605 allows me to build an IF of 21.4MHZ. Will the SA605 SSOP package perform just as good at 21.4MHz IF as it does at 455kHz?

A: Although we have not worked with SA605 SSOP at 21.4MHZ, we believe that it would be difficult to get a 12dB SINAD measurement at -120dBm. The wavelengths are much smaller at 21.4MHz than 455kHz. Since the wavelengths are smaller, there is a higher probability of regeneration occurring in the IF section. Therefore, a designer will probably have to reduce the gain in the IF section. Additionally, the SSOP package has pins that are physically closer together than with the normal type of packaged parts which can contribute to the unstable state with higher IF frequencies.

Demodulating at 10.7MHz IF with the SA605/625 AN1996

Author: Alvin K. Wong

INTRODUCTION

The need for high speed communications is increasing in the market place. To meet these needs, high performance receivers must demodulate at higher IF frequencies to accommodate for the wider deviations in FM systems.

The standard 455kHz IF frequency, which is easier to work with, and thus more forgiving in production, no longer satisfies the high speed communication market. The next higher standard IF frequency is 10.7MHz. This frequency offers more potential bandwidth than 455kHz, allowing for faster communications.

Since the wavelength at 10.7MHz is much smaller than 455kHz, the demand for a good RF layout and good RF techniques increases. These demands aid in preventing regeneration from occuring in the IF section of the receiver. This application note will discuss some of the RF techniques used to obtain a stable receiver and reveal the excellent performance achieved in the lab.

BACKGROUND

If a designer is working with the SA605 for the first time, it is highly recommended that he/she reads AN1994 and AN1995. These two application notes discuss the SA605 in great detail and provide a good starting point in designing with the chip.

Before starting a design, it is also important to choose the correct part. Philips Semiconductors offers an extensive receiver line to meet the growing demands of the wireless market. Table 1 (see end of app note) displays the different types of receivers and their key features. With the aid of this chart, a designer will get a good idea for choosing a chip that best fits their design needs.

If low voltage receiver parts are required in a design, a designer can choose between a SA606, SA607, SA608, or SA626. All of these low voltage receivers are designed to operate at 3V while still providing high performance to meet the specifications for cellular radio. All of these parts can operate with an IF frequency as high as 2MHz. However, the SA626 can operate with a standard IF frequency of 10.7MHz and also provide fast RSSI speed. Additionally the SA626 has a power down mode to conserve battery power.

A close look at Table 1 will also show that there are subtle differences between the 3V receivers. The main differences between the SA606, SA607, and SA608 can be seen in the audio and RSSI output structure. Additionally the SA607 and SA608 provide a frequency check pin which can aid in locking in the desired received frequency over temperature.

OBJECTIVE

The objective of this application note is to show that the SA605 can perform well at an IF frequency of 10.7MHz. Since most Philips Semiconductors receiver demo-boards are characterized at RF = 45MHz/IF = 455kHz, we decided to continue to characterize at this frequency. This way we could compare how much degradation (for different IFs) there was with a RF = 45MHz/IF = 455kHz vs RF = 45MHz/ IF = 10.7MHz. As we will discuss later, there was minimal degradation in performance.

We also tested at RF = 240MHz/IF = 10.7MHz. The 240MHz RF is sometimes referred to as the first IF for double conversion receivers. Testing the board at RF=83.16MHz (which is also a common first IF for analog cellular radio) and IF = 10.7MHz was not done because the conversion gain and noise figure does not change that much compared to 45MHz input. Therefore, we can probably expect the same type of performance at 83.16MHz.

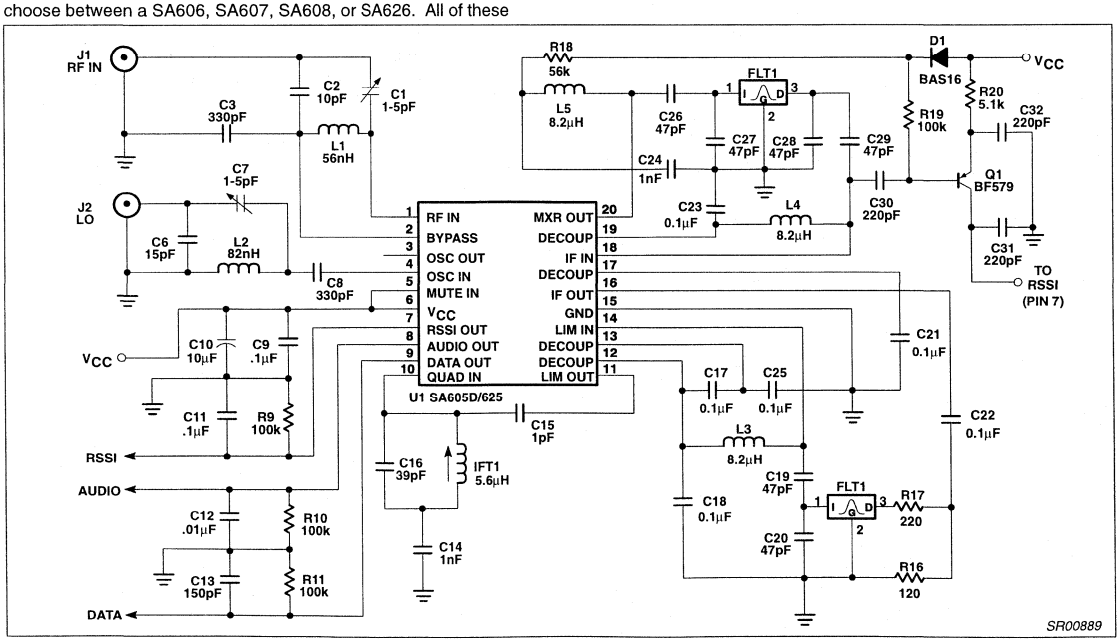

Figure 1. SA605/625 Schematic: RF = 240MHz, LO = 229.3MHz, IF = 10.7MHz

Demodulating at 10.7MHz IF with the SA605/625 AN1996

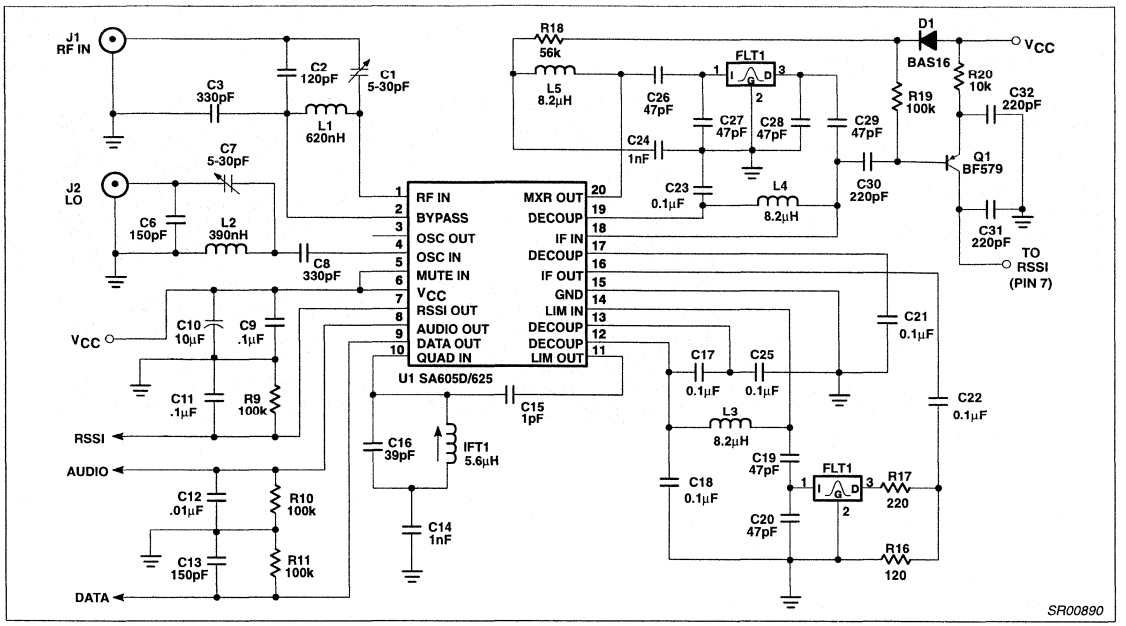

Figure 2. SA605/625 Schematic: RF = 45MHz, LO = 55.7MHz, IF = 10.7MHz

The RF = 240MHz/IF = 10.7MHz demo-board is expected to perform less than the RF = 45MHz/IF = 10.7MHz demo-board because the mixer conversion gain decreases while the noise figure increases. These two parameters will decrease the performance of the receiver as the RF frequency increases.

With the new demands for fast RSSI time, Philips Semiconductors has also designed receiver chips with fast RSSI speed: The SA624, SA625 and SA626. The SA625 can also be used in this layout because it is pin-for-pin compatible with the SA605. The RSSI circuitry was the only change done for the SA625, so performance will be similar to the SA605. Performance graphs shown in this application note will reveal the similarities.

For systems requiring low voltage operation, IF=10.7MHz and fast RSSI speed, the SA626 will be the correct choice, however, this application note does not address the performance of the SA626 because the SA626 was not available at this writing.

Board Set-Up and Performance Graphs

Figures 1 and 2 show the SA605/625 schematics for the 240MHz and 45MHz boards, respectively. Listed below are the basic functions of each external components for both Figures 1 and 2.

SO Layout Schematic List

U1- SA605 or SA625
FLT1-10.7MHz ceramic filter Murata SFE10.7MA5-A (280kHz BW)
FLT2-10.7MHz ceramic filter Murata SFE10.7MA5-A (280kHz BW)

Note: If a designer wants to use different IF bandwidth filters than the ones used in this application note, the quad tank's S-curve may need to be adjusted to accommodate the new bandwidth.

C1- Part of the tapped-C network to match the front-end mixer
C2- Part of the tapped-C network to match the front-end mixer
C3- Used as an AC short to Pin 2 and to provide a DC block for L1 which prevents the upsetting of the DC biasing on Pin 1
C6- part of the tapped-C network to match the LO input
C7- part of the tapped-C network to match the LO input
C8- DC blocking capacitor
C9- Supply Bypassing
C10-Supply bypassing (this value can be reduced if the SA605/625 is used with a battery)
C11-used as a filter, cap value can be adjusted when higher RSSI speed is preferred over lower RSSI ripple
C12-used as a filter
C13-used as a filter
C14-used to AC ground the quad tank
C15-used to provide the 90° phase shift to the phase detector
C16-quad tank component to resonant at 10.7MHz with IFT1 and C15
C17-IF limiter decoupling capacitor
C18-DC block for L3 which prevents the upsetting of the DC biasing on Pin 14
C19-part of the tapped-C network for FLT2
C20-part of the tapped-C network for FLT2
C21-IF amp decoupling cap
C22-DC blocking cap
C23-IF amp decoupling cap and DC block for L3 which prevents the upsetting of the DC biasing on Pin 14
C24-provides DC block for L5 which prevents the upsetting of the DC biasing on Pin 20
C25-IF limiter decoupling capacitor
C26-part of the tapped-C network for FLT1
C27-part of the tapped-C network for FLT1
C28-part of the tapped-C network for FLT1
C29-part of the tapped-C network for FLT1

R9- used to convert the current into the RSSI voltage
R10-converts the audio current to a voltage
R11-converts the data current to a voltage
R16-used to kill some of the IF signal for stability purposes
R17-used in conjunction with R16 for a matching network for FLT2

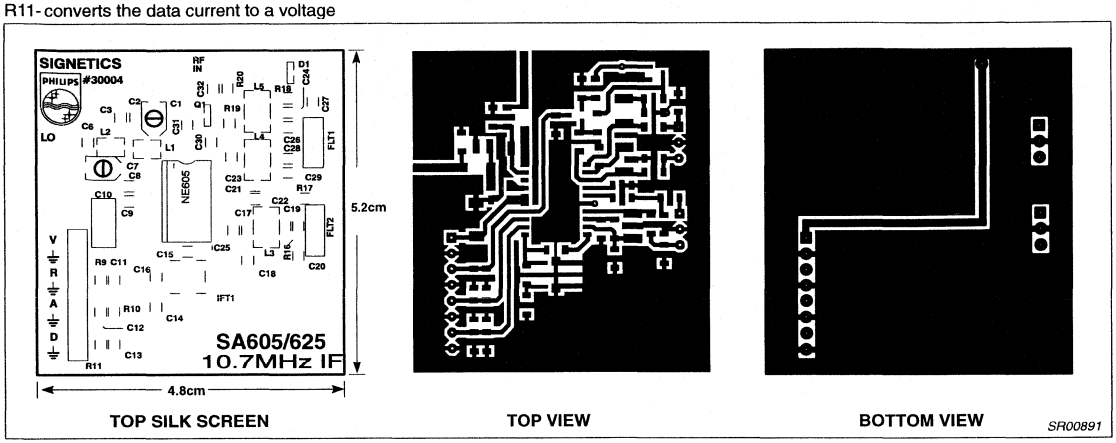

Figure 3. SA605/625 SO Demo-Board Layouts (Not Actual Size)

L1 - part of the tapped-C network to match the front-end mixer
L2 - part of the tapped-C network to match the front-end mixer
L3- part of the tapped-C network to match the input of FLT2
L4- part of the tapped-C network to match the input of FLT1
L5- part of the tapped-C network to match the input of FLT1

RSSI Extender Circuit

R18-provides bias regulation, the gain will stay constant over varying V_{CC}
R19-for biasing, buffer RF DC voltage
R20-provides the DC bias, RSSI gain (when R20 increases, RSSI gain decreases
C30-DC blocking capacitor which connects the ceramic filter's output to the PNP transistor's input
C31-decoupling capacitor, and should be removed for measuring RSSI systems speed
C32-peak detector charge capacitor
D1- diode to stabilize the bias current
Q1- Philips BF579 PNP transistor
IFT1-part of the quad tank circuit

There are minor differences between Figures 1 and 2. The RF and LO tapped-C component values are changed to accommodate for the different RF and LO test frequencies (RF=240MHz and 45MHz and LO = 229.3MHz and 55.7MHz). The other difference is the value of R20. This resistor value was changed to optimize the RSSI curve's linearity (see RSSI extender section in this application note for further details).

The recommended SA605/625 layout is shown in Figure 3. This layout can be integrated with other systems.

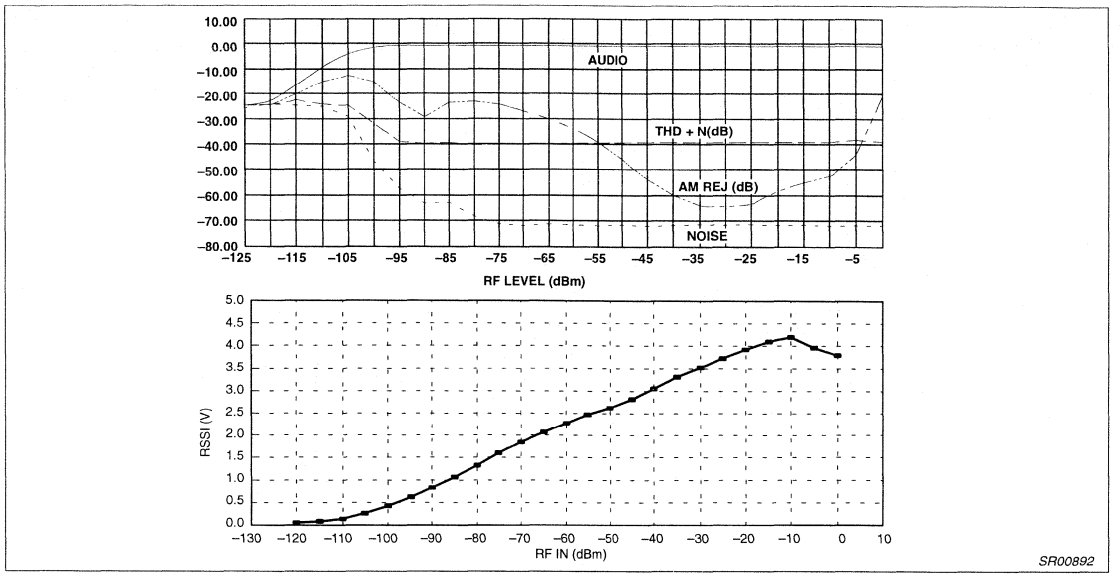

Figure 4. SA625 SO Performance Graphs at 240MHz

Figures 4 through 7 show the performance graphs for the SA605 & SA625 at 240MHz and 45MHz RF inputs. There was no real noticeable difference in performance between a SA605 or SA625 except for AM rejection. The SA605 appears to have a little better AM rejection, but from the end user's point of view, there is no difference between the receiver. All the other measurements were perfect, including SINAD.

RF Input

The SA605/625 board is set up to receive an RF input of 240MHz (see Figure 1). This is achieved by implementing a tapped-C network. The deviation should be set to ±70kHz to achieve ***-110dBm to -112dBm for -12dB SINAD***. However, the deviation can be increased to ±100kHz, depending on the bandwidth of the IF filter and the Q of the quad tank.

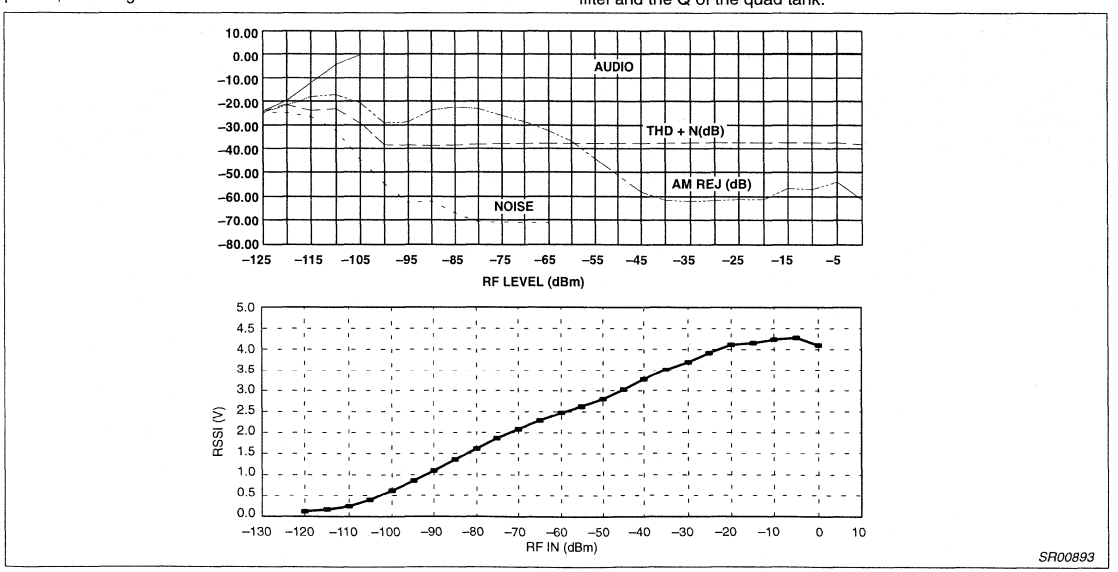

Figure 5. SA625 SO Performance Graphs at 45MHz

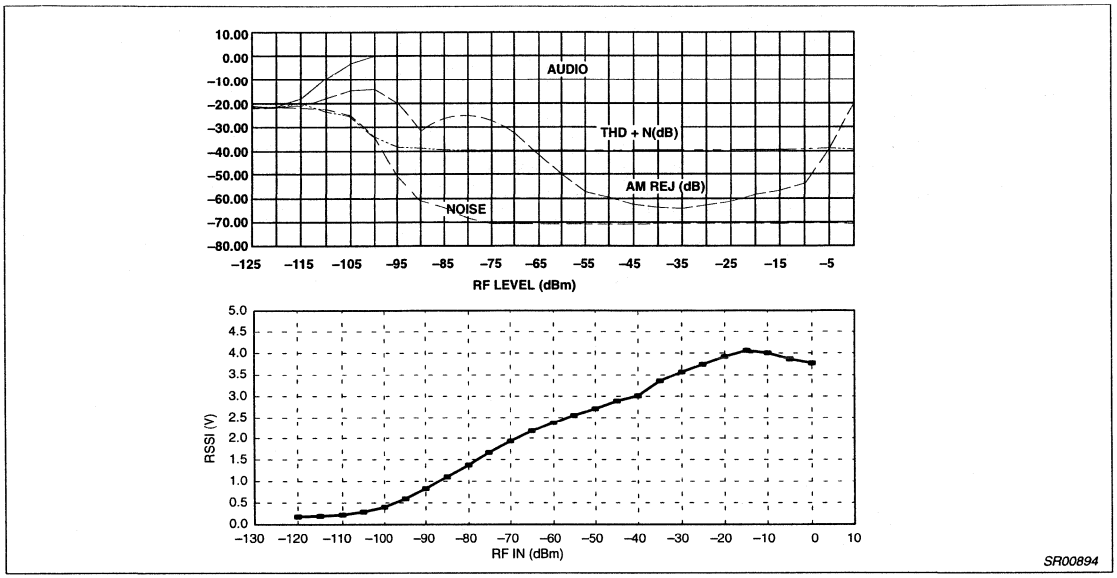

Figure 6. SA605SO Performance Graphs at 240MHz

Because we wanted to test the board at 45MHz, we changed the values of the tapped-C network for the RF and LO ports (see Figure 2). We found that a ***-116dBm to -118dBm for -12dB SINAD*** could be achieved. With these results, we were pretty

close to achieving performance similar to our standard 455kHz IF board.

A designer can also make similar RF and LO component changes if he/she needs to evaluate the board at a different RF frequency. *It should be noted that if a designer purchases a stuffed SA605/625 demo-board from Philips Semiconductors its set up will be for an RF input frequency of 240MHz.* AN1994 will aid the designer in calculating the tapped-C values for other desired frequencies, while AN1995 will be of value for making S11 bench measurements. Just remember that the input impedance will differ for different RF frequencies.

LO Input

The LO frequency should be 229.3MHz for the RF = 240MHz demo-board and have a drive level of -10dBm to 0dBm (this also applies for the RF = 45MHz and LO = 55.7MHz). The drive level is important to achieve maximum conversion gain. The LO input also has a matched tapped-C network for efficiency purposes which makes for good RF practices.

If a designer wanted to change the matching network to inject a different LO frequency, he/she could follow the steps in AN1994 and assume that the input impedance is around 10kΩ for low frequency inputs. The main goal is to get maximum voltage transfer from the signal generator to the inductor.

An external oscillator circuit was used to provide greater flexibility in choosing different RF and LO frequencies; however, an on-board oscillator can be used with the SA605/625. New high frequency fundamental crystals, now entering the market, can also be used for high LO frequency requirements. Most receiver systems, however, will use a synthesizer to drive the LO port.

10.7MHz Ceramic Filters

The input and output impedance of the 10.7MHz ceramic IF filters are 330Ω. The SA605/625's input and output impedances are roughly 1.5KΩ. Therefore, a matching circuit had to be implemented to obtain maximum voltage transfer. Tapped-C networks were used to match the filters input and output impedance.

But in this case, we decided to go with non-tuning elements to reduce set-up time. Figure 8 shows the values chosen for the network.

Although our total deviation is 140kHz, we used 280kHz IF bandwidth filters to maximize for fast RSSI speed. The SINAD performance difference between using 180kHz BW filter versus 280kHz BS filter was insignificant.

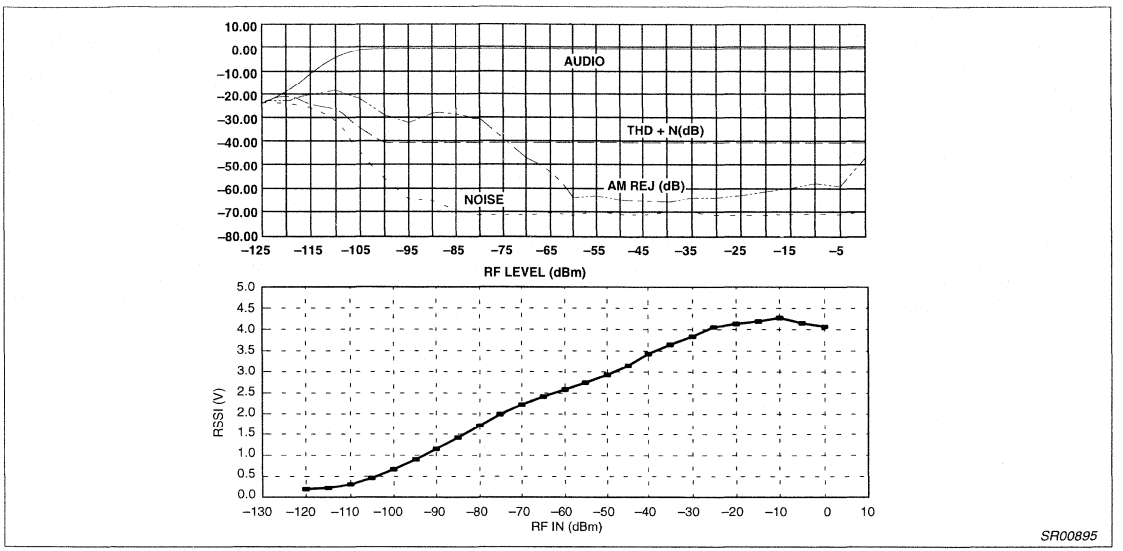

Figure 7. SA605 SO Performance Graphs at 45MHz

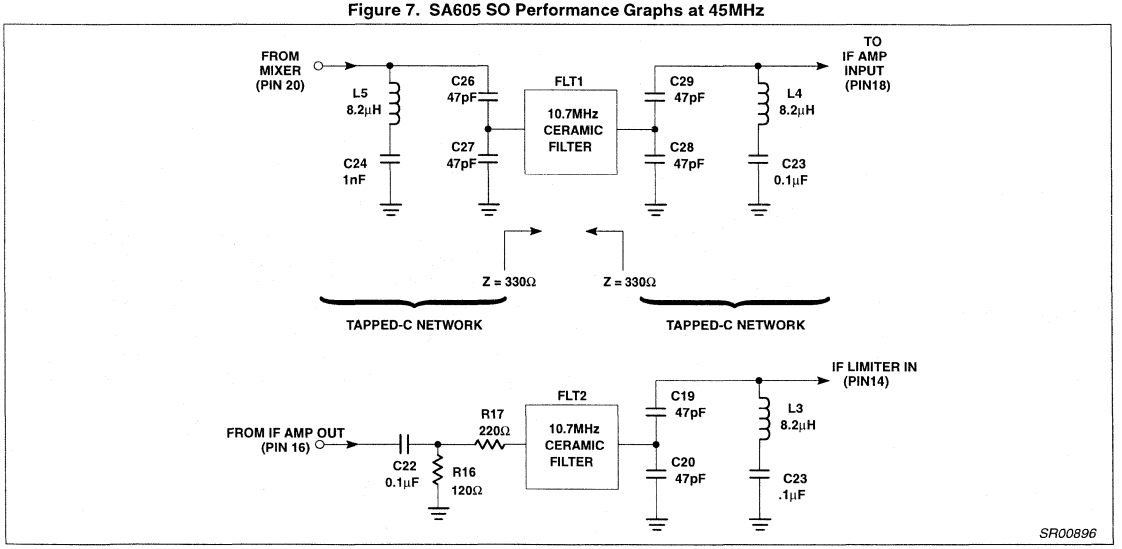

Figure 8. Matching Configuration for FLT1 and FLT2

Stabilizing the IF Section From Regeneration

Because the gain in the IF section is 100dB and the wavelength for 10.7MHz is small, the hardest design phase of this project was to stabilize the IF section.

The steps below show the methods used to obtain a stable layout.

1. The total IF section (IF amp and limiter) gain is 100dB which makes it difficult to stabilize the chip at 10.7MHz. Therefore, a 120Ω (R16 of Figure 1) resistor was used to kill some of the IF gain to obtain a stable system. (NOTE: Expect AM rejection performance to degrade as you decrease the IF gain externally.)
2. Since the tapped-C inductors for FLT1 and FLT2 are not shielded, it is important not to place them too close to one another. Magnetic coupling will occur and may increase the probability of regeneration.
3. It was also found that if the IF limiter bypass capacitors do not have the same physical ground, the stability worsens. Referring to Figure 1, the IF limiter bypass capacitors (C17, C25) are connected to assure a common ground.
4. The positioning of ground feedthroughs are vital. A designer should put feedthroughs near the IF bypass capacitors ground

points. In addition, feedthroughs are needed underneath the chip. Other strategic locations are important for feedthroughs where insufficient grounding occurs.

5. Shielding should be used after the best possible stability is achieved. The SA605/625 demo-board is stable, so shielding was not used. However, if put into a bigger system, shielding should be used to keep out unwanted RF frequencies. As a special note, if a good shield is used, it can increase the R16 resistor value such that there is less IF gain to kill to achieve stability. This means the RSSI dynamic range is improved. So if a designer does not want to implement the RSSI extender circuit, but is still concerned with SINAD and RSSI range, he/she can experiment with R16 and shielding because there is a correlation between them (see RSSI extender section in this application note for more information). In addition, AM rejection performance will improve due to the greater availability of the total IF gain.

The key to stabilizing the IF section is to kill the gain. This was done with a resistor (R16 in Figure 8) to ground. All the other methods mentioned above are secondary compared to this step. Lowering the value of this resistor reduces the gain and the increasing resistor value kills less gain. For our particular layout, 120Ω was chosen to obtain a stable board, but we were careful not to kill too much gain. One of the downfalls of killing too much gain is that the SINAD reading will become worse and the RSSI dynamic range is reduced.

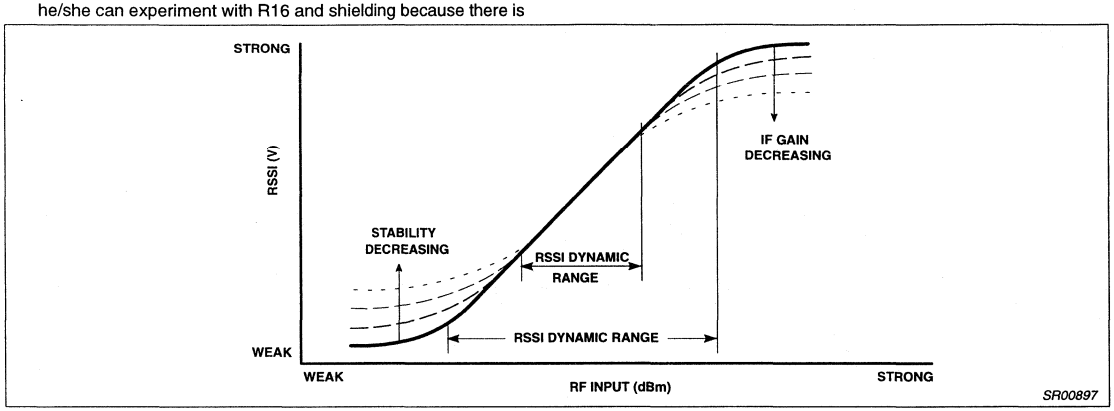

Figure 9. RSSI Dynamic Range

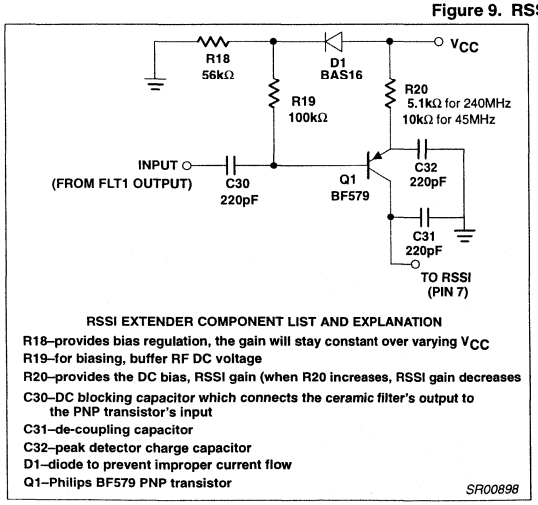

Figure 10. External RSSI Extender Circuit

RSSI Dynamic Range

There are two main factors which determine the RSSI dynamic range. These two factors are 1.) how stable is the board, and 2.) how much gain is killed externally. If the board is unstable, a high RSSI voltage reading will occur at the bottom end of the curve. If too much gain is taken away, the upper half of the curve is flattened. Thus the dynamic range can be affected. Figure 9 shows how the linear range can be decreased under the conditions mentioned above.

It is important to choose the appropriate resistor to kill enough gain to get stability but not too much gain to affect the upper RSSI curve dynamic range. Because we had to kill some IF gain to achieve good board stability and good SINAD readings, our RSSI overall dynamic range was reduced on the upper end of the curve.

Because SINAD and the RSSI dynamic range are two important parameters for most of our customers, we decided to add an "RSSI extender" modification to the board to get the best of both worlds. Together with the RSSI external modification and the "stability resistor", we can now achieve excellent SINAD readings and maintain a wide RSSI dynamic range.

RSSI Extender Circuit

The RSSI extender circuit increases the upper dynamic range roughly about 20-30dB for the 240MHz demo-board. The SA605/625 demo-board has 90-100dB of linear dynamic range when the RSSI modification is used.

Referring to Figure 10, one can see that one transistor is used with a few external components. The IF input signal to the PNP transistor is tapped after the ceramic filter to ensure a clean IF signal. The circuit then senses the strength of the signal and converts it to current, which is then summed together with the RSSI output of the chip.

The PNP transistor stage has to be biased as a class B amplifier. The circuit provides two functions. It is a DC amplifier and an RF detector. The gain of the RSSI extender can be controlled by R20 and R9 (Gain = R9/R20). Adjusting R20 is preferable because it

controls the upper half of the RSSI curve, whereas adjusting R9 shifts the whole RSSI curve.

If a different RF frequency is supplied to the mixer input, it is important to set the external RSSI gain accordingly. When the RF input was changed from 240MHz to 45MHz, the conversion gain of the mixer increased. Therefore, the earlier gain settings for the RSSI extender was too much. A lower gain setting had to be implemented such that a smoother transition would occur.

Quad Tank

The quad tank is tuned for 10.7MHz ($F=1/2\pi\sqrt{LC}$). Figure 1 shows the values used (C14,C15, C16, IFT1) and Figure 11 shows the S-curve. The linear portion of the S-curve is roughly 200kHz. Therefore, it is a good circuit for a total deviation of 140kHz. It is possible to deviate at 200kHz, but this does not leave much room for part tolerances.

If more deviation is needed, a designer can lower the S-curve with a parallel resistor connected to the quadrature tank. A designer should play with different value resistors and plot the S-curve to pick the best value for the design. To key in on the resistor value with minimum effort, a designer can put a potentiometer in parallel with the quad tank and tune it for best distortion. Then the designer can use fixed value resistors that are close to the potentiometer's value.

Fixed quad tank component values can be used to eliminate tuning, but a designer must allow for part tolerances and temperature considerations. For better performance over temperature, a resonator/discriminator can be used. Thus, no tuning is required for the quad tank section, which will save on production costs.

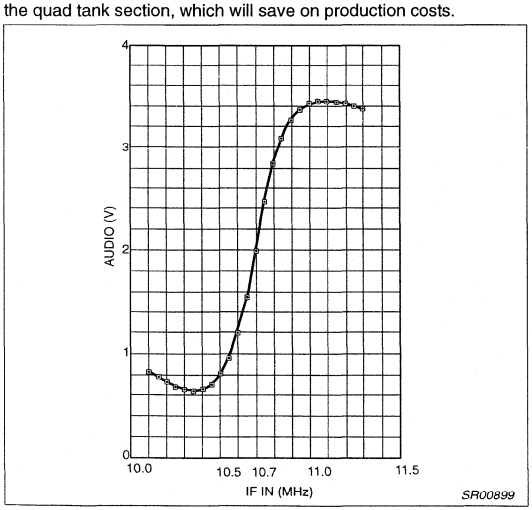

Figure 11. 10.7MHz Quad Tank S-Curve

RSSI System Speed

The RSSI rise and fall times are important in applications that use pulsed RF in their design. The way we define the speed is how fast the RSSI voltage can travel up and down the RSSI curve. Figure 12 shows a representation of this. Five different pulsed RF levels were tested to get a good representation of the RSSI speed. One can predict that the stronger the pulsed signal, the higher the RSSI voltage and the longer it will take for the fall time to occur. Generally speaking, the rise time is determined by how long it takes to charge up an internal capacitor. The fall time depends on how long it takes to discharge this capacitor.

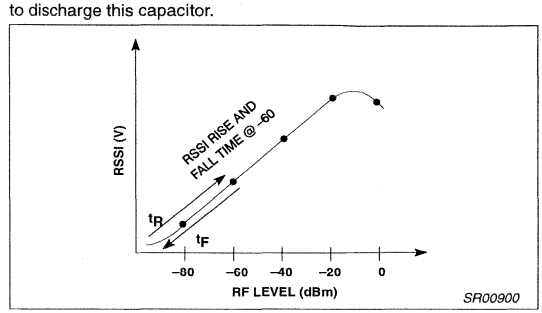

Figure 12. RSSI Cuve with Pulsed RF Levels

It is also important to understand that there are two types of RSSI speeds. The first type is the RSSI *chip* speed and the second is the RSSI *system* speed. The RSSI *chip* speed will be faster than the *system* speed. The bandwidth of the external filters and other external parts can slow down the RSSI system speed dramatically.

Figure 13 shows the bench set up for the RSSI system speed measurements. The pulsed RF was set for 10kHz and and the RSSI output was monitored with a digital oscilloscope. Figure 14 shows how the rise and fall times were measured on the oscilloscope.

The modifications done on the SA625 board are shown in Figure 15. The RSSI caps C11 and C31 were eliminated, and the RSSI resistor values were changed. We wanted to see how much time was saved by using a smaller RSSI resistor value.

The RSSI system speed for the 240MHz SA625 demo board is shown in Figure 16. Again, the only modification was that the RSSI caps (C11 and C31) were taken out and the RSSI resistor value (R9) was varied. For different RF levels, the speed seems to vary slightly, but this is expected. The higher the RSSI voltage, the longer it will take to come back down the RSSI curve for the fall time.

Looking more closely at Figure 16, one can note that the 0dBm input level has a faster fall time than the -20dBm level. This occurs because of the limited dynamic range of the test equipment. The equipment does not have sufficient on/off range, so at 0dBm the 'off' mode is actually still on. Therefore, you don't get a true reading.

At 0dBm the RSSI voltage is lower than –20dBm. The reason why this happens is because the RSSI linearity range stops at -10dBm. When the RF input drive is too high (e.g., 0dBm), the mixer conversion gain decreases, which causes the RSSI voltage to drop.

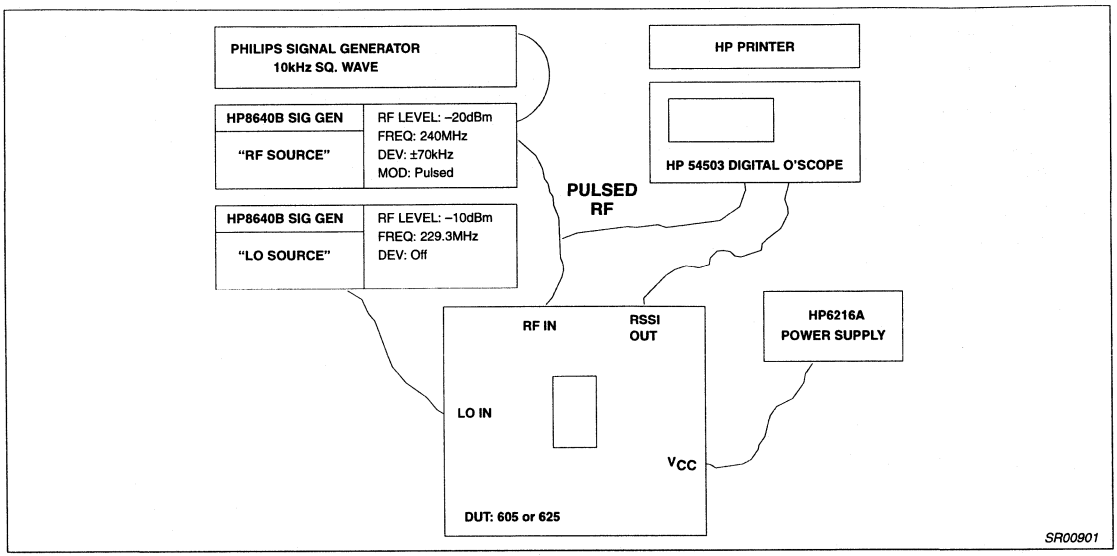

Figure 13. RSSI Speed Set-Up

QUESTION AND ANSWER SECTION

Q. What should the audio level at Pin 8 be?

A. The audio level is at 580mV$_{P-P}$ looking directly at the audio output pin and does not include a C-message filter. However, the audio output level will depend on two factors: the "Q" of the quadrature tank and the deviation used. The higher the quad tanks "Q", the larger the audio level. Additionally, the more deviation applied, the larger the audio output. But the audio output will be limited to a certain point.

Q. Am I required to use the 10µF supply capacitor?

A. No, a smaller value can be used. The 10µF capacitor is a suggested value for evaluation purposes. Most of the time a power supply is used to evaluate our demo boards. If the supply is noisy, it will degrade the receiver performance. We have found that a lower value capacitor can be used when the receiver is powered by a battery. But it is probably safer to stay at a reasonable capacitor size.

Q. Can I use different IF filters for my required bandwidth specifications?

A. Yes, you can order different IF filters with different bandwidths. Some of the standard manufacturers have 180kHz, 230kHz, and 280kHz bandwidths for 10.7MHz ceramic filters. Just be sure that the quad tank "S-curve" is linear for your required bandwidth. The SA605/625 demo-board has a 200kHz linearity for the quad tank. So ±70kHz deviation is perfect.

We have also found that even though the IF filter's bandwidth might be more than our requirements, it does not really degrade overall receiver performance. But to follow good engineering practices, a designer should order filters that are closest to their requirements. Going with wider bandwidth filters will give you better RSSI system speed.

Q. I want to use part of your demo board for my digital receiver project. Can you recommend a good 10.7MHz filter with accurate 10.7MHz center frequency which can provide minimum phase delay?

A. At the present time, I only know of one manufacturer that is working on a filter to meet digital receiver requirements. Murata has a surface mount 10.7MHz filter. The number is FX-6502 (SFECA 10.7). It was specifically designed for Japanese digital cordless phones. You can adapt these filters to our SA605/625 demo board.

We also used these filters in our layout and got similar SINAD and RSSI system speed performance compared to the standard 10.7MHz filters (280kHz BW). I believe the difference between the filters will be apparent for digital demodulation schemes.

Q. If the system RSSI time is dependent on the external components used, like the IF filters, then what is the difference in using the SA605 vs the SA625?

A. The difference comes in the fall time for high IF frequencies. You are correct that for IFs like 455kHz, there is probably little delta difference because the filter's bandwidth prohibits the speed dramatically. However, for 10.7MHz IFs, there will be a difference in the fall time between the chips because the bandwidths are much wider. Therefore, the chips will play a role in the RSSI system speed. The chip difference in RSSI speed will depend on your overall system configuration.

Q. Why does the AM rejection performance look better on the SA605, 455kHz IF board than the SA605/625 10.7MHz IF demo-board?

A. For the 455kHz IF demo-board there is more IF gain available compared to the 10.7MHz IF board. Recall that for the 10.7MHz IF board, some of the IF gain was killed externally for stability reasons. Since the IF gain helps improve AM rejection performance, by killing IF gain, AM rejection is decreased.

Demodulating at 10.7MHz IF with the SA605/625 AN1996

Q. The SA605/625 10.7MHz IF demo-board is made for the SO package. Can I use your SSOP package and expect the same level of performance?

A. We have not done a SSOP layout yet. But if the same techniques are used, I am sure the SSOP package will work. The SA626 demo-board will be done in SSOP, and probably be available in the future.

Q. I tried to duplicate your RSSI system reading measurements using your demo-board and I get slower times. What am I doing wrong?

A. The RSSI system speed measurements are very tricky. Make sure your cable lengths are not too long. I have found that when making microsecond measurements, lab set-up is of utmost importance. Also, make sure the RSSI caps (C11 and C31) are removed from the circuit.

Also be sure that the bandwidth of your IF filters is not slowing down the RSSI system speed (Cf: section on RSSI system speed).

Q. I am going to use your design in my NTT cordless digital phone. Can you recommend a 240.05MHz filter?

A. Murata SX-4896 (SAMAFC 240.05) is a filter you can use for your application.

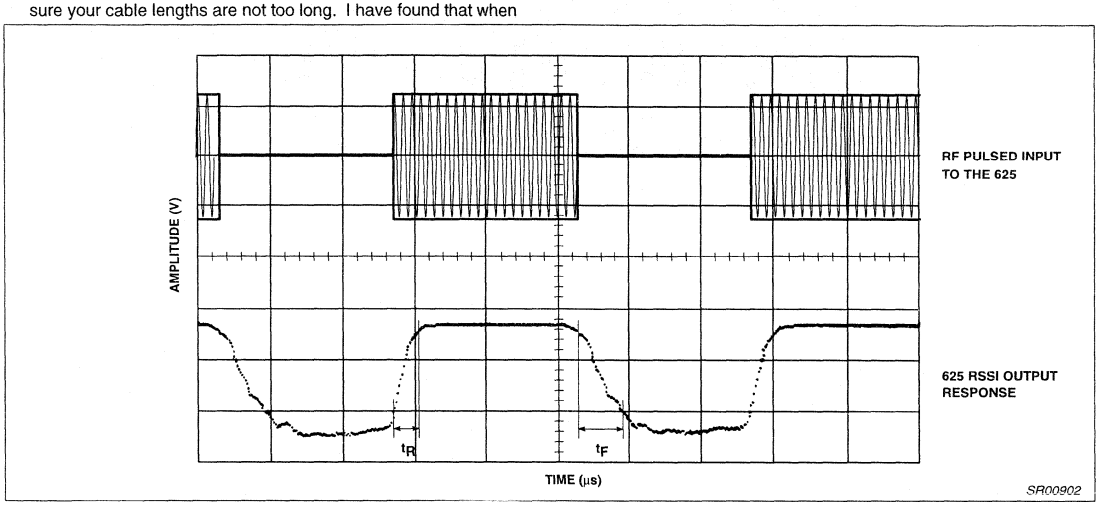

Figure 14. Oscilloscope Display of RSSI System Rise and Fall Time

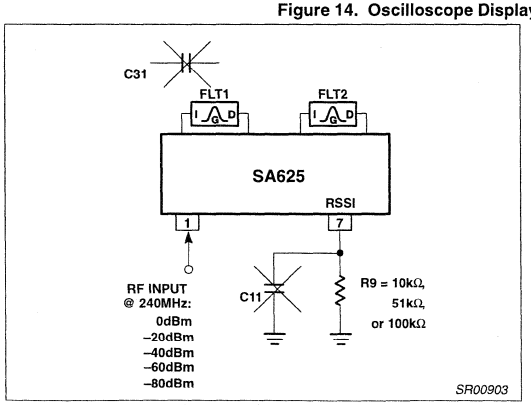

Figure 15. SA625 RSSI Test Circuit Configuration

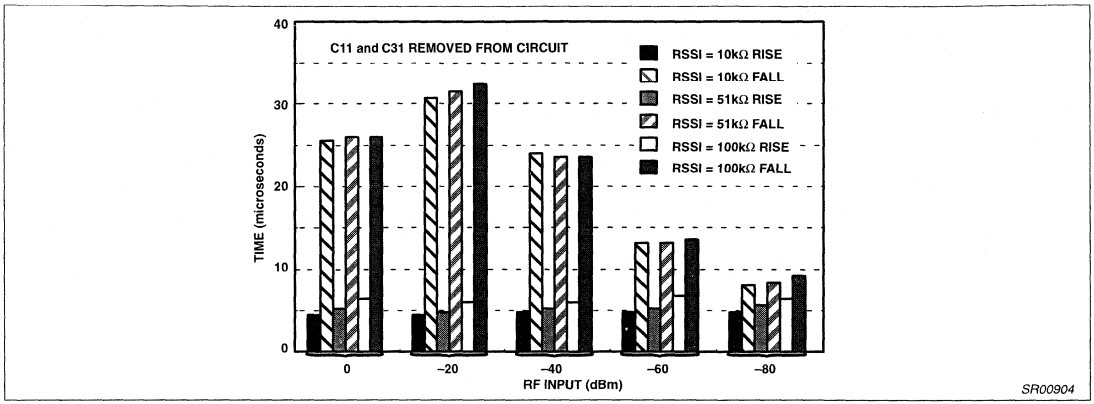

Figure 16. RSSI Systems Rise and Fall Time with Different RSSI Resistor Values

Table 1. FM/IF Family Overview

SR00905

Table 1. FM/IF Family Overview

			SA602A/604A		SA605	SA606	SA607	SA608	SA624	SA625	SA626	SA627
V_{CC}			4.5–8V	4.5–8V	4.5–8V	2.7–7V	2.7–7V	2.7–7V	4.5-8.0V	4.5-8.0V	2.7–5.5V	4.5-8.0V
I_{CC}			2.4mA@6V	3.3mA @ 6V	5.7mA @ 6V	3.5mA @ 3V	3.5mA @ 3V	3.5mA @ 3V	3.4mA @ 6V	5.8mA @ 6V	6.5mA @ 3V	5.8mA @ 6V
Number of Pins			8	16	20	20	20	20	16	20	20	20
Packages SA: 0 to +70°C SA: –40 to +85°C N: Plastic DIP D: Plastic SO FE: Ceramic DIP DK: SSOP			SA602AN SA602AD SA602AFE	SA604AN SA604AD	SA605N SA605D SA605DK				SA624N SA624D	SA625N SA625D SA625DK		SA627N SA627D SA627DK
			SA602AN SA602AD SA602AFE	SA604AN SA604AD	SA605N SA605D SA605DK	SA606N SA606D SA606DK	SA607N SA607D SA607DK	SA608N SA608D SA608DK	SA624N SA624D	SA625N SA625D SA625DK	SA626D SA626DK	627N 627D 627DK
–12dB SINAD (RF = 45MHz), IF = 455kHz) 1kHz Tone, 8kHz Dev.			–120dBm / .22uV		–120dBm / .22uV	–117dBm / .31uV	–117dBm / .31uV	–117dBm / .31uV	–120dBm / .22uV	–120dBm / .22uV	–112dBm / .54uV (RF = 240MHz) (IF = 10.7MHz) 1kHz Tone, +/–70kHz Dev.	–120dBm / .22uV
Process f_t			8GHz		8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz
For lower cost version and less performance			612A & 614A		615	616	617	—	—	—	—	—
Features			– Audio & Data pins – IF BW of 25MHz – No external matching required for standard 455kHz IF filter		– Audio & Data pins – IF BW of 25MHz – No external matching required for standard 455kHz IF filter	– Low voltage – Internal RSSI and audio op amps – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Freq check pin – Low voltage – Internal RSSI and audio op amps – Unity gain RSSI output – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Freq check pin – Low voltage – Internal RSSI and audio op amps – Unity gain audio output – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Fast RSSI Time – Pin-to-Pin compatible with 604A – No external matching required for standard 455kHz IF filter	– Fast RSSI Time – Pin-to-Pin compatible with 605 – No external matching required for standard 455kHz IF filter	– Power down mode – Low voltage – Fast RSSI Time – IF BW of 25MHz – Internal RSSI & audio op amps – No external matching required for standard 10.7MHz IF filter	– Fast RSSI Time – Freq check pin – IF BW of 25MHz – Internal RSSI & audio op amps – No external matching required for standard 455kHz IF filter
RSSI OUTPUT SECTION	**Dynamic Range**		90dB		90dB	90dB	90dB	90dB	90dB	90dB	90dB	90dB
	Accuracy		+/–1.5dB		+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB
	455kHz IF	**Rise * Time**	—	1.4us	—	—	—	—	1.1us	1.2us	—	1us
		Fall * Time	—	21.3us	—	—	—	—	1.3us	2.1us	—	1.7us
	10.7MHz IF	**Rise * Time**	—	1.5us	—	—	—	—	1.2us	1.2us	1.2us	0.9us
		Fall * Time	—	19.4us	—	—	—	—	1.6us	2us	2us	1.4us

***NOTE: No IF filters in the circuit**

Table 1. (cont.) FM/IF Family Overview

			SA602A/604A		SA605	SA606	SA607	SA608	SA624	SA625	SA626	SA627
MIXER		Max. Conversion Power Gain (RF = 45MHz; IF = 455kHz)	17dB	—	13dB	17dB	17dB	17dB	—	13dB	13dB	13dB
		3rd Order Intercept Point (Input) f1 = 45MHz f2 = 45.06MHz	–13dB	—	–10dBm	–9dBm	–9dBm	–9dBm	—	–10dBm	–11dBm f1 = 240.05 f2 = 240.35	–10dBm
		Noise Figure @45MHz	5dB	—	5dB	6.2dB	6.2dB	6.2dB	—	5dB	11dB @ 240MHz	5dB
		RF Input Resistance and Capacitance @45MHz	1.5k 3pF	—	4.7k 3.5pF	8k 3pF	8k 3pF	8k 3pF	—	4.7k 3.5pF	4.7k 3.5pF @ 240MHz	4.7k 3.5pF
		Output Resistance	1.5k	—	1.5k	1.5k	1.5k	1.5k	—	1.5k	330	1.5k
IF SECTION	IF AMP	Input Impedance	—	1.6k	1.6k	1.5k	1.5k	1.5k	1.6k	1.6k	330	1.5k
		Output Impedance	—	1.0k	1.0k	330	330	330	1.0k	1.0k	330	1.0k
		Gain	—	40dB	40dB	44dB	44dB	44dB	40dB	40dB	44dB	40dB
		BW	—	41MHz	41MHz	5.5MHz	5.5MHz	5.5MHz	41MHz	41MHz	40MHz	40MHz
	IF LIMITER	Input Impedance	—	1.6k	1.6k	1.5k	1.5k	1.5k	1.6k	1.6k	330	1.5k
		Output * Impedance	—	330	330	330	330	330	330	330	330	330
		Gain	—	60dB	60dB	58dB	58dB	58dB	40dB	60dB	58dB	60dB
		BW	—	28MHz	28MHz	4.5MHz	4.5MHz	4.5MHz	28MHz	28MHz	28MHz	28MHz
	Total IF Gain		—	100dB	100dB	100dB	100dB	100dB	100dB	100dB	96dB (includes –6dB pad)	100dB
	Total IF BW		—	25MHz	25MHz	2MHz	2MHz	2MHz	25MHz	25MHz	25MHz	25MHz

NOTE: *Not designed to drive a matched load

SR00906

Philips FM/IF systems for GMSK/GFSK receivers AN1997

Author: Yanpeng Guo

ABSTRACT

To assist Philips Semiconductors customers in digital cellular and wireless/PCS system design, a Philips FM/IF system-based GMSK/GFSK demoboard has been developed based on CT-2 specifications. This application note presents a detailed description of this board including circuits, design information, and measured BER performance. The circuit diagram, component list, and board layout are also included.

INTRODUCTION

In order to meet the rapidly increasing demand for mobile radio and wireless/PCS services, digital cellular and digital wireless systems have become the new generation of mobile communications for higher capacity. It is a new challenge for engineers to find IC solutions for these digital wireless applications.

In worldwide digital cellular, wireless/PCS standards, GMSK/GFSK modulation techniques have been widely employed as illustrated in Table 1. In order to assist the applications of Philips ICs in these digital systems, a Philips FM/IF system-based GMSK/GFSK demoboard has been developed. The purpose of this application note is to provide a detailed description of this board, to help customers achieve the best performance using Philips SA626, and also to provide suggestions for the applications of other Philips FM/IF systems.

Table 1. A Summary of Digital Cellular and Cordless Standards

Standard	Access	Modulation	Bit Rate	Ch. Spacing
IS-54	TDMA	π/4-DQPSK	48 kb/s	30 kHz
GSM	TDMA	GMSK	270 kb/s	200 kHz
CT-2	TDMA	GFSK	72 kb/s	100 kHz
DECT	TDMA	GFSK	1.152 Mb/s	1.728 MHz

This application note is organized as follows:

- Introduction.
- Review of GMSK/GFSK modulation: advantages of GMSK/GFSK modulation techniques and implementation methods.
- Overview of the demoboard: general block diagram and detailed description of each part of the board.
- BER measurements: measurement set-up, procedures, and measured results.
- Questions & Answers.

REVIEW OF GMSK/GFSK MODULATION

GMSK(Gaussian Minimum Shift Keying) is a premodulation Gaussian filtered binary digital frequency modulation scheme with modulation index of 0.5. The following features make GMSK very suitable for digital cellular and wireless applications.

1. Constant envelope: this allows the operation of Class-C RF power amplifiers to achieve higher system power efficiency.
2. Narrow power spectrum: narrow mainlobe and low spectral tails keep the adjacent channel interference to low levels and achieve higher spectral efficiency.
3. Coherent/non-coherent detection capabilities.
4. Good BER performance.

GMSK modulation can be implemented in two ways. The most straightforward way is to transmit the data stream through a Gaussian low-pass filter and apply the resultant wave form to a voltage controlled oscillator (VCO) as shown in Figure 1. The output of the VCO is then a frequency modulated signal with a Gaussian response. The advantage of this scheme is the simplicity, but it is difficult to keep an exact modulation index of 0.5 with this scheme. Therefore, VCO implemented GMSK is usually used in non-coherent detection systems such as DECT and CT2.

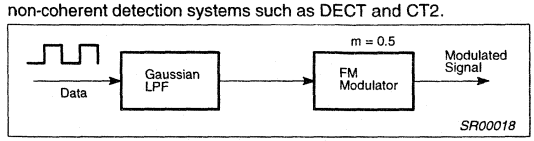

Figure 1. VCO Implemented GMSK Modulator

GMSK signals can also be generated using a quadrature modulation structure. Consider the phase modulated signal given by:

$$s(t) = \cos[\omega_C t + \phi(t)] \quad \text{(EQ. 1)}$$

This can be expanded into its in-phase and quadrature components,

$$s(t) = \cos[\phi(t)]\cos(\omega_C t) - \sin[\phi(t)]\sin(\omega_C t) \quad \text{(EQ. 2)}$$

The quadrature modulator is based on Equation (2). The implementation of such a GMSK modulator is shown in Figure 2. The incoming data is used to address two separate ROMs which contain the sampled versions of all possible phase trajectories within a given interval. After D/A conversion, the output of each ROM is applied to the I/Q modulator. The output is the GMSK modulated signal. This implementation scheme provides an exact modulation index of 0.5, which allows coherent detection.

GFSK (Gaussian Frequency Shift Keying) is also a premodulation Gaussian filtered digital FM scheme, but without the restriction of modulation index to be 0.5. The block diagram of GFSK modulator is the same as shown in Figure 1, but the modulation index can be specified according to the applications.

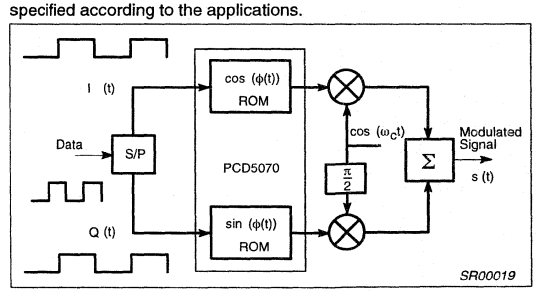

Figure 2. I/Q Implemented GMSK Modulator

GMSK signals can be demodulated in three ways: 1.) FM discriminator detection, 2.) differential detection, and 3.) coherent detection. The coherent detection scheme has the best BER performance, but is only suitable for I/Q structure based GMSK systems (Ref 6.). The differential detection method has BER degradation even with complex implementation (Ref 7.). The limit/frequency discriminator structure is the simplest scheme suitable for both GMSK and GFSK applications. Therefore, the FM discriminator technique is widely used for GMSK/GFSK demodulation in digital cellular/PCS applications. Figure 3 presents the block diagram of an FM discriminator GMSK/GFSK demodulator.

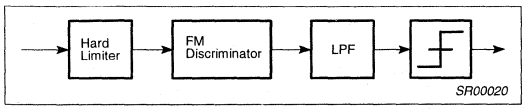

Figure 3. Limit/Frequency Discriminator GMSK/GFSK Demodulator

OVERVIEW OF THE GMSK/GFSK DEMOBOARD

Figure 4 is the block diagram of a VCO/FM discriminator based GMSK/GFSK modem (modulator/demodulator), which also illustrates the structure of the Philips GMSK/GFSK demoboard. The demoboard contains the entire demodulator as well as the Gaussian low-pass filter (LPF) for the modulator. The input data stream is first premodulation filtered by the Gaussian LPF, then the filtered base band wave form is applied to an FM signal generator with specific modulation index. The output is then the GMSK/GFSK modulated signal. After the limit/frequency discriminator detection, a Gaussian LPF is employed to eliminate noise. The output of the threshold detector is the regenerated binary data, which can be sent to a data error analyzer to evaluate the BER performance.

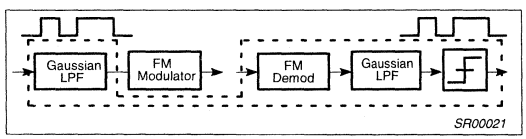

Figure 4. VCO/FM Discriminator GMSK/GFSK Modem (dotted line for the demoboard)

Gaussian LPF

On the demoboard, a 4th-order Gaussian LPF is implemented for both premodulation filtering and post demodulation filtering. The response function of this 4th-order filter can be expressed as (Ref 4.):

$$H(s) = \frac{\omega_1^2}{S^2 + 2\zeta_1\omega_1 S + \omega_1^2} \cdot \frac{\omega_2^2}{S^2 + 2\zeta_2\omega_2 S + \omega_2^2} \quad \text{(EQ. 3)}$$

By looking up the Gaussian LPF poles table[4], with 3dB bandwidth normalized to unity, we have:

$$\omega_1 = 1.9086, \quad \zeta_1 = 0.7441; \quad \omega_2 = 1.6768, \quad \zeta_2 = 0.9720$$

This 4th-order Gaussian LPF is implemented with switched capacitor filters. The reason for using this scheme is that the LPF's 3dB bandwidth can be controlled by an external clock which allows generating GMSK signals with different BTb. To realize a 4th-order LPF, two stages of LMF100 are cascaded and operated at mode-3[5]. Figure 5 shows the circuit diagram for this mode.

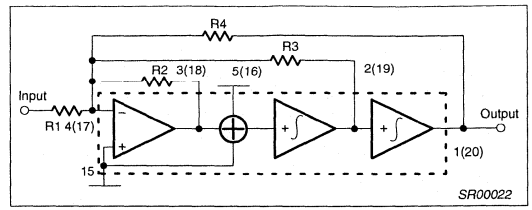

Figure 5. Circuit Diagram of LPF with LMF100 at Mode-3

For mode-3 LPF applications, the following formulas can be used to calculate the resistor values [5]:

$$H_{LP}(s) = \frac{H_{OLP}\omega_0}{S^2 + S\omega_0/Q + \omega_0} \quad \text{(EQ. 4)}$$

where, $H_{OLP} = -\frac{R_4}{R_1}$ (EQ. 5)

$$\omega_0 = \left(\frac{f_{CLK}}{100}\right) \cdot \sqrt{\frac{R_2}{R_4}} \quad \text{(EQ. 6)}$$

$$Q = \left(\frac{R_3}{R_2}\right) \cdot \frac{\sqrt{R_2}}{R_4} \quad \text{(EQ. 7)}$$

Example:

Step 1. Decide the gain and choose R value:
For unity gain, we have
$H_{OLP} = -R_4/R_1 = -1$, i.e. $R_4 = R_1$.
For the first stage, we choose a convenient value for input resistance: $R_{14} = R_{11} = 22k\Omega$

Step 2. Calculate R_{12}:
Compare (3) with (4), we have:

$$\omega_1 = \left(\frac{f_{CLK}}{100}\right) \cdot \sqrt{\frac{R_{12}}{R_{14}}} \quad \text{(EQ. 8)}$$

By choosing f_{clk} = 100 times the 3dB bandwidth, we have

$$\omega_1 = \sqrt{\frac{R_{12}}{R_{14}}} \rightarrow R_{12} = 80.14k\Omega$$

Step 3. Calculate R_{13}:
From the comparison of (3) and (4), we also have,

$$Q_1 = \frac{1}{(2\zeta_1)} = \left(\frac{R_{13}}{R_{12}}\right) \cdot \sqrt{\frac{R_{12}}{R_{14}}} = \frac{1}{(2 \cdot 0.7441)} \quad \text{(EQ. 9)}$$

$R_{13} = 28.22k\Omega$

For the second stage, the resistor values can be calculated by the same procedures. For this example, they are:

$R_{24} = R_{21} = 22k\Omega$
$R_{22} = 61.86k\Omega$
$R_{23} = 18.98k\Omega$

To obtain a good Gaussian LPF, the resistor values have to be adjusted with all input/output circuits connected. Baseband eye-diagrams and modulated power spectrum could be the references for the adjustment. The final values for this example are shown in the circuit diagram.

FM/IF System

The Philips low-voltage high performance monolithic FM/IF system, SA626, is employed for demodulation on the GMSK/GFSK demoboard. SA626 was designed specially for wide bandwidth portable communications applications, incorporating with a mixer/ oscillator, two limiting intermediate frequency amplifiers, quadrature detector, and audio and RSSI op amps. The RF section is similar to the famous SA605. The audio and RSSI outputs have amplifiers. With power down mode, SA626 will function down to 2.7V. Figure 6 is the block diagram of SA626. Detailed information can be found in the data book and application note [1, 2, 3].

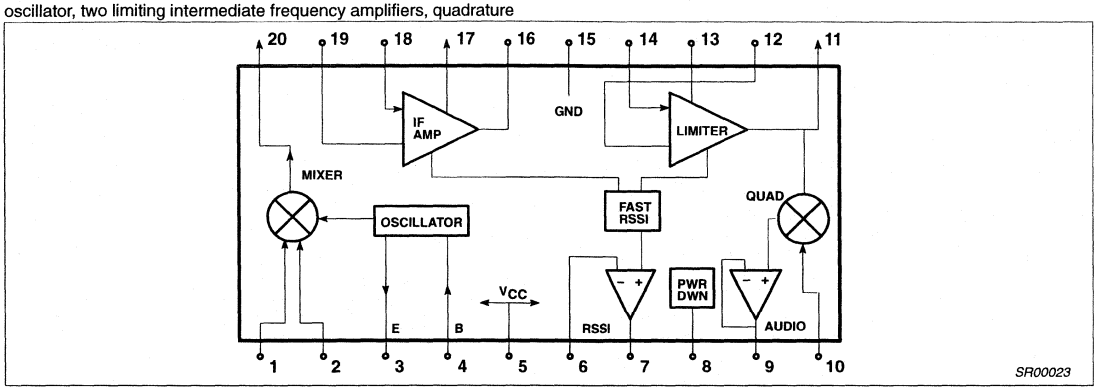

Figure 6. Block Diagram of the FM/IF System SA626

The GMSK/GFSK demoboard is designed for an RF frequency of 45MHz, LO frequency of 55.7 MHz, and intermediate frequency of 10.7MHz. For different RF frequency applications, the step-by-step matching circuits design procedure is presented in Ref. 1.

Although this demoboard is designed with SA626 based on CT-2 specifications, Philips also provides FM/IF solutions for many other GMSK/GFSK systems. SA626 is specially designed for wide bandwidth applications. For lower data rate applications such as CDPD (19.2 kb/s), SA605/625 family is recommended. For DECT and other high data rate applications, SA636 and SA639 are the recommended solutions. Data (audio) output bandwidth is the main limiting factor for high data rate applications. Table 2 presents a summary of the major characteristics of Philips FM/IF systems. The suggested maximum data rate for each part is an approximation based on the baseband eye pattern. Higher data rate could be operated with some modifications or if more BER degradation is allowed.

Table 2. Major Characteristics of the FM/IF Systems

	SA602/604	SA605	SA625	SA626	SA636	SA639*
V_{CC}	4.5 - 8V	4.5 - 8V	4.5 - 8V	2.7 - 5.5V	2.7 - 5.5V	2.7 - 5.5V
I_{CC}	2.4/3.3mA @ 6V	5.7mA @ 6V	5.7mA @ 6V	6.5mA @ 3V	6.5mA @ 3V	8.3mA @ 3V
SINAD	-120dBm/.22µV (RF: 45MHz, IF: 455kHz, 1kHz tone, 8kHz Dev.)	-120dBm/.22µV (RF: 45MHz, IF: 455kHz, 1kHz tone, 8kHz Dev.)	-120dBm/.22µV (RF: 45MHz, IF: 455kHz, 1kHz tone, 8kHz Dev.)	-112dBm/.54µV (RF: 240MHz, IF: 10.7MHz, 1kHz tone, 70kHz Dev.)	-111dBm/.54µV (RF: 240MHz, IF: 10.7MHz, 1kHz tone, 125kHz Dev.)	-111dBm/.54µV (RF: 240MHz, IF: 10.7MHz, 576kHz tone, 288kHz Dev.)
Features	Audio & Data pins IF BW of 25MHz Matching for standard 455kHz IF filters	Audio & Data pins IF BW of 25MHz Matching for 455kHz IF filters	Pin compatible with SA605 Fast RSSI IF BW of 25MHz Matching for 455kHz IF filters	Power down mode Low voltage Fast RSSI IF BW of 25MHz Int. RSSI & Audio op amp Matching for 10.7MHz IF filters	Power down mode Low voltage Fast RSSI IF BW of 25MHz Int. RSSI op amp Wideband data out Matching for 10.7MHz IF filters	Power down mode Low voltage Fast RSSI IF BW of 25MHz Int. RSSI op amp Wideband data out Post detection amp Matching for 10.7MHz IF filters
Data Rate**	100kb/s	100kb/s	100kb/s	300kb/s	1.5Mb/s	2Mb/s
NOTES	* Objective specifications. ** Approximated maximum data rate. With some modifications, higher data rate might be operated.					

Threshold Detector and Data Regeneration

A 2-level threshold detector with sampling time adjustment circuits is implemented for data regeneration as shown in the circuit diagram. The output base band signal (eye-diagrams) from SA626 is first fed into a comparator (LM311) to generate a TTL logic signal which is then sampled with the data clock at the transmitting bit rate. The phase of the data clock can be adjusted manually through a monostable multivibrator (74HC123) to achieve the optimal sampling

time. The demoboard is initially adjusted for a bit rate of 72 kb/s. If a different data rate is used, the sampling time has to be re-adjusted.

The symbol timing recovery (STR) circuit is not implemented on this demoboard. The transmitting data clock should be either hard-wire connected from the transmitter, or obtained from a separate STR circuit for operation. The measured performance presented in this paper is conducted with hard-wire connected data clock. However, BER degradation caused by STR should be no more than 1dB (Ref 8.).

PERFORMANCE MEASUREMENTS

The performance of this GMSK/GFSK demoboard including receiver sensitivity and BER is experimentally evaluated. BER performance is evaluated based on CT-2 specifications. Measurement procedures and the measured results are presented in this section.

Measurement Set-up

Figure 7 illustrates the measurement set-up with the GMSK/GFSK demoboard. A data error analyzer is employed to generate a pseudo random binary sequence (PRBS) with length of 10^9 -1 at a data rate of 72kb/s. This data sequence is sent to the Gaussian LPF on the board for premodulation filtering. The output Gaussian filtered base band signal is then applied to an FM signal generator as the modulating signal. To generate a GMSK modulated signal (modulation index = 0.5) at a bit rate of 72kb/s, frequency deviation of the FM signal generator needs to be set at 18kHz. The output from the generator is then a GMSK modulated signal (at 45MHz). Another signal generator is employed to provide an LO signal at 55.7MHz for the FM/IF system detection.

After FM discriminator detection, the output base band signal is fed into another Gaussian LPF on the board to eliminate noise. The 3dB bandwidth of both Gaussian LPFs is controlled by an external clock. This clock should be a square wave signal with TTL level. By controlling the frequency of this clock, different BTb can be achieved for certain bit rate. To have BTb equal 0.5 with bit rate of 72kb/s, the clock signal is set at 3.6MHz (100 times the required 3dB bandwidth). The output from the LPF is then sent to the threshold detector for data regeneration. The data clock signal is taken directly from the data error analyzer. The sampling time can be controlled by adjusting VR2 in the circuit diagram. The recovered data sequence is fed back to the Data Error Analyzer for BER measurement.

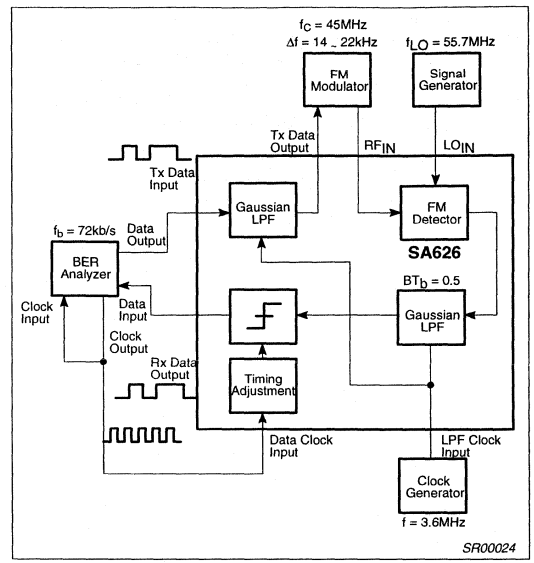

Figure 7. Measurement Set-Up with the GMSK/GFSK Board

Measurement Procedure and Results

1. **Measure SINAD at the audio output of SA626:** use the same set-up as described above, but set RF = 45MHz, fm = 1kHz, Δf = 8kHz; LO = 55.7MHz, -10dBm; the measured typical sensitivity for 12dB SINAD should be about -110dBm. (See Ref 1. for detailed SINAD measurement.)
2. **Check "LPF clock input":** this clock should be a TTL level signal with the frequency of 100 times the desired 3dB bandwidth of the LPF. For the data rate of 72kb/s and BTb = 0.5 LPF, the clock frequency is 3.6MHz (100 × 36kHz).
3. **Check "Tx data input":** 72kb/s baseband NRZ signal.
4. **Measure "Tx data output":** Gaussian low-pass filtered baseband eye-diagram as shown in Figure 8.
5. **Check "data clock input":** 72kHz clock signal.
6. **Adjust sampling position:** by adjusting VR2, set the rising edge of the clock at Pin 11 of Unit 4 (74HC74) to be at the center of the eye-diagram at Pin 2 of Unit 6 (LM311) in the circuit diagram.
7. **Measure BER with high RF level:** set RF input signal level at -80dBm and -90dBm, LO signal level at -10dBm: error free.
8. **Measure BER vs. RF input level curve:** RF level: -94 ~ -104 dBm, LO level: -10dBm, at each point, at least 100 errors have to be measured. Figure 9 presents the measured BER as a reference.

QUESTIONS & ANSWERS

Q. For the SINAD measurement, is it necessary to connect the whole system?

A. Even though only part of the system is used to measure SINAD, it is recommended to connect the whole system because the RF part should be tested under the operating conditions.

Q. Why is the DC current (I_{CC}) very large when I measure the SINAD on SA626?
A. Check the power supplies. Make sure both +5V and -5V are connected all the time even though only +5V is needed for SA626.

Q. Is it possible that SINAD is good, but BER is not good?
A. Yes, because there are other factors affecting BER .

Q. Is it possible that SINAD is bad, but BER is good?
A. No. Good SINAD is a necessary condition to achieve good BER.

Q. What are the main factors affecting BER?
A. They are:
1. Tx LPF
2. FM deviation and RF signal level
3. RF part sensitivity
4. Rx LPF
5. Threshold detector
6. Sampling time

Q. There are two "Rx Data Output" ports. Which one should be used?
A. Two "Rx Data Output" ports are designed to provide convenience for different measurement conditions. Either one can be used if the BER analyzer has the Q/$\overline{Q}$ detection capability.

Q. What needs to be done for higher RF frequency applications?
A. First, RF and LO input matching circuits have to be redesigned at the desired frequency. Second, the layout of RF and LO input circuits might also need to be re-designed. The inputs should be further away from each other and in different directions (not in parallel with each other) to provide better isolation.

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6. "GMSK modulation for digital mobile radio telephony", K. Murota and K. Hirade, *IEEE Transactions on Communications*, July 1981.
7. "Low complexity GMSK modulator for integrated circuit implementation", S. Grath and C. J. Burkley, *Proceedings of IEEE VTC'90.*
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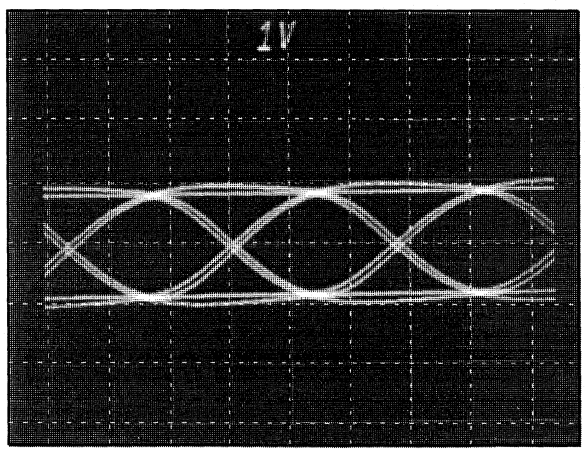

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Figure 8. Baseband Eye-Diagram at the Output of Tx Gaussian LPF

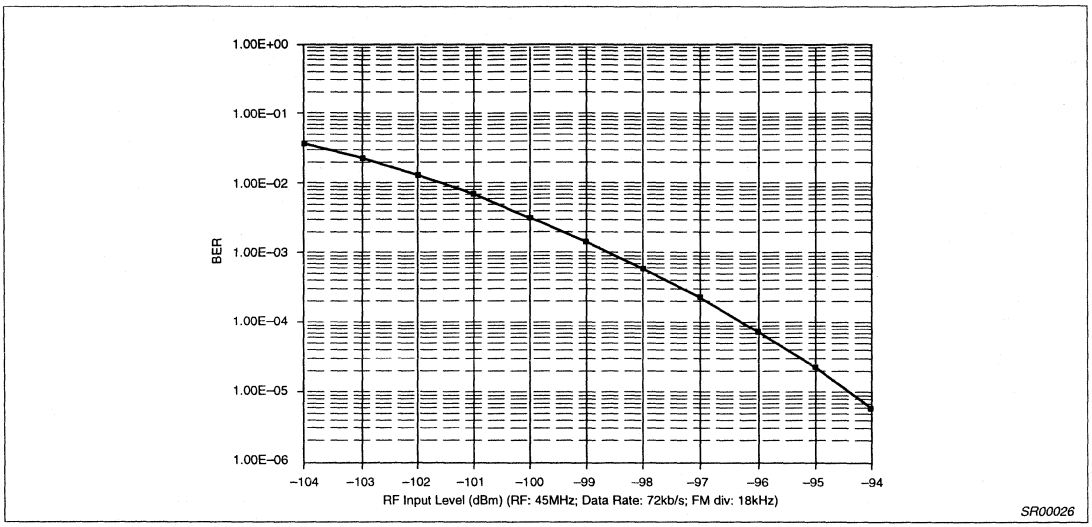

Figure 9. BER of the GMSK/GFSK Demoboard

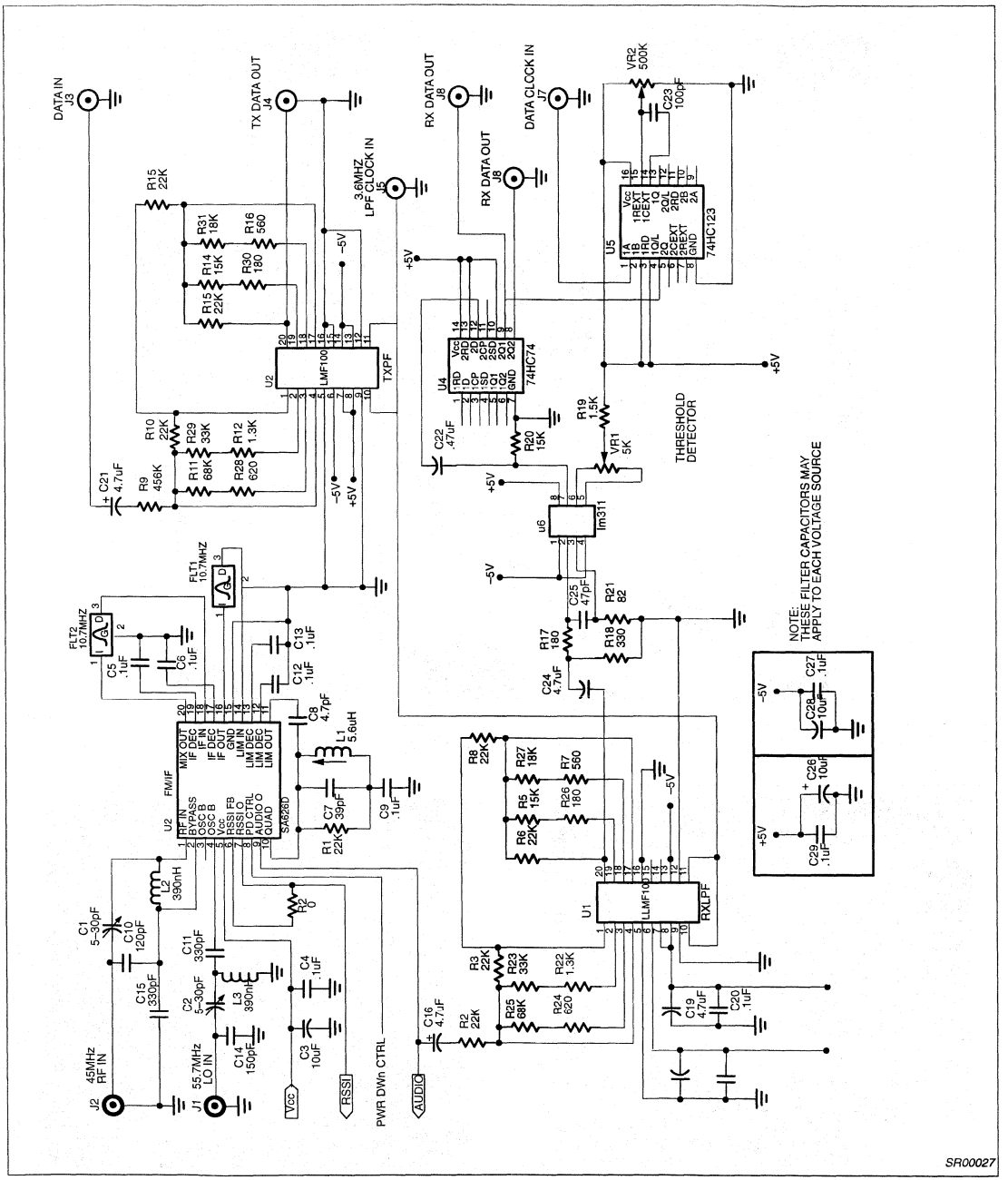

Figure 10. Circuit Diagram of the GMSK/GFSK Demoboard

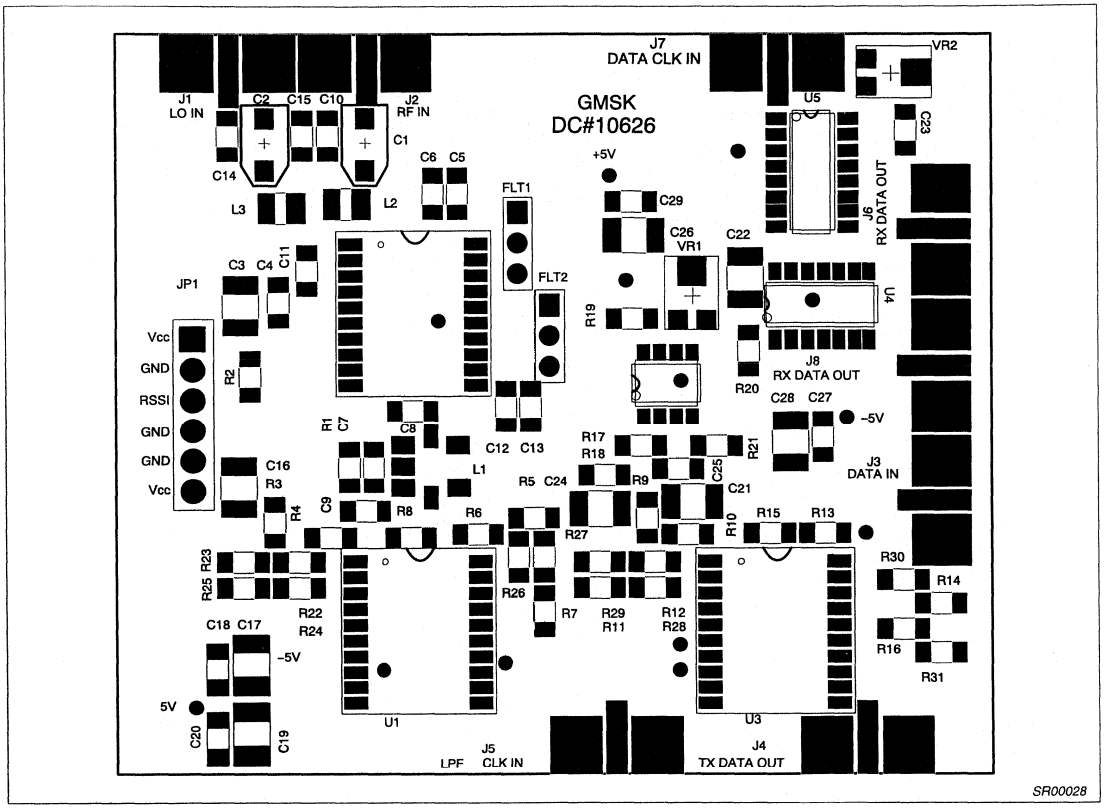

Figure 11. GMSK/GFSK Demoboard Components Layout

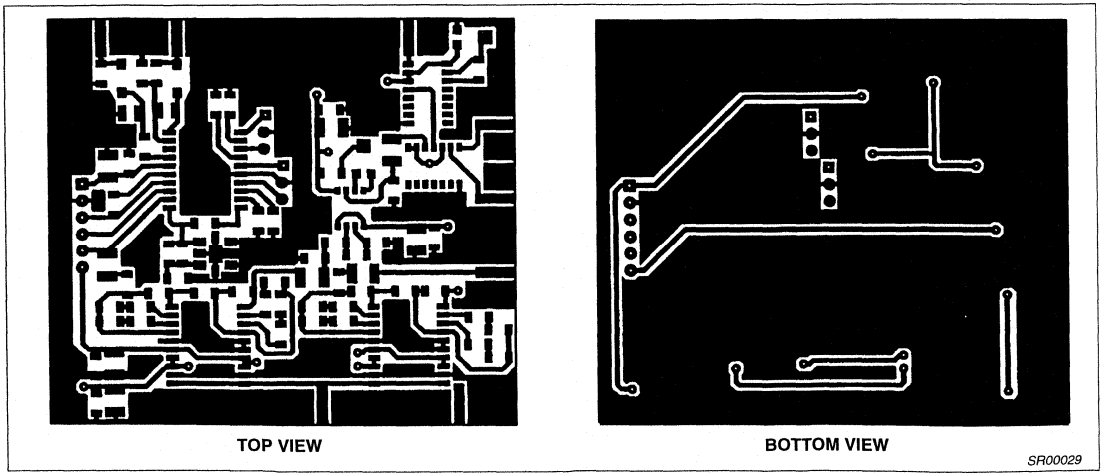

Figure 12. GMSK/GFSK Demoboard Layout

Table 3. Customer Application Component List for GMSK/GFSK Demoboard

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	4.7pF	50V	C8	Cap. cer. 1206 NPO ±0.25pF	Garrett	Rohm	MCH315A4R7CK
1	39pF	50V	C7	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A390JK
1	47pF	50V	C25	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A470JK
1	100pF	50V	C23	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG101J9BB0
1	120pF	50V	C10	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG121J9BB0
1	150pF	50V	C14	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG151J9BB0
2	330pF	50V	C11, C15	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG331J9BB0
8	0.1µF	50V	C4, C5, C6, C9, C12, C13, C18, C20	Cer. chip cap 1206 X7R ±10%	Garrett	Philips	1206R104K9BB0
1	0.47µF	35V	C22	Tant. chip cap B 3528 ±10%	Garrett	Philips	49MC474B035KOAS
3	4.7µF	10V	C16, C21, C24	Tant. chip cap B 3528 ±10%	Garrett	Philips	49MC475B010KOAS
3	10µF	10V	C3, C17, C19	Tant. chip cap B 3528 ±10%	Jaco	AVX	TAJB106K016R
	Option		C26, C27, C28, C29				
Surface Mount Variable Capacitors							
2	5-30pF		C1, C2	Trimmer capacitor	Kent Elect	Kyocera	CTZ3S-30C-W1
Surface Mount Resistors							
1	0Ω		R2	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
1	82Ω		R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW820E
3	180Ω		R17, R26, R30	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW181E
1	330Ω		R18	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW331E
2	560Ω		R7, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
2	620Ω		R24, R28	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW621E
2	1.3kΩ		R12, R22	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW132E
1	1.5kΩ		R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW152E
3	15kΩ		R5, R14, R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW153E
2	18kΩ		R27, R31	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW183E
1	20kΩ		R1	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW203E
7	22kΩ		R3, R4, R6, R8, R10, R13, R15	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW223E
2	33kΩ		R23, R29	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW333E
1	56kΩ		R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW563E
1	68kΩ		R11, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW683E
Surface Mount Variable Resistors							
1	5kΩ		VR1	SM RES TRIM, 1 TRN ±20% J-H	Garrett	Philips	ST-4TA502
1	500kΩ		VR2	SM RES TRIM, 1 TRN ±20% J-H	Garrett	Philips	ST-4TA504
Surface Mount Inductors							
2	0.39µH		L2, L3	Chip Inductors-1800CS series	Coilcraft	Coilcraft	1800CS-391
Surface Mount Variable Inductors							
1	5.6µH		L1	Adjustable SM Inductor 5CCD type	Digikey	TOKO	TKS2251
Filters							
2	10.7MHz		FLT1, FLT2	10.7MHz IF filter 110kHz±30kHz	Murata	Murata	SFE10.7MHY-A
Surface Mount Integrated Circuits							
2			U1, U3	Switched capacitor filter	Hamilton	National	LMF100CIWM
1			U2	Low voltage mixer FM IF high RSSI	Philips	Philips	SA626D
1			U4	Dual D-type flip-flop	Philips	Philips	74HC74
1			U5	Dual re-triggerable monostable	Philips	Philips	74HC123
1			U6	Voltage comparator	Philips	Philips	LM311
Miscellaneous							
8			J1, J2, J3, J4, J5, J6, J7, J8	SMA gold connector	Newark	EF Johnson	142-0701-801
1			JP1	6-pins header straight	Mouser	Molex-Waldem	538-22-05-2061
1				Printed circuit board	Philips	Philips	GMSK/DC#10626
78 Total Parts							

An FM/IF system for DECT and other high speed GFSK applications: SA639

AN1998

Author: Yanpeng Guo

ABSTRACT

A Philips low voltage high performance monolithic FM/IF system, the SA639 is introduced to meet the increasing demand for high speed digital wireless PCS applications. In order to assist the system design, a SA639-based performance evaluation board has been developed according to the Digital European Cordless Telephone (DECT) specifications. This application note presents a detailed description of the SA639 FM/IF system, the evaluation board, and design information including circuit diagram, component list, and the board layout. The experimental performance evaluation procedures, measured bit error rate (BER), sensitivity to frequency off-set, and sensitivity to FM deviation variation of this system are also presented. Results indicate that the low voltage SA639 FM/IF system provides superior performance for high speed digital wireless applications.

I. INTRODUCTION

To achieve the goal of wireless personal communications, allowing users access to the capabilities of the global communications network at any time without regard to location and mobility, cellular and cordless telephony have been taken as two major approaches. Cellular systems are evolving towards smaller cells (microcells) and lower power levels to provide higher overall capacity. Cordless telephones have evolved from home appliances towards wide spread "universal" low power personal communications systems. With the advent of digital cordless telephony, cordless systems with enhanced functionality have been developed that can support higher data rates and more sophisticated applications such as wireless private branch exchanges (WPBX) and public-access Telepoint systems. One of the first digital cordless standards is the Digital European Cordless Telecommunications (DECT) system, a pan-European standard designed to connect all of Europe with a common digital cordless system. DECT is also a flexible standard for providing a wide range of services in small cells.

In this application note, the SA639, a Philips low voltage FM/IF system with several important features such as post filter amplifier and active data switch, is proposed for DECT and other high speed digital wireless applications. A SA639-based DECT receiver evaluation board has been developed. Detailed description of the SA639 FM/IF system, structure of the evaluation board, design information, and experimental evaluation results are presented.

II. REVIEW OF DECT STANDARD

DECT is designed as a flexible interface to provide cost-effective communications services to high user densities in small cells. This standard is intended for the applications such as domestic cordless telephony, Telepoint, cordless PBXs, and Radio Local Loop (RLL). It supports multiple bearer channels for speech and data transmission (which can be set up and release during a call), hand over, location registration, and paging. Functionally, DECT is closer to a cellular system than to a classical cordless telephone. However, the interface to PSTN or ISDN remains the same as for a PBX or corded telephone. Table 1 is a summary of the key specifications of DECT and other digital cordless telephone systems.

DECT is based on Time Division Duplex (TDD) and Time Division Multiple Access (TDMA) with 10 carriers in the 1880 - 1900MHz band. Figure 1 illustrates the DECT TDD/TDMA frame structure.

The completed frame is 10ms in duration with 24 time slots. The first 12 slots are allocated for the transmission from base station to handsets, and the other 12 slots are for the transmission from hand sets to base station. Each slot is 417μs long with 480 bits. The first 32 bits is a "1010..." sequence for synchronization. The 32kb/s ADPCM CODEC is used for speech coding in DECT, which provides 320 bits during each 10ms frame. When a call is made, two slots (one is in the first 12 slots, the other is in the last 12 slots) are assigned to the user for transmit and receive.

Gaussian filtered FSK (GFSK) modulation scheme is employed in DECT. GFSK is a premodulation Gaussian filtered digital FM scheme. Figure 2 shows the block diagram of a GFSK modulator. The advantages of GFSK can be summarized as follows.

i) Constant envelope nature: this allows GFSK modulated signal to be operated with class-C power amplifier without introducing spectrum regeneration. Therefore, lower power consumption and higher power efficiency can be achieved.

ii) Narrow power spectrum: narrow mainlobe and low spectral tails keep the adjacent channel interference to low levels and achieve higher spectral efficiency.

iii) Non-coherent detection: GFSK modulated signal can be demodulated by the limiter/discriminator receiver as shown in Figure 3. This simple structure leads to low cost GFSK receivers.

III. THE SA639 FM/IF SYSTEM

The SA639 is a low-voltage high performance monolithic FM/IF system with high speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, fast RSSI op amps, post detection filter amplifier, and a data switch. The block diagram of SA639 is presented in Figure 4. The SA639 was designed specially for high data rate portable communications applications and will function down to 2.7V. The data output provides a minimum bandwidth of 1MHz to demodulate high speed data, such as in DECT applications. Figure 5 presents the quad tank S-curve of SA639, which indicates the linear range to be about 2MHz. The measured RSSI characteristics of SA639 is presented in Figure 6. With more than 75dB dynamic range, the SA639 RSSI rise/fall time is 0.8/2.0ms at -45dBm RF level.

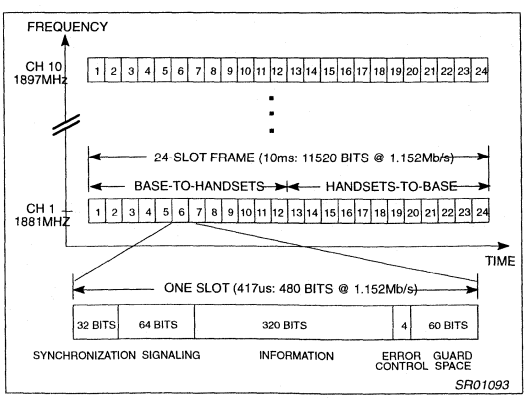

Figure 1. DECT TDD/TDMA Frame Structure

An FM/IF system for DECT and other high speed GFSK applications: SA639

AN1998

Table 1. Summary of Digital Cordless Standards

Standard	CT2/CT2+	DECT	PHS	PACS
Region	Europe/Canada	Europe	Japan	USA
Frequency Band (MHz)	CT2: 864–868 CT2+: 944–948	1880–1900	1895–1918	Tx: 1850-1910 Rx: 1930-1990
Duplex	TDD	TDD	TDD	FDD
Multiple Access	TDMA	TDMA	TDMA	TDMA
Number of Channels	40	10	77	16 pairs
Channel Spacing (kHz)	100	1728	300	300
Users/Channel	1	12	4	8/pair
Modulation	GFSK (FM dev. 14-25kHz)	GFSK (FM dev. 288kHz)	π/4-DQPSK	π/4-DQPSK
Bit Rate	72kb/s	1.152Mb/s	384kb/s	384kb/s
Speech Coding	32kb/s ADPCM	32kb/s ADPCM	32kb/s ADPCM	32kb/s ADPCM
Frame Duration	2ms	10ms	5ms	2.5ms
Peak Power	10mW	250mW	80mW	200mW

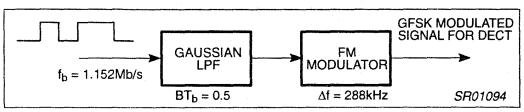

Figure 2. Block Diagram of GFSK Modulator

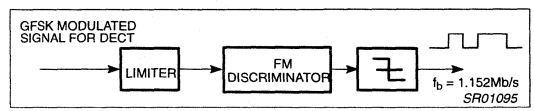

Figure 3. Block Diagram of GFSK Demodulator

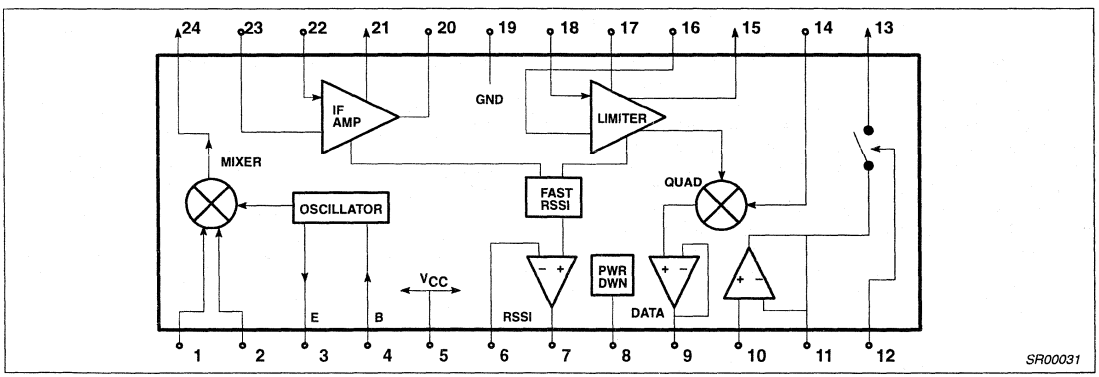

Figure 4. Block Diagram of the SA639 FM/IF System

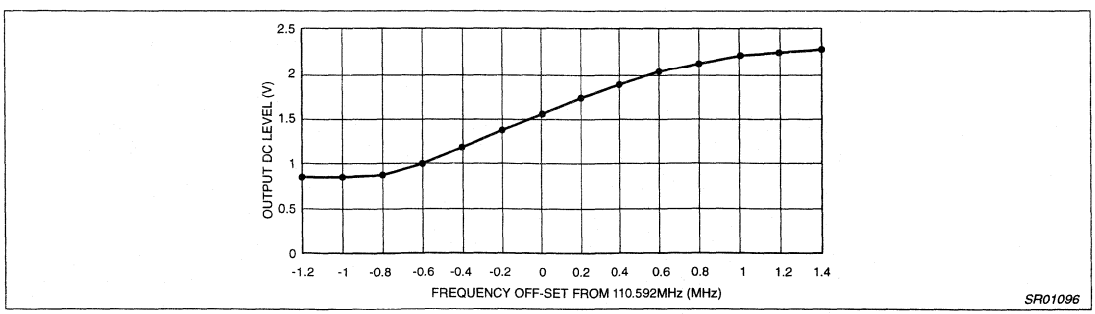

Figure 5. Quad Tank S-Curve of SA639 Board

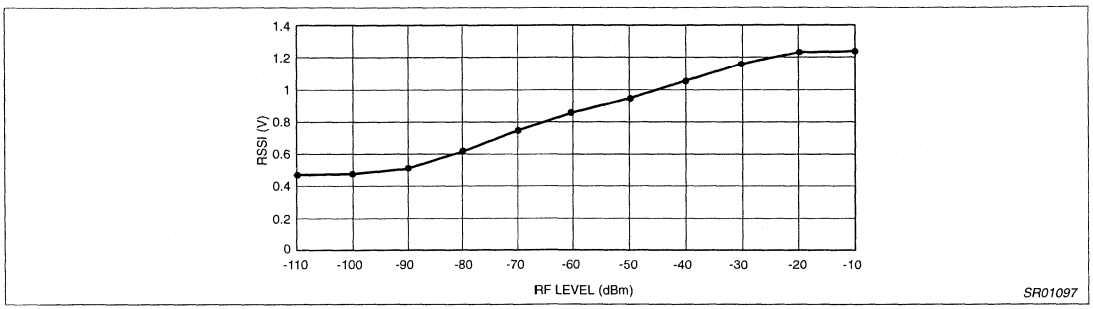

Figure 6. Measured RSSI Characteristics of SA639

The post-detection amplifier may be used to realize a group delay optimized low pass filter. The filter amplifier provides 0dB gain and has a 3dB bandwidth of at least 4MHz in order to keep its frequency response influence on the filter group delay characteristics at a minimum. It can be configured for Sallen & Key low pass with Bessel characteristic and a 3dB cut frequency of about 800kHz.

The SA639 incorporates an active data switch to derive the data comparator reference voltage by means of routing a portion of data signal to an external integration circuit. The data switch is typically closed for 10ms in the course of 32 bit synchronization sequence, and is open otherwise. The time constant of the external integration circuit is about 5 to 10ms. This active switch provides excellent tracking behavior over a DC input range of 1.2 - 2.0V. The slew rate is better than 1V/ms. When the switch is opened, the output is in a tri-state mode with a leakage current of less than 100nA. This reduces the discharge of the external integration circuit. As compared to other similar FM/IF chips, another advantage of SA639 is that during power down mode (between data bursts) the data switch will output a reference of about 1.6V to maintain a charge on the external RC circuit. This idea helps extract the reference voltage for the external capacitor in a shorter time and improves the accuracy of the voltage on the capacitor. The overall system is well suited for battery operated high quality products in digital wireless personal communications. Detailed specifications of SA639 can be found in [3].

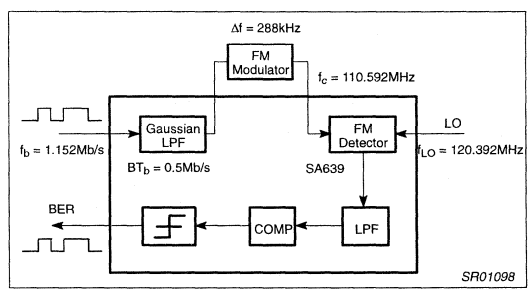

Figure 7. Structure of the SA639 GFSK Evaluation Board

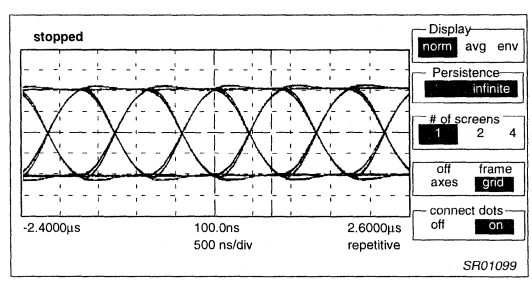

Figure 8. Measured Eye-Diagram at the Output of Tx Gaussian LPF

IV. STRUCTURE OF THE SA639 EVALUATION BOARD

A SA639-based evaluation board has been developed based on DECT specifications. The structure of this board is illustrated in Figure 7 together with a VCO/FM discriminator based GFSK modem (modulator/demodulator). The demo board contains the entire demodulator as well as the Gaussian low-pass filter (LPF) for the modulator. The DECT modulated signal, therefore, can be generated either by a standard DECT signal generator, or by sending a 1.152Mb/s data stream to the on-board Gaussian LPF (BTb = 0.5), then applying the filtered base band wave form to a FM signal generator with a modulation index of 0.5. The output is then the GFSK modulated signal (DECT). The schematic of the Gaussian LPF can be found in Figure 14. Baseband eye-diagram at the output of the Gaussian LPF is presented in Figure 8.

At the output of the limit/frequency discriminator, the post-detection amplifier is configured as a Sallen & Key LPF to eliminate noise. For the convenience of operation, the evaluation board is designed in such a way that the reference voltage for the data comparator can be obtained either from the switch controlled DC extraction circuit, or directly from the power supply. If the DECT Burst Mode Control circuit is available, the active data switch can be used to extract and track DC level during the synchronization sequence. Otherwise the DC reference can be obtained from the power supply and manually adjusted for the comparator operation.

A 2-level threshold detector with sampling time adjustment circuit is implemented on the board for data regeneration. The phase of data clock can be adjusted manually through a monostable multivibrator (74HC123) to achieve the optimal sampling time. The demo board is initially adjusted for a bit rate of 1.152Mb/s. If a different data rate

is used, the sampling time has to be re-adjusted. The output of the threshold detector is the regenerated binary data, which can be sent to a data error analyzer to evaluate the BER performance.

The symbol timing recovery (STR) circuit is not implemented on this evaluation board. Transmit data clock either hard-wire connected from the transmitter or from a separate STR circuit is required for the operation. The performance measurements presented in this application note were conducted with hard-wire connected data clock. However, BER degradation caused by STR should not be more than 1dB [6].

This SA639-based GFSK demo board is designed with DECT specifications at RF frequency of 110.592MHz, LO frequency of 120.392MHz, and intermediate frequency of 9.8MHz. For different frequency plan applications, the step-by-step matching circuit design procedure can be found in [1]. Tables 2 and 3 present the SA639 RF/LO input impedance and Mixer/Limiter output impedance over frequency, respectively.

Table 2. SA639 RF/LO Input Impedance Over Freq.

Frequency	RF Input	LO Input
50MHz	846Ω // 4.52pF	6900Ω // 4.07pF
110MHz	687Ω // 3.84pF	4900Ω // 4.09pF
240MHz	510Ω // 3.69pF	1900Ω // 4.22pF
500MHz	190Ω // 4.21pF	245Ω // 4.98pF

Table 3. SA639 Mixer/Limiter Output Impedance Over Freq.

Frequency	RF Input	LO Input
0.5MHz	395Ω // 20.2pF	438Ω // 14.5pF
10MHz	350Ω // 6.67pF	383Ω // 3.5pF
21MHz	339Ω // 4.58pF	393Ω // 2.04pF
50MHz	326Ω // 3.44pF	391Ω // 1.35pF

V. PERFORMANCE EVALUATION

Performance of this SA639 based DECT GFSK system including BER and sensitivity to frequency off-set and FM deviation variation is experimentally evaluated. Measurement procedures and the measured results are presented in this section.

Figure 9 illustrates the measurement set-up with the SA639 DECT evaluation board. A data error analyzer is employed to generate a pseudo random binary sequence (PRBS) with length of 10^9-1 at a data rate of 1.152Mb/s. This data sequence is sent to a DECT signal generator to generate a standard DECT modulated signal at 110.592MHz. Another signal generator is employed to provide an LO signal at 120.392MHz for the FM/IF system detection. The reference DC voltage for the data comparator is obtained from power supply for this evaluation. Data clock signal is directly from the data error analyzer. The sampling time is manually adjusted at the center of baseband eye diagram. Recovered data sequence is fed back to the Data Error Analyzer for BER measurement.

The BER measurement procedures can be summarized as follows.

- Build the measurement set-up as shown in Figure 9.
- Measure SINAD at the data output of SA639: RF = 110.592MHz, fm = 1kHz, Df = 288kHz; LO = 120.392MHz, -10dBm; the typical sensitivity for 12dB SINAD should be about -97dBm.
- Check SA639 output level: tune the quad tank circuit to have the least distorted eye-diagrams at the post-op. amp. output. The DC level should be about 1.4 - 1.7v.
- Check the DC reference for the comparator: set the reference voltage at the DC level of the op. amp. output by adjusting VR1 in Figure 14.
- Adjust sampling position: set the up edge of the clock at pin 11 of 74HC74 to be at the center of the eye-diagram at pin 2 of LM311B by adjusting VR2 in Figure 14.
- Measure BER with high RF level: set RF input signal level at -60 dBm; LO signal level at -10 dBm: error free.
- Measure BER vs. RF input level curve: RF level: -76 ~ -86 dBm, LO level: -10 dBm, at each point, at least 100 errors have to be measured.

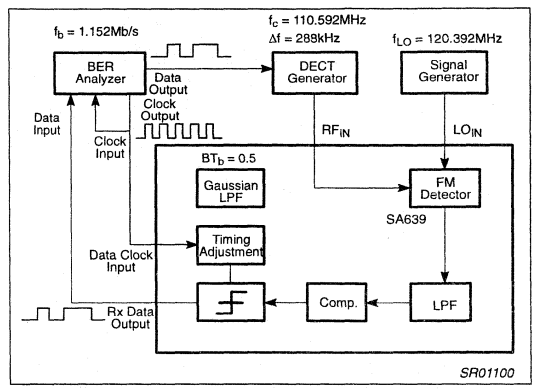

Figure 9. Block Diagram of the BER Evaluation Set-up

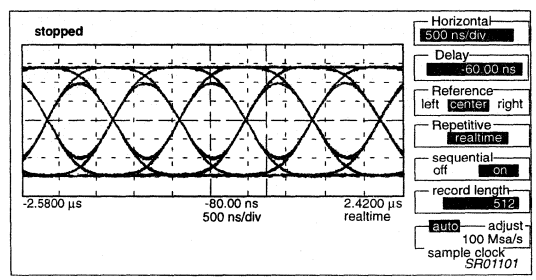

Figure 10. Recovered Eye-Diagram at the Output of SA639

The recovered baseband eye-diagram is shown in Figure 10, and the measured BER vs. RF input level is presented in Figure 11. It can be seen that about -83dBm RF power is needed to achieve the bit error rate of 10^{-3}. Since a typical front-end circuit has a better noise figure than FM/IF system, it is common to achieve more than 5dB signal-to-noise ratio gain by the front-end circuit. Therefore, with the SA639 FM/IF the overall system sensitivity could be better than -88dBm for the BER of 10^{-3}. Based on our measurements, by applying the Philips UAA2077AM 2GHz image rejecting front-end to the SA639 FM/IF system the overall system sensitivity is -91dBm for the BER of 10^{-3}. This performance compares very well to the DECT specifications for public access equipment (-86dBm for 10^{-3} BER).

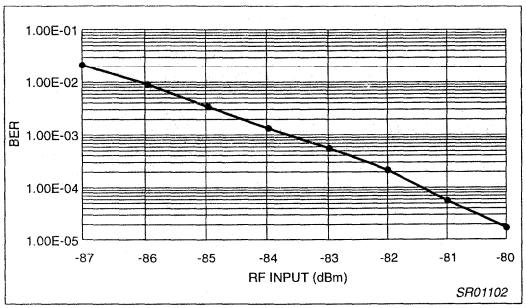

Figure 11. BER of the SA639 DECT Demoboard (RF: 110.592 MHz; LO: 120.392 MHz; fb: 1.152 Mb/s)

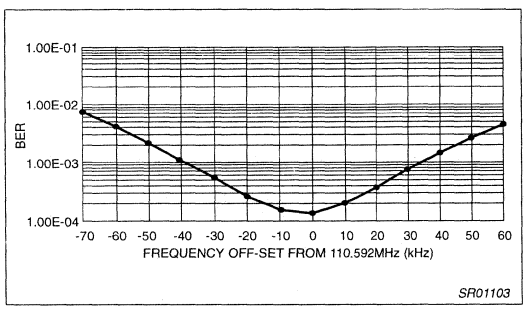

Figure 12. BER Degradation Caused by Frequency Off-Set (RF: -82dBm)

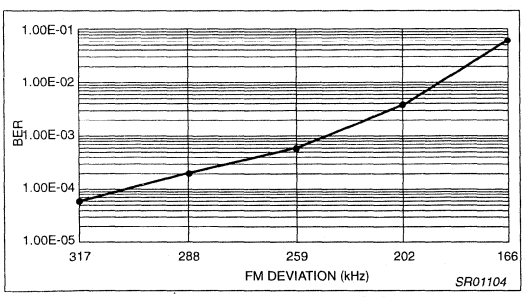

Figure 13. BER vs. FM Deviation (RF: 110.592 MHz, -82 dBm; fb: 1.152 Mb/s)

The performance degradation caused by frequency off-set and the sensitivity to FM deviation variation of this system are also evaluated. Figure 12 presents the measured BER vs. frequency off-set. Even with 50 kHz off-set, only minor degradation can be observed, and -82dBm RF level is enough for 10^{-3} BER. The sensitivity of this system to FM deviation variation is illustrated in Figure 13. Even with 10% deviation reduction (259kHz), less than -82dBm RF signal is needed to achieve the BER of 10^{-3}. These results indicate that the Philips SA639 FM/IF system provides superior performance for DECT and other high data rate GFSK applications.

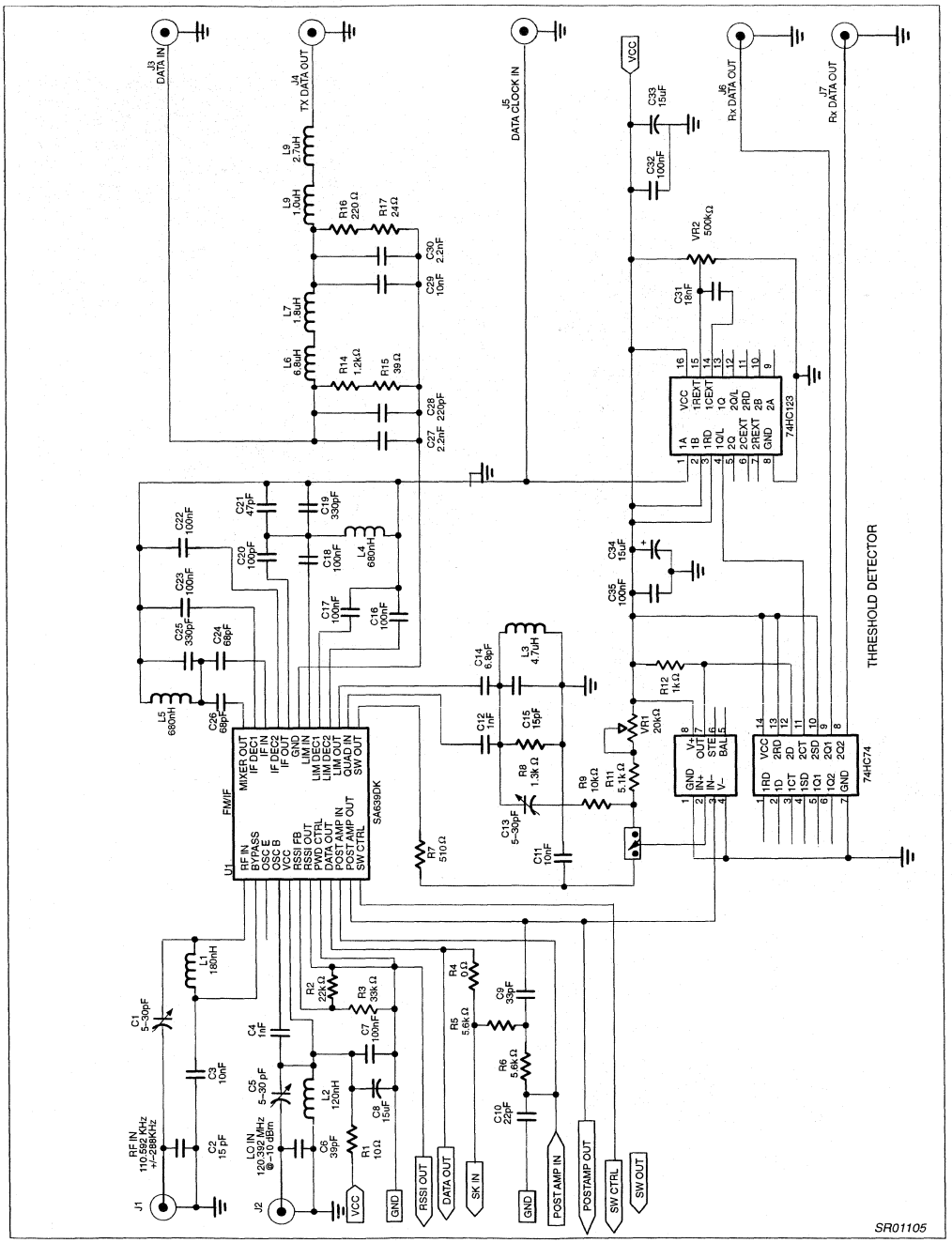

Figure 14. Schematic

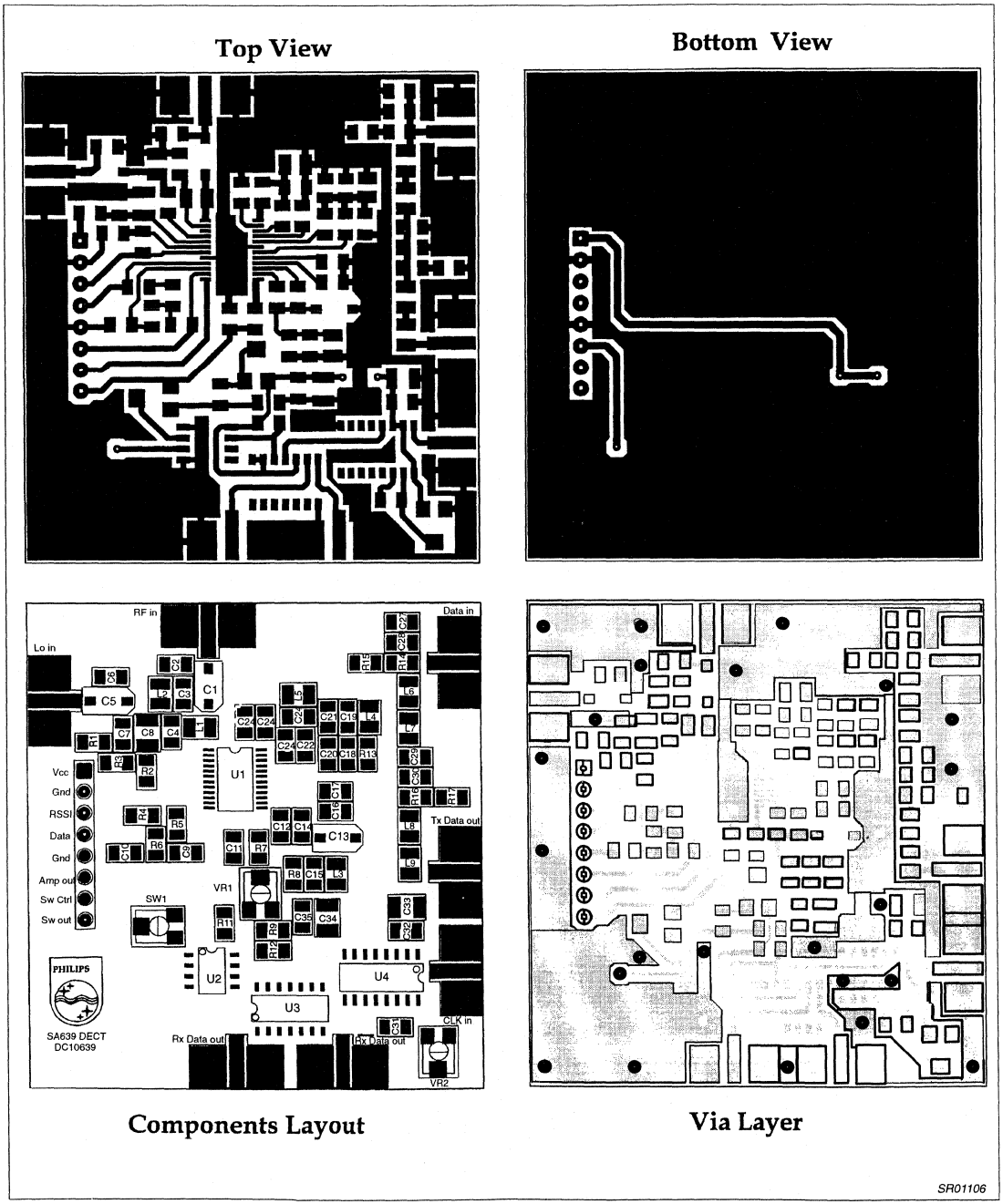

Figure 15. Board Layout

VI. CONCLUSIONS

A Philips low voltage high performance FM/IF system (SA639) based GFSK modem evaluation board is presented. Experimental performance evaluation including bit error rate (BER), sensitivity to frequency off-set, and sensitivity to FM deviation variation of this system has been conducted based on DECT specifications. Results indicate that a superior performance can be achieved with the Philips FM/IF systems for high speed digital wireless applications.

Table 4. Customer Application Component List for GMSK/GFSK Demoboard

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	6.8pF	50V	C14	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG689C9BB2
1	15pF	50V	C2, C15	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG150J9BB2
1	18pF	50V	C31	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG180J9BB2
1	22pF	50V	C10	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG220J9BB2
1	33pF	50V	C9	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG330J9BB2
1	39pF	50V	C6	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG390J9BB2
1	47pF	50V	C21	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG470J9BB2
2	68pF	50V	C24, C26	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG680J9BB2
2	100pF	50V	C18, C20	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG101J9BB2
1	220pF	50V	C28	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG221J9BB2
1	330pF	50V	C19, C25	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG331J9BB2
3	1000pF	50V	C4, C12	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG102J9BB2
2	2200pF	50V	C27, C30	Cap. cer. 1206 NPO ±5%	Garrett	Philips	1206CG222J9BB2
3	0.01µF	50V	C3, C11, C29	Cer Cap 1206 X7R ±10%	Garrett	Philips	12062R103K9BB2
7	0.1µF	50V	C7, C16, C17, C22, C23, C32, C35	Cer Cap 1206 X7R ±10%	Garrett	Philips	12062R104K9BB2
3	15µF	10V	C8, C33, C34	Tantalum Capacitor Chips	Garrett	Philips	49MC106C006KOAS
Surface Mount Variable Capacitors							
3	5-30pF		C1, C5, C13	Trimmer capacitor	Kent Elect	Kyocera	CTZ3S-30C-W1
Surface Mount Resistors							
1	0Ω	50V	R4	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW000E
1	10Ω	50V	R1	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW100E
1	24Ω	50V	R17	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW240E
1	39Ω	50V	R15	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW390
1	220Ω	50V	R16	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW221E
1	510Ω	50V	R7	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW511E
1	560Ω	50V	R13	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW561E
1	1kΩ	50V	R12	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW102E
1	1.2kΩ	50V	R14	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW122E
1	1.3kΩ	50V	R8	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW132E
1	5.1kΩ	50V	R11	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW512E
2	5.6kΩ	50V	R5, R6	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW562E
1	10kΩ	50V	R9	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW223E
1	22kΩ	50V	R2	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW223E
3	33kΩ	50V	R3	Res. chip 1206 ±5%	Garrett	Rohm	MCR18JW333E
Surface Mount Variable Resistors							
1	20kΩ	50V	VR1	Trimmer Resistor .25W ±20%	Garrett	Philips	ST-4TA203
1	500kΩ	50V	VR2	Trimmer Resistor .25W ±20%	Garrett	Philips	ST-4TA504
Surface Mount Switch							
1	SPDT		SW1	4mm Selector Switch	Garrett	Philips	CS-412YTA
Surface Mount Inductors							
1	120nH		L2	Chip Inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-331XKBB
1	180nH		L1	Chip Inductor 1008 ±10%	Coilcraft	Coilcraft	1008CS-331XKBB
2	680nH		L4, L5	Chip Inductor 1008 ±10%	Digikey	TOKO	380NB-R68M
1	1.8µH		L7	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-1R8K
1	2.7µH		L9	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-2R7K
1	4.7µH		L3	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-4R7K
1	6.8µH		L6	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-6R8K
1	10µH		L8	Chip Inductor 1210 ±10%	Garrett	J.W. Miller	PM20-100K

Table 4. Continued

Surface Mount Integrated Circuits							
1		5V	U1	FM IF with filter switch	Philips	Philips	SA639
1		5V	U2	Voltage comparator	Philips	Philips	LM311B
1		5V	U3	Dual D-type flip-flop	Philips	Philips	74HC74
1		5V	U4	Dual re-triggerable multivibrator	Philips	Philips	74HC123
Miscellaneous							
7			J1, J2, J3, J4, J5, J6, J7	SMA gold connector	Newark	EF Johnson	142-0701-801
1			JP1	8-pins header straight	Mouser	Molex	538-22-03-2081
1				Printed circuit board	Excel	Philips	DC10639
78 Total Parts							

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Techniques for optimizing UHF front–end integrated circuits

AN2000

Author: Randall Yogi

ABSTRACT

This application note discusses S-parameter theory and applications and a method for obtaining device noise parameter data for the SA621 and SA611 UHF front-end integrated circuits. These devices are high performance, low-power communications systems, optimized over the 800-1000MHz frequency range. The SA621 contains a low noise amplifier (LNA), mixer and voltage controlled oscillator (VCO), while the SA611 is a simplified version containing only the LNA and mixer. This application note will focus primarily on matching the LNA input and output to achieve stability and optimal gain using S-parameter data and related calculations. Discussed is a procedure developed for obtaining device noise parameters without the need for an automated data-acquisition setup. In addition, performance trade-offs for the LNA, mixer, and VCO circuits are addressed.

INTRODUCTION

The high frequency communication industry is growing so rapidly that the design phase of product development is becoming shorter and shorter. Time-to-market is one of the critical factors in the success or failure of a product. Given that, long periods of experimentation are no longer feasible, designers need quick and reliable ways to evaluate integrated circuits to decide which parts are best suited for their products.

One way to reduce trial-and-error experimentation is by judiciously using S-parameters. In order to optimize a design, accurate S-parameters may need to be taken when not available from published data sheets. Through use of these measurements, stability can be determined and optimal gain achieved. Another significant way which design uncertainties can be reduced is by an experimental noise figure procedure capable of producing accurate results when automated data-acquisition equipment is unavailable. This application note presents and discusses S-parameter techniques that can be readily applied using a hand-held scientific calculator. This is particularly useful for obtaining desired, first order design approximations. Later in the application note trade-offs for optimizing particular aspects of front-end performance are presented in regards to the LNA, mixer, and VCO circuits of the SA611 and SA621.

SA621/SA611 LNA AND S-PARAMETERS

To prepare the reader for the examples to follow, a short description of the SA621/SA611 is presented. The LNA performance of the SA621 and SA611 are virtually identical. They have an average gain of 15dB with an achievable noise figure of approximately 1.7dB, and an input IP3 of –7dBm over the Advanced Mobile Phones System (AMPS) receive frequency range (869–894MHz). The LNA also performs well in the Industrial, Scientific and Medical (ISM) band (902–928 MHz.).

S-parameters play a critical role in designing for optimum gain and noise figure performance. Understanding how they are obtained and what to do with them can greatly decrease the experimental work necessary to make the LNA function properly. Knowing exactly where data sheet S-parameters are measured is the first step in applying them. The SA621/SA611 data sheet records typical measurements taken at *the pins of the IC*. They were obtained using a calibration board designed specifically for this purpose (Figure 1). Thus, any matching networks will refer to an actual pin connection on the IC. Measurements were made using a Hewlett Packard network analyzer (HP8753D) to automatically log data over a swept range from 100 to 1200 MHz. This instrument measures reflection coefficients at the ends of its calibrated coaxial connection points. These points are connected to the IC pins through SMA connectors and short PCB microstrip transmission lines. Time delays associated with these connectors and lines at the input and output (Figure 2 a) were rotated out using the "Port Extensions" function located in the "Calibration" menu of the HP8753D. Open and short termination results were observed with no chip on the board. If the microstrip transmission line and its associated connector (input or output) have negligible effect on each measurement over this frequency range, then the pad is open circuited and the rotated display should ideally be a single point on the outermost circle of the Smith Chart at R = ∞ (Figure 2 b). When the pad is shorted a similar point would be observed at R = 0. Following this port extension calibration, a chip was then soldered onto the calibration board and actual S-parameter data automatically gathered. Note that these parameters cannot be obtained from the demonstration(demo) board available from Philips Semiconductors because the external matching networks and associated transmission lines are in the way.

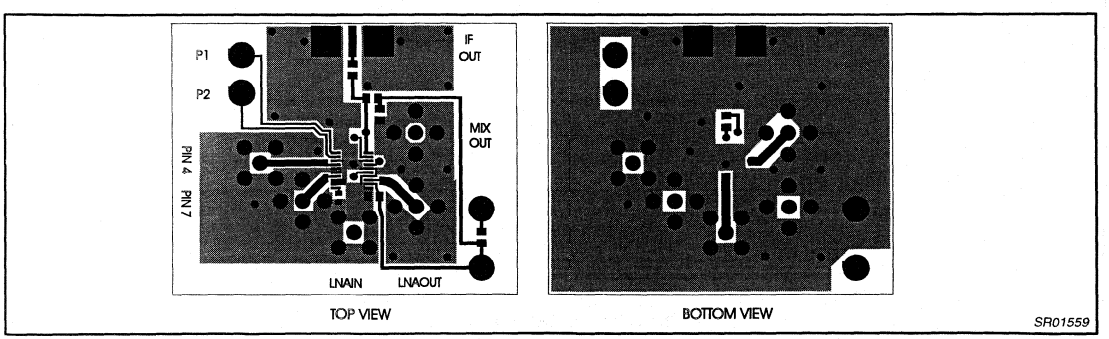
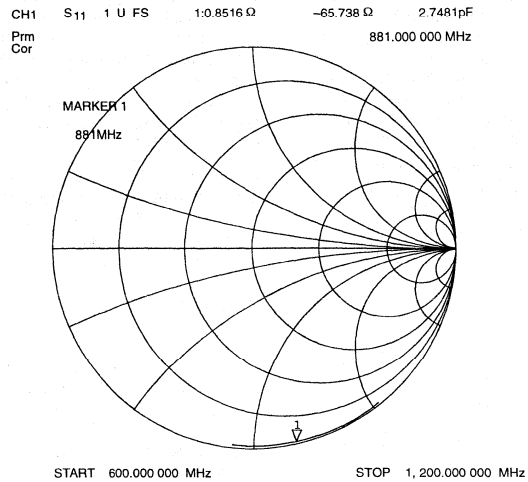
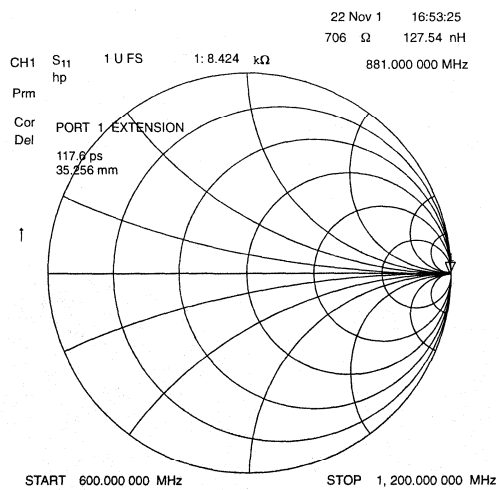


Figure 1 . Calibration Board Layout



A. OUTPUT BEFORE ROTATION

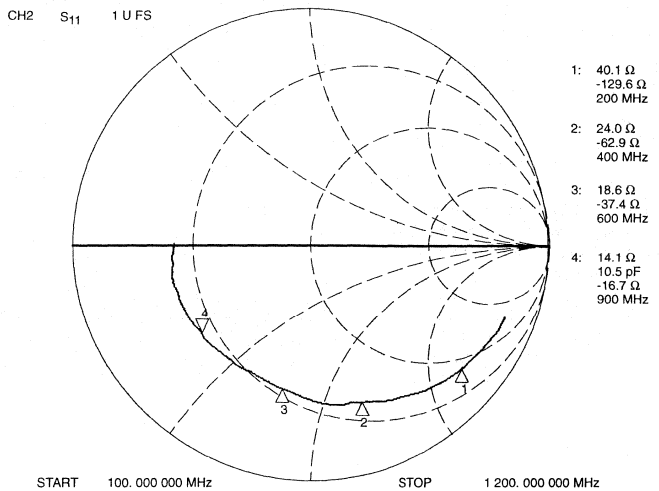


B. OUTPUT AFTER ROTATION

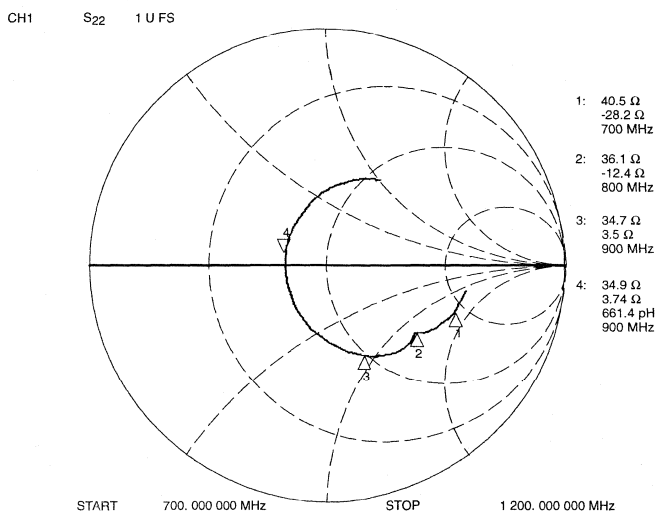
SR01560

Figure 2 . Network Analyzer Calibration

Measured LNA input and output S-parameters (S11 and S22) are shown below (Figures NO TAGa and NO TAGb). A full set of S-parameter data is available in the SA621 and SA611 data sheets.



A. S11 DATA



B. S22 DATA

SR01252

Figure 3 . Measured LNA S11 and S22 Data

MAXIMUM GAIN

Data sheet S-parameters only inform us of the LNA's performance when the source and load terminations are 50 ohms. Since the input and output impedances of this device are not 50 ohms, some return loss will be associated with the mismatch to 50 ohms at each port. These losses can be eliminated simply by conjugately matching each of them to 50 ohms. The standard first-order equation describing the resulting maximum unilateral gain (G_{umax}) is given by (1.1a) below (many good references exist treating the theory and practice of S-parameters [1] and [2]).

$$G_{umax} = \frac{1}{1 - |S_{11}|^2} |S_{21}|^2 \frac{1}{1 - |S_{22}|^2}, \quad (S_{12} = 0) \qquad (1.1a)$$

This equation assumes the LNA is unconditionally stable when conjugately matched. The first and last terms describe the result of conjugately matching both the input and output ports respectively, thereby gaining back the losses due to mismatches present when S_{11} and S_{22} were determined at whatever impedance they were measured at, 50 ohms with the network analyzer in this case. It should be clear that if both LNA ports miraculously exhibited 50 ohm impedances, S_{11} and S_{22} would be 0 (no reflections!) and these terms would reduce to unity leaving only $|S_{21}|^2$, the unilateral transducer gain (remember, since scattering parameters are voltage ratios, they must be squared to obtain power). This term is an invariant property of the LNA itself that depends externally only on frequency but not source and load terminations. Finally, this is a *practical* equation since it assumes that the reverse transmission gain is zero (S_{12}= 0), making the device *unilateral*. Specifically, it does not account for the fact that when the load termination changes S_{11} also changes slightly and vice-versa.

The complete expressions for the non-unilateral or *bilateral* maximum gain G_{max} when $S_{12} \neq 0$ are:

$$G_{max} = \left|\frac{S_{21}}{S_{12}}\right| \left(K + \sqrt{K^2 - 1}\right) \text{ when } B < 0 \qquad (1.1b)$$

$$G_{max} = \left|\frac{S_{21}}{S_{12}}\right| \left(K - \sqrt{K^2 - 1}\right) \text{ when } B > 0 \qquad (1.1c)$$

where the parameter $B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$, and K and Δ are from (1.2) and (1.3) which are described next. G_{umax} is much easier to calculate, and usually is close enough to the actual value Gmax to warrant using it as a good approximation for design purposes.

STABILITY

As noted above, (1.1a,b,c) can only be used if the amplifier in question is stable when conjugately matched. Some amplifiers will oscillate with certain source and load terminations; these devices are *conditionally stable*. Otherwise, they are *unconditionally stable* since no passive source and load terminations exist that will cause oscillation. Stability is easily determined from measured S-parameters. This involves finding a stability factor *K*(scalar number) and Δ (a complex number), where

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}S_{12}|} = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}S_{12}|} \quad (1.2)$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (1.3)$$

If $K>1$, the device will be *at least* stable when simultaneously conjugately matched to 50 ohms, and Gumax or Gmax can then be found. If $K>1$ *and* $|\Delta|<1$, then the device is also unconditionally stable with any termination. Note that *K* only tells us whether the device is stable when conjugately matched to the same characteristic impedance used to obtain the measured S-parameters, usually 50 ohms. The SA621/611 LNA is unconditionally stable at all frequencies between 100 and 1200 MHz.

Conditionally stable devices require further analysis to determine regions on the Smith Chart where they are stable. This is done by determining classic *source* and *load* stability circles. Not only must their location and radii be determined, but also whether the regions inside or outside the circles constitute stable terminations. This treatment is beyond the scope of this application note and will not be discussed here. Those interested in an excellent and readable treatment should refer to [2] as a good example.

EXAMPLE 1

Example showing the LNA to be unconditionally stable at 870 MHz:

Substitute S-parameters from Table 1 below into stability equations (1.2) and (1.3). Note: S-parameter data are vector quantities having both magnitude and phase; therefore, care must be taken to use vector arithmetic where necessary in the equations given in this application note.

Table 1. S-Parameter Data at 870 MHz

$\|S_{11}\|$	∠°	$\|S_{12}\|$	∠°	$\|S_{21}\|$	∠°	$\|S_{22}\|$	∠°
0.596	–135.8	0.027	111.9	4.81	26.9	0.179	–175.1

Find $|\Delta|$ first, then stability factor *K*:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$$

$$|\Delta| = |0.596 \cdot 0.179 \angle(-135.8 - 175.1) - 0.027 \cdot 4.81 \angle(111.9 + 26.9)| = 0.168$$

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|}$$

$$K = \frac{1 + 0.168^2 - 0.596^2 - 0.179^2}{2 \cdot 0.027 \cdot 4.81} = 2.25$$

Since $K>1$ and $|\Delta|<1$, the LNA is unconditionally stable at 870 MHz.

Thus, the maximum unilateral gain can be found from (1.1a),

$$G_{umax} = \frac{1}{1 - |S_{11}|^2} |S_{21}|^2 \frac{1}{1 - |S_{22}|^2} = (1.551)\,(4.81)^2\,(1.033) = 37.1 = 15.69 \text{ dB}$$

and the bilateral gain from (1.1b,c), found by computer,

$G_{max} = 15.77$ dB.

These two results differ by less than 0.08 dB and show the value of the simpler unilateral form. Note also that gain measured by the network analyzer would be just $10\log(|S_{21}|^2) = 13.6$ dB. Thus, we conclude that without any matching (50 ohm source and load terminations) we can expect a gain of 13.6 dB, while the most obtainable under any matching conditions is about 15.8 dB.

GAIN AND NOISE CIRCLES

Gain Circles

Input gain and noise circles plotted on the Smith Chart greatly facilitate the design of input matching networks by graphically showing the designer the tradeoff between any particular gain and wanted noise figure. The use of input gain and noise circles to achieve this end is discussed next. With the calibration board, S-parameter data is accurately referred right to the pin of the IC. From the measured S-parameters, LNA gain can be calculated for *any* matching network attached to either the input or the output pins.

Consider the case when the input matching network has a source reflection coefficient Γ_S (scattering parameter looking *into* the *output* of the network connected to the LNA input pin) equal to the conjugate of the input reflection coefficient S_{11} (scattering parameter seen looking *into* the LNA input IC pin) (Figure 4).

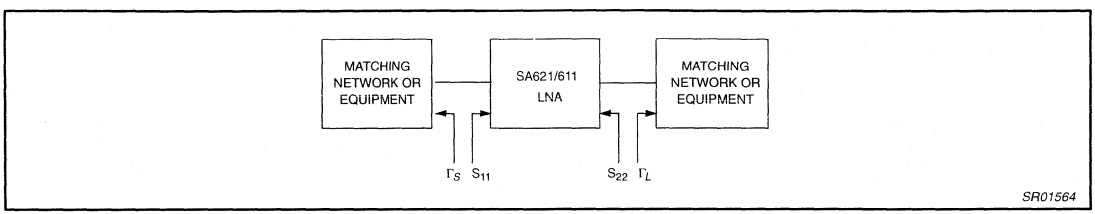


Figure 4 . Amplifier Setup

Thus,

$$\Gamma_S = S_{11}^*, \text{ unilateral device } (S_{12} = 0). \quad (1.4a)$$

$$\Gamma_S = \left(S_{11} + \frac{S_{12}S_{21}\Gamma_S}{1 - \Gamma_L S_{22}}\right)^*, \text{ bilateral device } (S_{12} \neq 0). \quad (1.4b)$$

This condition will plot Γ_S as a single point on the Smith Chart that can be used to design a suitable matching network to whatever source is driving the network's input, typically 50 ohms. Note that (1.4a) is quite simple and often differs little from (1.4b), especially for quick estimations. Comparison of (1.4a) and (1.4b) clearly shows the effect the load has on the LNA input when $S_{12} \neq 0$.

If a similar procedure is used to match the output, we have the unique situation described by equation (1.1a), where the LNA exhibits its maximum possible gain, G_{umax} If we stipulate that the output always remain conjugately matched, but introduce a deliberate input mismatch, the gain G will obviously be less than the maximum possible. For any particular $G<G_{max}$, many different Γ_S exist that will result in this same gain. It can be shown that the locus of these various Γ_S all lie on a single circle on the Smith Chart [1] [2]. Therefore, choosing any point on this circle defines a particular matching network all of which yield the same return loss or mismatch and thus the same gain G. In the time domain, this simply means the amplitude ratio of the forward and reverse traveling waves remains unchanged, but the phase between them will be different for each point on the circle.

Calculating input gain circles can be accomplished using either simplified unilateral equations or the more complicated bilateral forms. The former are useful for practical designs and can easily be done by any good engineering calculator. For an in–depth discussion into this topic refer to *Hewlett Packard Application Note 154* [1]. Reference [2] contains a well-developed complete treatment for an actual bilateral device like the SA621/SA611, with calculations that are most efficiently handled by a computer or calculator program.

Since the device will no longer be conjugately matched, (1.5) expresses the unilateral gain form of (1.1a) rewritten for *any* source or load terminations:

$$G_u = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{12}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \text{ where } G_u \text{ is always } < G_{umax}. \quad (1.5)$$

As stated earlier, the output will remain conjugately matched; only the input mismatch will be varied through Γ_S. For this special case, (1.5) becomes:

$$G_{su} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1}{1 - |S_{22}|^2} \quad (1.6)$$

Since any arbitrary value of G_{su} is between 0 and G_{umax}, solutions for Γ_S lie on a circle. We can choose any Γ_S and calculate its gain (G_{su}). So if we choose Γ_S along a 15.2dB circle, we would have a G_{su} of 15.2dB. Equations (1.7 – 1.9) from [1] determine where a gain circle can be found on the Smith Chart.

$$d_{ui} = \frac{g_{ui}|S11|}{1 - |S_{11}|^2(1 - g_{ui})} \angle S_{11}^*, \text{ gain circle center} \quad (1.7)$$

$$R_{ui} = \frac{\sqrt{1 - g_{ui}}\ (1 - |S_{11}|^2)}{1 - |S_{11}|^2\ (1 - g_{ui})}, \text{ gain circle radius} \quad (1.8)$$

where g_{ui} is a parameter expressing the gain circle's wanted gain G_{ui} normalized to G_{max}.

$$g_{ui} = G_{ui}(1 - |S_{11}|^2) = \frac{G_{ui}}{G_{umax}} \quad (1.9)$$

Note that d_{ui} is the distance from the center of the Smith Chart to the center of the gain circle along the conjugate S_{11}vector (S_{11}^*) and R_{ui} is the radius of the circle at that point.

EXAMPLE 2

Calculate and plot on the Smith Chart an input gain circle 0.5dB below the maximum gain for the SA621/SA611 at 870 MHz using the simplified unilateral assumption and compare it to the general bilateral case.

Begin by finding g_{ui}:

$$g_{ui} = G_i(1 - |S_{11}|^2) = \frac{G_i}{G_{umax}}$$

Choose $G_i = G_{umax} - 0.5$ dB = 15.7 dB – 0.5 dB = 15.2 dB.

Linearize the gain and find g_{ui}:

$$g_{ui} = 10^{\frac{15.2 - 15.7}{10}} = 0.891$$

Find the center, C_{ui}:

$$C_{ui} = \frac{g_i|S_{11}|}{1 - |S_{11}|^2\ (1 - g_{ui})} \angle S_{11}^*$$

$$C_{ui} = \frac{(0.891)\ (0.596)}{1 - (0.596)^2\ (1 - 0.891)} \angle - (-135.8)^\circ = \frac{0.530}{0.9614} \angle 135.8^\circ = 0.55 \angle 135.8^\circ$$

Find the radius, R_{ui}:

$$R_{ui} = \frac{\sqrt{1 - g_{ui}}\ (1 - |S_{11}|^2)}{1 - |S_{11}|^2(1 - g_{ui})} = \frac{\sqrt{1 - 0.891}\ (1 - (0.596)^2)}{0.9614} = 0.22$$

Thus, the center will be located at $0.55 \angle 135.8^\circ$ with radius of 0.22.

Compare this result with a computer derived bilateral center and radius for the same G_{max} – 0.5 dB gain circle [2]:

Gain Circle for G_{max}– 0.5 *dB* = 15.3 dB

$d_{ci} = 0.56 \angle 133.4^\circ$

$R_{ci} = 0.22$

The radii are equal with the centers differing only slightly and the gains by 0.1 dB. Now that all the information is found, a designer can draw these gain circles on the Smith Chart for visual comparison. Figure 5 shows these two gain circles plotted on the Smith Chart.

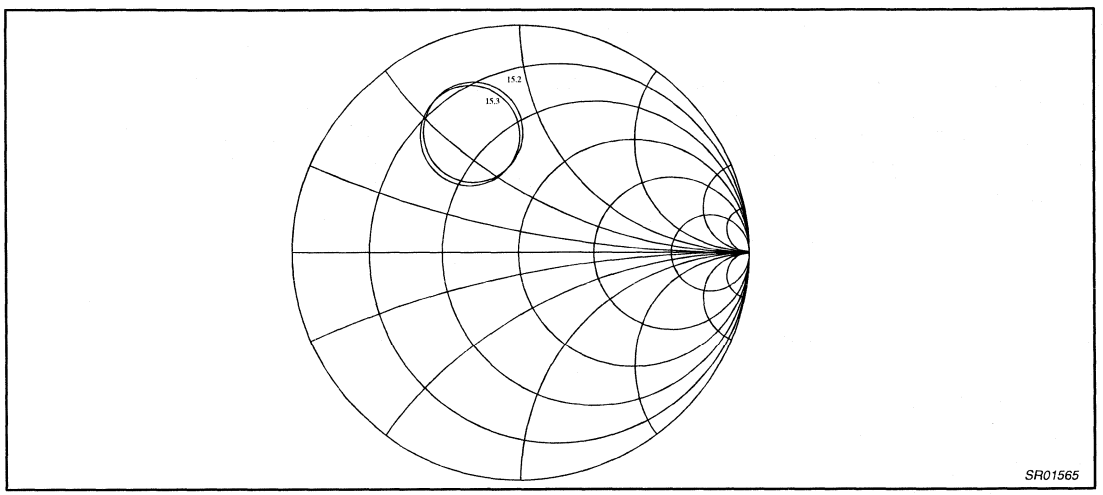


Figure 5 . Plot of Example–1: Unilateral (15.2dB) and Bilateral (15.3dB) Gain Circle

Noise Figure Circles

Noise factor *NF* is defined as the ratio of the signal-to-noise ratio at the input to the signal-to-noise ratio at the output,

$$NF = \frac{S_i/N_i}{S_o/N_o}$$

It is always greater than 1 for practical devices. Noise figure *F* is simply *NF* expressed in dB, *F = 10log(NF)*. Note that a perfect device having no internal noise generation has noise factor of 1 which yields a noise figure of 0 dB.

The LNA noise figure depends on the source impedance connected to its input port and frequency of operation. Further, the minimum noise figure, F_{min}, increases monotonically with frequency. Like most devices, F_{min} does not occur when the source is 50 Ωs. Thus, if a designer conjugately matches the input to realize maximum gain, observed noise figure *F* will be greater than F_{min}. How much greater? Similar to gain circles, noise circles can also be determined and plotted as an indispensable design aid to answering this question. Each circle describes a locus of source reflection coefficients Γ_s all having a constant $F>F_{min}$. Essentially, this is the same thing we did for gain circles except here the parameter is noise figure rather than gain.

Remember that gain circles are found by calculation employing the four basic S-parameters known at a particular frequency. Noise figure circles are based on three additional parameters: F_{min} at Γ_{min} and R_n. If these are not known and a designer does not have automated testing equipment, accurately determining them can be an exacting and time-consuming chore. An experimental method for obtaining them is presented in *Hewlett Packard Application Note 154* [1]. This method requires two basic measurements: One to determine what input reflection coefficient $\Gamma_s = \Gamma_{min}$ is required for best noise figure F_{min} and one additional point used to find the equivalent noise resistance R_n, described below in (1.10). The value and limitations of this method when applied to the LNA will be discussed later. After obtaining these quantities, any wanted noise circle may be found and plotted on the Smith Chart.

The following equation [1][2] expresses the fundamental relation between any noise figure *F* and the minimum noise figure F_{min} (at Γ_{min}) as a function of Γ_s.

$$F = F_{min} + 4r_n \frac{|\Gamma_s - \Gamma_{min}|^2}{|1 + \Gamma_{min}|^2 (1 - |\Gamma_{min}|^2)} \qquad (1.10)$$

where

$$r_n = \frac{R_n}{Z_o} \qquad (1.11)$$

F	noise figure ≥ F_{min}
S	source reflection coefficient at F
F_{min}	minimum noise figure possible for the device
Γ_{min}	source reflection coefficient at minimum noise figure
R_n	equivalent noise resistance in Ohms
Z_o	characteristic impedance of system, usually 50 Ohms
r_n	normalized equivalent noise resistance

Note that R_n is a parameter having dimensions of Ωs. It is *not* the actual Thevenin source resistance required for minimum noise figure; that can be found from Γ_{min}. Rather, it is a scalar factor gauging the dependence of *F* on Γ_s. This should be evident by inspection of (1.10). Also, Smith Charts usually have the center normalized to be 1 Ω, so only normalized quantities can be plotted. Thus, the normalized equivalent noise resistance r_n must be found.

Once r_n is found, it is used with min and F_{min} to determine a family of circles representing different noise figures found by applying (1.13) and (1.14) for each one as follows.

$$C_{Fi} = \frac{\Gamma_{min}}{1 + N_i} \quad \text{noise circle center} \qquad (1.12)$$

$$R_{Fi} = \frac{1}{1 + N_i}\sqrt{N_i^2 + N_i\left(1 - |\Gamma_{min}|^2\right)} \quad \text{noise circle radius} \qquad (1.13)$$

where

$$N_i = \frac{F_i - F_{min}}{4r_n}\left[1 + \Gamma_{min}\right] \qquad F_i > F_{min} \qquad (1.14)$$

C_{Fi} determines where the noise circle is located, and is found by measuring C_{Fi} from the center of the Smith Chart along the vector $\angle C_{Fi}$. R_{Fi} is the radius of the circle then constructed at that point. Note that S_{12} does not appear in these equations (1.10 to 1.14), so they are applicable to both unilateral and bilateral devices.

The necessary parameters were determined using the following setup:

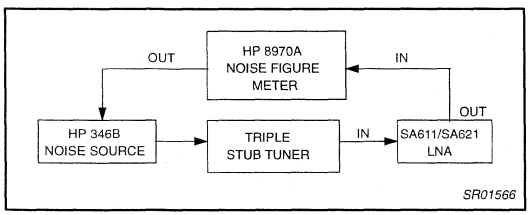


Figure 6 . Noise Circle Setup for Measuring Noise Figure

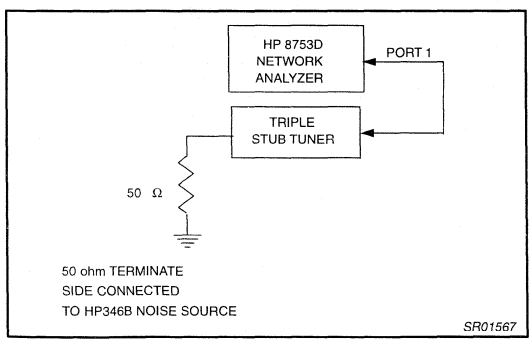


Figure 7 . Noise Circle Setup To Determine Location

The setup consists of two major pieces of equipment, a noise figure meter and a network analyzer and follows the general method discussed in *Hewlett Packard Application Note 154* [1]. The following is for those familiar with test procedures when measuring source reflection coefficients, Γ_S. The point to remember, here, is we are finding reflection coefficients looking *into* the *output* of the network that was connected to the *input* of the LNA. When we measure Γ looking into the LNA we label it S_{11}. When we measure Γ looking into the output of a network attached to the LNA's input, we label it Γ_S.

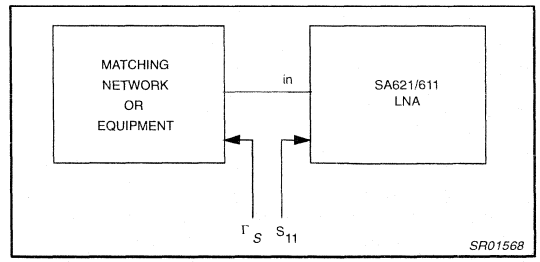


Figure 8 . Input Matching Network Showing Source Reflection Coefficient Γ_s and Input Reflection Coefficient S_{11}

1. Using the noise figure meter (Figure 6), find the minimum noise figure F_{min} of the device by carefully tuning the triple-stub tuner. Most noise figure meters express to 3 significant digits (e.g. 1.73 dB), so some physical interpolation of the stub elements may be necessary to set the triple-stub to a good estimate of where the minimum actually occurs. The reflection coefficient looking into the stub will be equal to Γ_{min}.
2. To measure Γ_{min}, connect a 50 Ω termination to the triple-stub tuner on the *same* side where the noise source was connected (Figure 7). Measure the reflection coefficient Γ of the tuner on a network analyzer. This will be the same as $F_{S} = F_{min}$. Note that on the HP8753D network analyzer is displayed when the format is "Polar". If the format is "Smith", then the display will give impedance Z even though the reflection coefficient plane is actually being displayed. The formulas require reflection coefficients not impedances. However, one can easily convert Z to by using the familiar relation:

$$\Gamma = \frac{Z_S - Z_L}{Z_S + Z_L} \qquad (1.15)$$

where, Z_s and Z_L are the source and load impedance, respectively. Because the HP network analyzer normalizes to 50 Ωs, the equation becomes:

$$\Gamma = \frac{Z_S - 1}{Z_S + 1} \qquad (1.16)$$

3. This procedure can be repeated for measurements of different noise figures, not just F_{min} .
4. Please keep in mind that *any* added lengths and attenuations need to be *accurately* accounted for. Depending on hardware, this can be tedious and complicated. For a simple example, if an SMA-to-SMA connector adaptor, often referred to as a barrel or through, is attached to the triple-stub tuner (that was not used when the stub was connected to the LNA) to obtain Γ_S, it will exhibit some time delay causing rotation on the Smith Chart as well as attenuation. Particular attention must be given to attenuations not accounted for when the noise figure apparatus was calibrated. Thus, attenuations of *all additional* RF hardware needs to be accounted for: including the stub-tuner, barrels, etc. Errors of 0.05 dB will typically be observable as changes in the diameter of the plotted noise circles.

EXAMPLE 3

Using the described noise circle setup, determine and plot the 2.0 dB noise circle on the Smith Chart for the SA621/SA611 at 881 MHz.

This is accomplished by using the triple-stub tuner to find all the necessary variables mentioned above. Following the HP procedure as a guide, we first find F_{min} and Γ_{min} using the noise figure meter and triple-stub tuner. Finding r_n requires another determination of any F and its associated Γ_s. Eqn. (1.10) is then solved for r_n, the named quantities substituted and r_n found. The HP procedure uses an especially simple and mathematically convenient way for finding this by letting $\Gamma_s = 0$; this occurs when the source termination is 50 Ω or just the noise figure reading *without* the triple-stub tuner. This makes sense, but unfortunately does not work well with the SA621/SA611 LNA. It turns out the two noise figures are quite close, F_{min} and F at 50 Ω, and each of these is expressed to only three significant figures; after linearizing their decibel forms, the resulting numerical error can be quite large. Further, the uncertainty in finding Γ_{min} with the stub tuner contributes to a larger overall uncertainty. Using this method, r_n has been observed to vary between 3 and 20 Ω, an unacceptably large variance. Philips has developed a better method to experimentally determine and verify these parameters.

The two re-written forms of (1.10), general and special cases respectively, solved for r_n, are given as:

$$r_n = \frac{(F - F_{min})\left(|1 + \Gamma_{min}|^2(1 - |\Gamma_S|^2)\right)}{4\left(|\Gamma_S - \Gamma_{min}|^2\right)} \qquad (1.17a)$$

$$r_n = \frac{(F - F_{min})\left(|1 + \Gamma_{min}|^2\right)}{4\left(|\Gamma_{min}|^2\right)} \qquad (1.17b)$$

Eqn. (1.17b) is used with the HP procedure, while (1.17a) the Philips procedure. Additional measurements are taken at random noise figures, ideally scattered around the Smith Chart, each yielding an associated r_n found by applying (1.12a) and multiplying by Z_0. Simple mean and variance or sample standard deviation are then calculated for the ensemble of r_n. The mean is taken to be the best estimate of r_n. Further, inspection of the r_n series can usually pin-point experimental errors when especially bad points turn up.

Assuming rotations and attentions have been properly accounted for (see point 4 above), the weak point in this procedure is the estimate of Γ_{min} since it is based on only one measurement subject to considerable error. This fact can only be appreciated by actually doing the laboratory measurement and getting a feel for the latitude one has in setting the triple-stub tuner at minimum noise figure. A further refinement is then possible using the measurement series of ordered pairs F and Γ_s for each r_n. A gradient search algorithm can be developed that finds a better estimate of Γ_{min} based on minimizing the ratio of the mean to variance of the ensemble r_n for each candidate Γ_{min}. Clearly, this is not suitable for hand calculator computations, but is easily done by a computer. First order approximations suitable for experimental design may be composed of several (at least 3) measurements for F and Γ_s to ascertain "whether we are in the ballpark" in the value settled upon for r_n. This is easily done on a hand calculator or with computer assistance using such common programs as Matlab.

Let's continue with this example using the Philips' method. A particular session in the screen room yielded the following actual set of experimental measurements using the calibration board for the LNA at 881 MHz:

Table 2. Noise Figure Measurements for Nine Samples

n	F(dB)	GAMMA	
SAMPLE	NOISE FIGURE	MAGNITUDE	ANGLE
1	1.60	0.170	126.1
2	4.53	0.737	15.0
3	3.15	0.551	–96.8
4	2.04	0.320	–131.1
5	2.45	0.428	–105.6
6	3.89	0.684	–102.2
7	3.38	0.706	–165.0
8	1.73	0.058	–91.0

Sample calculation using (1.17a for F = 2.03 dB at $\Gamma_S = 0.32 \angle -131.1°$,

$$r_4 = \frac{\left(\log^{-1}\left(\frac{2.03}{10}\right) - \log^{-1}\left(\frac{1.60}{10}\right)\right)\left(|1\angle 0° + 0.170\angle 126.1°|^2\left(1 - |0.32|^2\right)\right)}{4\left(|0.32\angle -131.1° - 0.170\angle 126.1°|^2\right)} = \frac{(0.150)(0.791)(0.898)}{4(0.131)}$$

$r_4 = 0.203\ \Omega$

$R_4 = r_4 Z_0 = (0.203)\ (50) = 10.2\ \Omega$

Using a computer, better estimates of Γ_{min} and r_n were found to be:

$\hat{\Gamma}_{min} = 0.174\angle 131.6°$, so $\hat{R}_n = 9.0\Omega$

To find the 2.0 dB noise figure circle we apply eqns.(1.12–1.14) using the non-optimized values for Γ_{min} and r_n for comparison purposes.

Find parameter N_i:

$$N_i = \frac{F_i - F_{min}}{4r_n}\left[1 + \Gamma_{min}\right]$$

$$N_i = \frac{\log^{-1}\left(\frac{2.0}{10}\right) - \log^{-1}\left(\frac{1.60}{10}\right)}{4\left(\frac{10.2}{50}\right)}\ |1\angle 0° + 0.170\angle 126.1°|^2 = \frac{(0.140)(0.791)}{0.816} = 0.135$$

Find where the noise circle is centered, C_{Fi}:

$$C_{Fi} = \frac{\Gamma_{min}}{1 + N_i} = \frac{0.170\angle 126.1°}{1.135} = 0.150\angle 126.1°$$

Find the noise circle's radius, R_{Fi}:

$$R_{Fi} = \frac{1}{1 + N_i}\sqrt{N_i^2 + N_i\left(1 - |\Gamma_{min}|^2\right)} = 0.881\sqrt{0.149} = 0.340$$

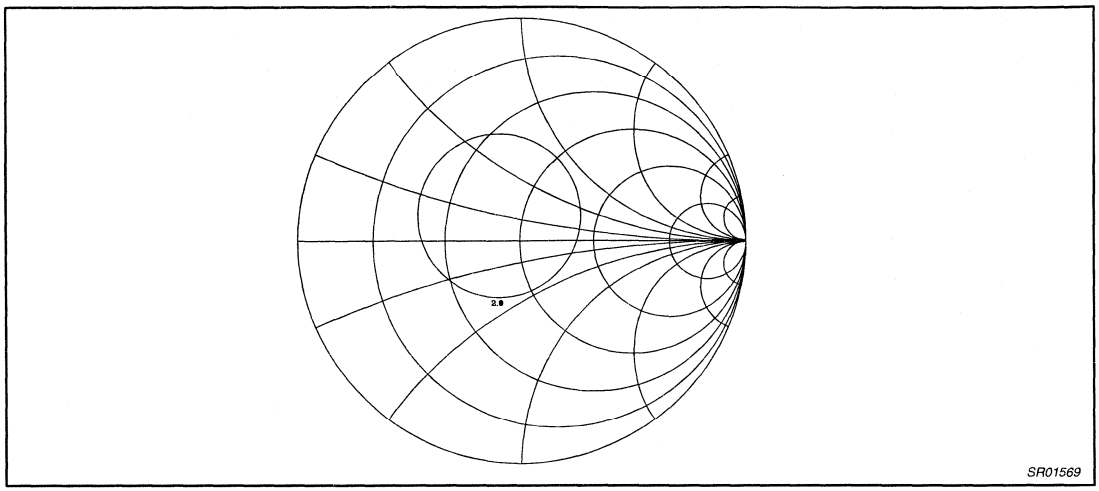


Figure 9 . 2.0 dB Noise Circle at 881 MHz

Piecing everything together

When gain circles, noise circles, and stability are all determined, the designer is ready to design a match to realize the optimal noise figure and gain combination for a specified application. Figure 10 shows the combined gain and noise circles on a single Smith Chart computed for 881 MHz. The noise circles were found from the data set in example 3 above with Γ_{min} and R_n optimized by a gradient search algorithm with the experimental data from Table 2. Compare especially the 2.0 dB noise circle with that found using the non-optimized Γ_{min} and r_n from example 3 shown in Figure 9 . The optimized location for this circle is $\hat{C}_{Fi} = 0.151 \angle 131.6°$ with a radius $\hat{R}_{Fi} = 0.361$

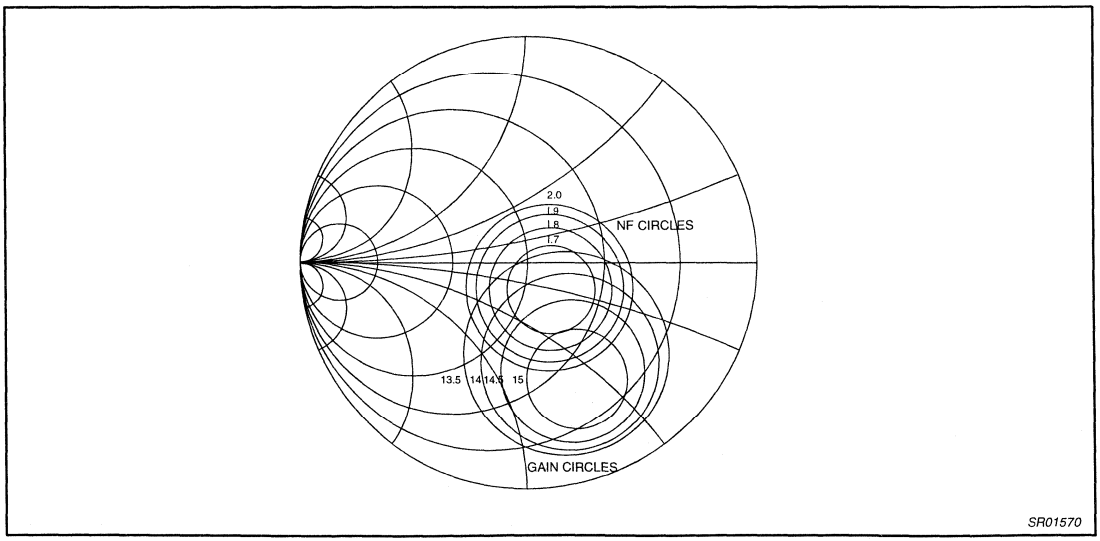


Figure 10 . Noise and Gain Circles at 881 MHz

Since the LNA is unconditionally stable at 881 MHz , there are no matching conditions that will cause it to oscillate. Therefore, interpreting the data in Figure 10 is easy: any input reflection coefficient Γ_S can be located as a point on the Smith Chart. The gain and noise circles tell us immediately what the expected gain and noise performance will be at this point, and we can proceed to design a suitable input matching network to realize this particular Γ_S.

Say a designer wants a noise figure of 1.8dB and a gain of 15dB when the source driving the LNA input is 50 Ω. On the Smith Chart, this noise figure and gain point are at approximately $Z_S = 31 + j20\ \Omega$. Since the LNA "sees" Γ_S, we begin from the center of the Chart, corresponding to the source of impedance of 50 Ω and move using suitable series or shunt elements to the Γ_S point. Thus, we choose components to match to the ending point (connected to the input of the LNA). Usually, more than one solution exists. In this case shunt C and series L are used. (Figure 11).

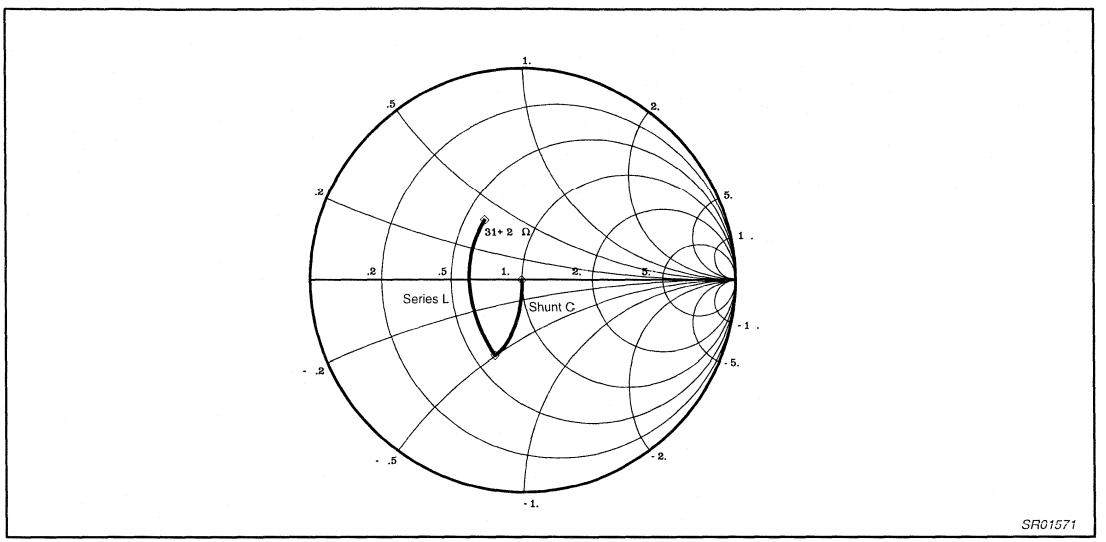


Figure 11 . Smith Chart Display of Matching

The circuit to match the input of the LNA is seen in Figure 11.

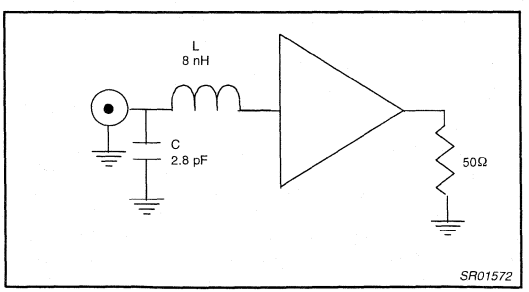


Figure 12 . LNA Input Matching

APPLICATION DEMONSTRATION BOARD (DEMO BOARD)

SA621/611 LNA

By conjugately matching the output port to 50 Ωs, the designer can easily improve the gain. 50 Ωs is desirable because most RF test equipment is designed for a 50 Ω characteristic impedance, and most image reject filters are specified in a 50 Ω environment.

On the application board however, no output matching was used because the output return loss without matching is about 10dB, so only about 0.5dB of gain is lost due to impedance mismatch. However, a designer could improve the output match, and thus the LNA gain, by 0.4dB by using the low pass circuit below (Figure 13), which also has the advantage of reducing high frequency noise. One is not constrained to use only this circuit, but may choose to use a high pass circuit which uses one less external component for those situations where parts count is more important than noise filtering.

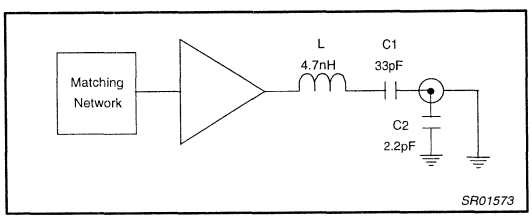


Figure 13 . LNA Output Circuit

The input matching circuit (Figure 14) is basically a simple shunt L match. The network may seem trivial but its realization is not. For example, placement of the 0805 size SMD inductor is critical because the necessary interconnecting transmission lines and the spatial size of the inductor itself will rotate the theoretical point to another position on the Smith chart. Therefore, the actual impedance being matched will vary depending on where the designer places the 6.8nH inductor with respect to the LNA input pin. This is always a consequence of using lumped parameter solutions at microwave frequencies rather than transmission line segments; the advantage is reduced board space at the expense of greater difficulty in getting the match to work properly. These devices should be as small as possible consistent with wanted efficiency or element Q. Inductors are typically size 0805 or larger while capacitors are 0603 or larger.

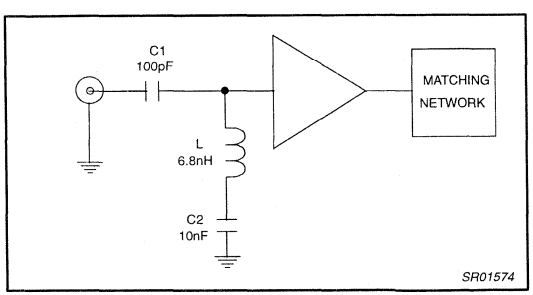


Figure 14 . LNA Input Match

Note that the input matching network also includes a 100pF capacitor for DC blocking as well as a 10nF capacitor. The 10nF capacitor plays two roles in this circuit. First, DC-wise, the capacitor prevents shorting the DC bias potential present on the input pin through the 6.8nH inductor to GND. Second, the 10nF capacitor introduces destructive phase cancellation of the third order intermodulation products present at the input and output thus improving the overall LNA IP3 performance. As this capacitor is increased, IP3 performance improves at the expense of LNA power-up turn-on time (turning "on" the LNA after powering it down). Table 3 shows the compromise between turn-on time and input IP3.

Table 3. LNA Input IP3 vs Switching Time

RF Input Level = –30dBm		Gain	Switching Time
Capacitance	IP3in		
10nF	–7.5	15	84uS
22nF	–6.3	14.8	220uS
47nF	–5	15	490uS
100nF	–5	15	720uS

With any UHF RF application, layout is critically important to circuit performance. For matching and RF signal routing, board traces must be viewed and treated as transmission lines or antenna segments. As transmission lines, they affect nodal impedances (impedance at any point on the segment or at its ends) and cause rotations on the Smith Chart. The most common model treats them using classic microstrip theory where they are implemented as traces over a single ground plane. Without a ground plane, a microstrip becomes a trace or wire behaving as an antenna segment susceptible to unwanted coupling and radiation. Thus, designer's must account for length and width of traces as well as their proximity and relation to associated ground planes. Generally, narrow traces should be avoided because of their high characteristic impedance, greater phase delay and radiation losses. The demo board has microstrip lines connected to both ports of the LNA with associated ground planes on opposite sides of the board. Their lengths were kept as short and as wide as practical. Since truly 50 Ω lines are impractical, being over 100 mils wide on 62 mil thick FR4/5 PCB, the demo board uses traces having characteristic impedances between approximately 75 and 90 Ωs. This makes introducing lumped matching elements simple, because they have predictable electrical length (phase delay) and low radiation thereby improving isolation and minimizing unwanted coupling. Discrete capacitors or inductors should generally be mounted over a ground plane for best isolation. Radiation, especially from inductors, may also need to be taken into account. A FET probe on a spectrum analyzer can be useful in determining whether such elements need shielding or re-location. Elements carrying comparatively high RF currents, in oscillator tank circuits for example, will nearly always require shielding for good isolation and spurious radiation attenuation.

Good port-to-port isolation is necessary to minimize unwanted output-to-input feedback that might result in parasitic oscillations or poor stability. Poor isolation also increases the affect of output termination on the actual input impedance of the device and vice-versa, modifying the actual $S_{11}$and S_{22} seen at input and outputs respectively with particular port terminations. Essentially, this modifies S_{12}. This can make realizing a particular gain and noise figure by design difficult or impossible.

Board layout will always degrade isolation. For example, on the SA621/SA611 demo board, the LNA input is pin 15 and the output pin 13. Since these pins are so close together, special attention must be given to obtaining good isolation between them. This is best accomplished by having the input and output ports on opposite sides of the board to take advantage of ground plane isolation. This layout achieved more than 25dB of isolation.

Another aspect to the layout is providing proper RF ground returns to the LNA pins 14 and 16. Input RF currents should return to pin 14 while output RF currents should return to pin 16. One must keep the ground lengths associated with these port's external components as short as physically possible. Failure to do so can result in poor isolation, instability, and parasitic oscillations.

SA621/611 Mixer

The SA621 mixer utilizes the local oscillator (LO), internal to the IC, as one of the inputs to the mixer. The mixer employs an open-collector output structure which allows the designer to match any high impedance load for maximum power transfer with a minimum number of external components. The SA621/611mixer outputs include internal 10pF capacitors that have an effective value of about 12pF because of parasitic capacitance from the internal bond wires and lead lengths from packaging. The mixer output enables the designer to match for high impedance devices (SAW or Crystal filters) or to 50 Ωs for testing. Reference Application note 1777 to review the details of the mixer output circuit commonly referred to as the current combiner. This portion of the application note gives the designer an intuitive feel of the performance of the mixer and the design trade-offs associated with it.

For the SA611, the mixer circuitry is basically the same except that the LO is driven externally. This allows designers to use a VCO component for the LO.

SA621/611 mixer performance

Table 4 is a comparison of the SA611 and SA621 mixer typical performance parameters.

The SA611 and SA621 has the same performance when comparing gain, 8.7dB of typical. As for input IP3 and noise figure, these parts exhibit some differences. For the SA611 the input IP3 is measured to be about +6dBm, while the SA621 measures typically +4.5dBm. The typical noise figure for the SA611 is 12.5dB while for the SA621 it is 12dB. Not too much difference when looking at noise figure. Lastly, the current consumption of both devices are different because the SA611 does not incorporate the SA621's oscillator section.

Improving SA621/611 mixer Noise Figure

Noise figure can be improved in several ways, however there are some trade-offs. The discussion below will go over these trade-offs.

As always, noise figure can be improved by matching, as seen from the LNA discussion earlier. However, with the mixer, noise circles cannot be easily obtained by the same method used for the LNA because the assumption was made that the LNA output was terminated in 50 Ωs. The mixer, on the other hand, has an open collector output structure where by the output is not 50 Ω terminated. To achieve this the output must be matched to 50 Ω, and because of this match, external component issues become a factor which could yield inaccurate results. All the user can do is match for the best noise figure with the triple stub tuner to achieve minimum noise figure. With the triple stub tuner adjusted for a desired noise figure, the designer can then match from any desired impedance to where the triple stub tuner's impedance lands on the smith chart. In effect the stub tuner is being replaced by a matching network that presents the same load impedance to the mixer as the stub tuner; hence, the same noise figure performance should be obtained.

Table 4. Typical performance comparison of the SA611 and SA621

Part	Gain	Input IP3	Noise Figure	Current
SA611	8.7 dB	+6 dBm	12.5 dB	8mA
SA621	8.7 dB	+4.5 dBm	12 dB	13mA

Method of noise figure improving

As mentioned before, there are trade-offs when improving noise figure. The trade-off here is that component count will increase for improved noise figure, while gain and IP3 remain about the same.

Figure 15 is the schematic of the existing mixer input match on the application demo board. From the S11 data from this application note, the match was determined. This is a low pass matching network to reject high frequencies at the IF output, namely the LO.

An alternative is to use a high pass match (Figure 16), however, experience has shown that the noise figure will increase by 0.5dB to 1dB. The benefit of the high pass match is that the component count is reduced by one because only a shunt inductor and a series cap are needed. Also, because there is one less component, the gain is improved by about 0.25dB while the input IP3 is maintained.

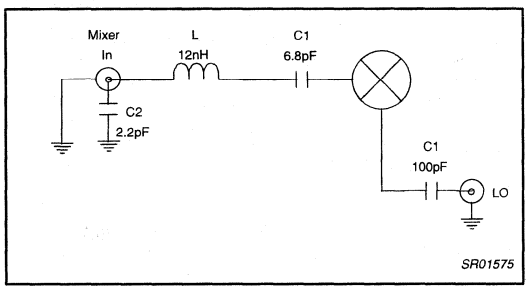


Figure 15 . Existing Mixer Configuration (Low Pass)

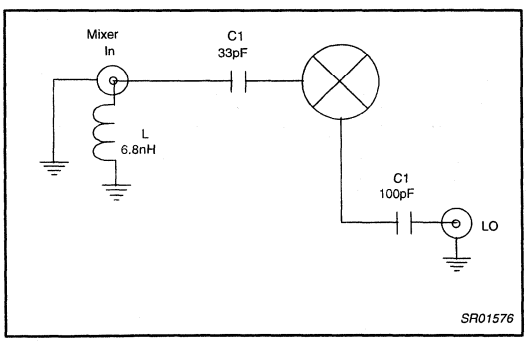


Figure 16 . High Pass Mixer Input Match. (NF Degradation of 0.5db to 1db, Gain Improvement .25db)

If the designer is not pleased with the existing match, he or she could continue to optimize by improving the LO input match. The improvement should be about 0.3dB in noise figure, while gain and input IP3 performance remain the same. Figure 17 shows an additional 3.3nH and 470pF bypass cap. This matching is used to shunt out some of the low frequency noise and improve matching to the LO port.

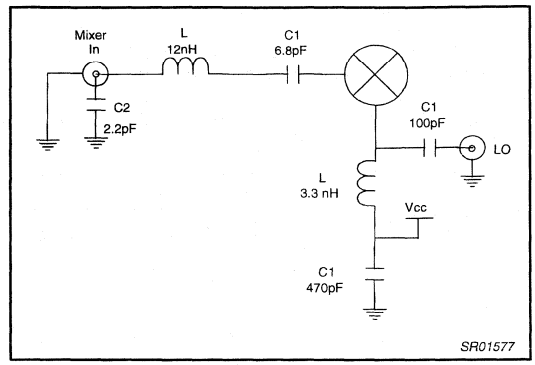


Figure 17 . Mixer with LO matching. (NF Improvement of 0.3dB)

If the designer wishes to improve the mixer noise figure even more at the expense of gain and input IP3, a 6.8KΩ resistor could be used to affect the biasing of the mixer (Figure 18). This improvement does two things, (1) the noise figure is improved nearly 1dB and (2) the mixer current is reduced about 0.5mA. The drawbacks are mixer gain degrades 0.3dB and the input IP3 drops to approximately 1 to 4dBm depending on the current consumption of the part. Further improvements to noise figure can perhaps be achieved by decreasing the resistor even more, however, no attempt was made to do this for this application note.

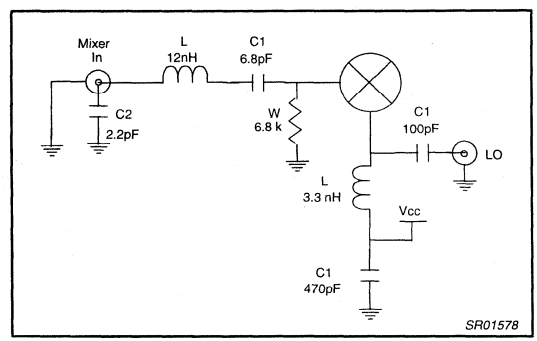


Figure 18 . Mixer Match With Resistor. (Nf Improves 1db, Current Drops 0.5ma, and Gain and IP3in Degrades)

Step by step method to matching the mixer out to 50 Ωs

Many designers have shown interest in using the Philips front-ends but were confused as to how to properly match the mixer output section. The following steps will simplify the task of matching the mixer output at any particular IF frequency or output impedance.

Techniques for optimizing UHF front–end integrated circuits

For a complete analysis of the current combiner theory, please refer to AN1777. The procedure to achieve a match to 50 Ωs will be discussed next.

1. Review of the current combiner circuit.

The current combiner circuit consist of two 10pF internal capacitors plus approximately 2pF parasitic pin capacitance due to internal bond wires, packaging, and the external inductor (Figure 19).

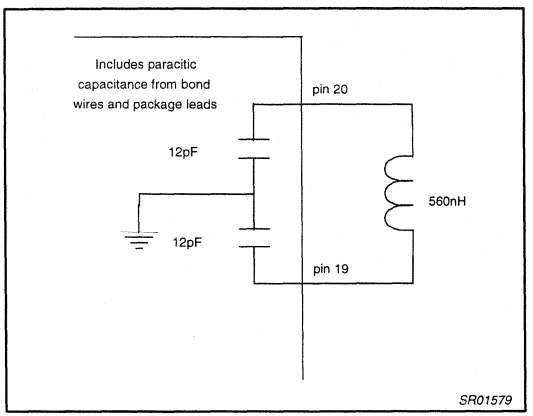


Figure 19 . Current Combiner Circuit

In this case an 83MHz intermediate frequency (IF) was used. The current combiner calculations for 83MHz IF and 12pF internal capacitors dictates that the inductor be 612nH. Since 612nH is not a standard value, 560nH was used instead.

After placing a 560nH inductor into the circuit, the current combiner's output impedance must be determined. Theoretically, the current combiner circuit at resonance will appear to be a pure "real" impedance; however, this is not an ideal case so some reactance will still be present as will be shown later.

First, a determination of a frame of reference for the network analyzer is required in order to begin the match to 50 Ωs. On the demo board, the inductor where Vcc is connected is temporally "shorted" to GND and a 0.1uF capacitor is placed in series before the output connector (Figure 20). This is done to allow the movement of the reference plane from the SMA connector on the network analyzers test cable to a location on the board where a temporary short circuit has been placed. On the network analyzer the port extensions are adjusted until a dot is achieved at the short-circuit point on the smith chart indicating that a new reference plane has been established at the location of the short on the board. This is the same concept that was used for the LNA but this time the dot will be located on the short-circuit side of the smith chart on the left versus the open-circuit side on the right. After achieving this, the temporary short is removed and the output impedance of the current combiner, at the new reference point, is measured.

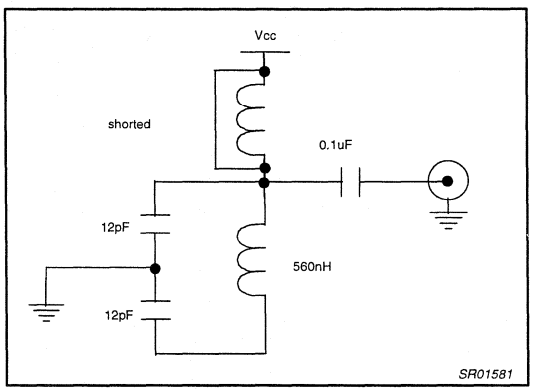


Figure 20 . Board Preparation

The network analyzer should show a reading close to the pure resistance axis of the smith chart at the desired IF frequency, indicating that resonance has been achieved at the proper frequency (Figure 21).

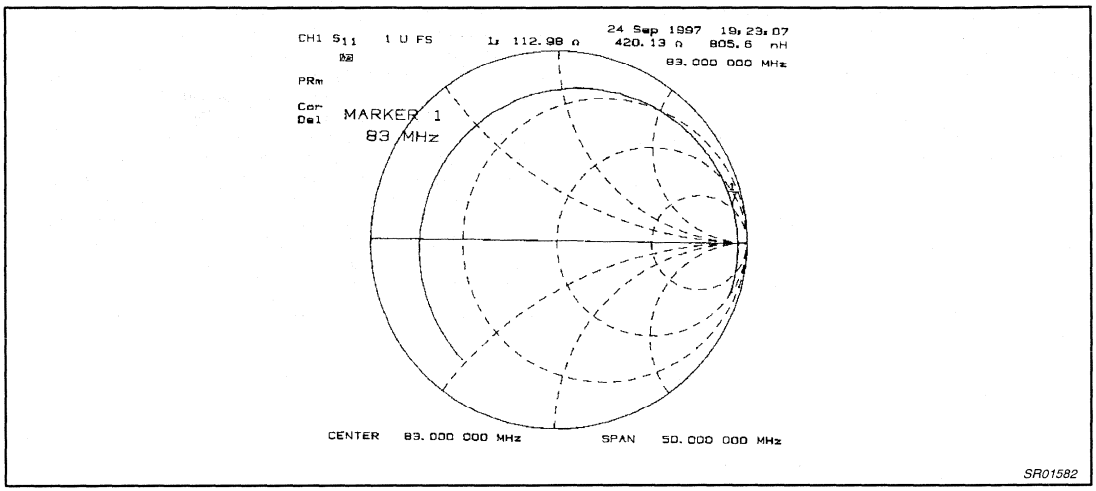


Figure 21 . Measured Output Impedance of the Current Combiner Circuit Shown in Figure 20

Note the residual reactance still present at the desired 83 MHz IF frequency.

To determine the output impedance of the current combiner circuit, the following steps were performed on an HP8753D network analyzer. Press the Marker button, then screen key "marker mode menu" , then screen key "smith marker menu", and finally screen key "R+jX". Once this is done, place the marker at the desired IF frequency, read the real portion of the impedance. In this case the impedance was approximately 420 Ωs in series with 800nH.

2. Match to 50Ωs

Matching to 50 Ωs is a two step process. (1) Add the pull-up inductor to rotate the current combiner impedance to the 50 Ω circle, and (2) add series capacitance to rotate the impedance down to the 50 Ω point located at the center of the smith chart

The same network analyzer calibration that was used for the current combiner output impedance measurement can again be used here. In this case make sure that the port extensions are turned "off" because the interface where the 50 Ω match is desired is now at the end of the network analyzer's test port SMA connector. For the SA621/611 mixer output, a 560nH inductor is used to rotate the current combiner's output impedance up near the 50Ω circle on the smith chart at 83MHz (Figure 22), followed by a series capacitor to rotate the impedance down to around the 50 Ω point on the chart (Figure 23). It was found that a 6.8pF capacitor was required to achieve the desired match.

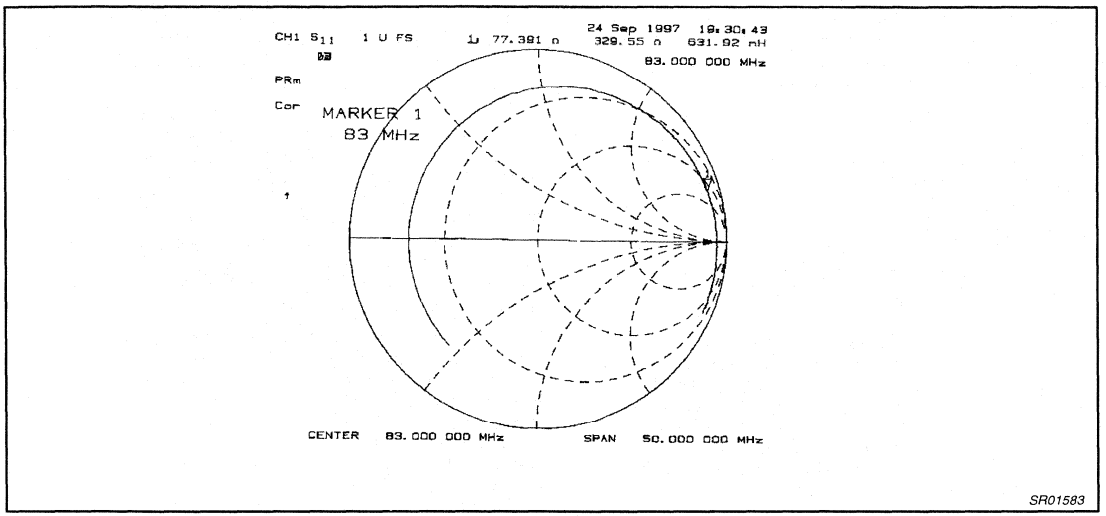


Figure 22 . Measured Output Impedance of the Current Combiner after Rotation on to the 50 Ω Circle at 83 MHz Using a 560nH Inductor to V_{CC}.

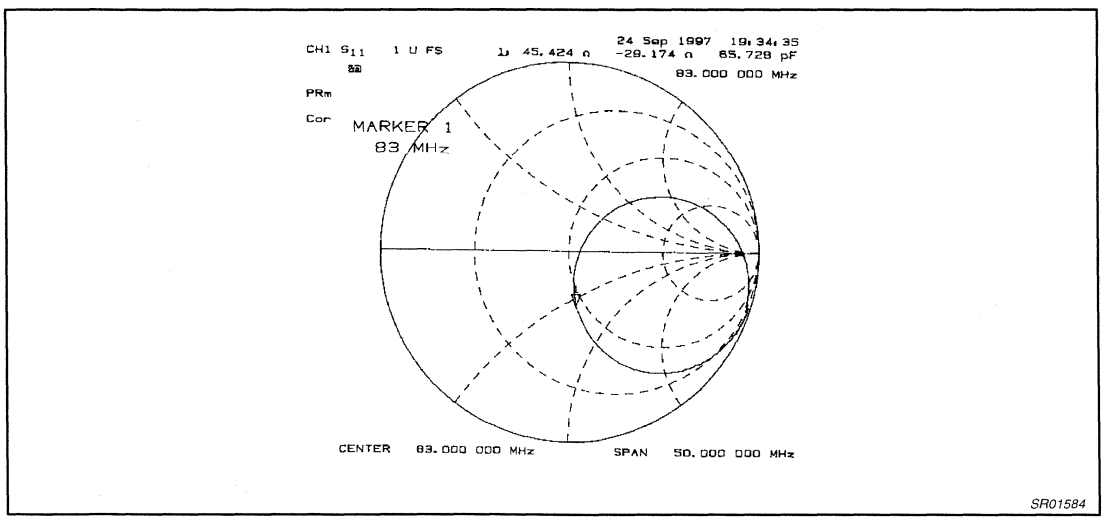


Figure 23 . Measured Output Impedance of the Current Combiner After Rotation To Approximately 50 Ωs at 83 MHz Using a Series 6.8pf Capacitor

When matching to a different frequency the designer should follow the same steps. This method is the quickest way to match to 50 Ωs or to any other impedance for that matter. Note that matching to higher impedances is more difficult but not impossible.

Layout considerations for the mixer

As with the LNA, care must also be taken in the layout of the mixer circuitry. The layout of the mixer input must be done to provide isolation between it and the LNA output in order to prevent signals from bypassing the image reject filter that is usually present between these two pins. If not done properly, degraded sensitivity performance can result from image band interference. For this reason, the LNA output and Mixer input connectors and traces are located on opposite sides of the board to achieve maximum isolation. (Figure 1 in previous LNA section).

In addition to isolation, parasitic capacitance plays a role with the mixer output circuit. A thinner board will have higher parasitic capacitance which will affect the current combiner circuit and impedance matching network. Designers should be careful when using calculated values such as those found in AN1777. These values are approximate and do not take into account parasitic capacitances, so some adjustments will be necessary to obtain the optimal match to a SAW or Crystal IF filter.

SA621 VCO

The SA621 contains a low-noise active circuit meant to be configured with an externally connected passive tank circuit to realize a voltage controlled oscillator (VCO). Feedback is fixed internally and is optimized to operate from approximately 800 to 1000MHz. This stage is capable of very low phase noise performance and is limited only by the external circuitry. A technique using dielectric resonators is presented on the Philips' demonstration (demo) board. Injection amplitude into the mixer LO port depends on oscillator activity, which is principally a function of oscillator circuit Q and impedance loading at pin-4. This pin is also used to sample the LO output for use with an external PLL.

The demonstration board VCO utilizes a physically small, 2mm, λ/4 dielectric resonator (DRO) coupled to pin-7 of the SA621 through a 1.5pF coupling capacitor, C1 (Figure 24). Decreasing this value improves phase noise, however, the trade-off is that the VCO may have start-up problems and/or the VCO may need a higher control voltage before oscillations can begin.

Choosing the dielectric resonator is critical. The designer should keep in mind that the board layout and external components have a significant effect on what frequency of oscillation is achieved. The resonator's center frequency is 1025MHz on the SA621 application board. Phase noise performance is better than –118 dBc/Hz at 60kHz carrier offset and better than –120 dBc/Hz with a 4mm DRO. As mentioned earlier layout adds parasitic capacitance and one method to decrease this capacitance is to minimize the grounding under the DRO. Doing this improved VCO phase noise and increased the oscillation frequency slightly.

Frequency control is normally obtained through use of an appropriately chosen high-Q, low loss, reverse-biased varactor diode lightly coupled through a capacitor in shunt with the DRO. Even with very low capacity varactors, sufficient coupling required to obtain an acceptable tuning range of 26MHz moves resonance to well below 900MHz. Thus, whatever varactor-controlled tuning arrangement is used, it must also introduce a negative susceptance (inductive) to raise the frequency of oscillations back to the target center frequency of 870MHz. This was accomplished on the demo board by coupling a high-Q shunt inductor, L1 and C2 of Figure 24 across the DRO. The varactor, D1, then moves this frequency down by an external DC control voltage, normally the filtered error voltage from an external PLL.

Lastly, pin 10 of the SA621 is used for bypassing. When a 10pF capacitor is used, the phase noise is improved due to internal filtering of unwanted noise; however, this can only be seen when no VCO circuitry is present (only C1 and the DRO). With the rest of the VCO circuit present, the improvement with the 10pF capacitor is not readily apparent because of the higher phase noise due to the presence of the rest of the VCO circuitry.

The Table 5 below summarizes the effects on the VCO of each component in the VCO circuit.

Table 5. VCO summary

PART	FUNCTION
C1	Coupling capacitor to lightly couple pin 7 to the DRO. Increasing its value will lower the VCO frequency and degrade phase noise. Decreasing its value will improve phase noise but oscillator start-up could be a problem.
C2	Coupling capacitor to the varactor diode (D1). This capacitor will affect the tuning range of the VCO. Increasing its value will provide a wider tuning range while sacrificing phase noise. Decreasing its value will have the opposite effect.
C3	Bypass capacitor of VCO. A value of 10pF will improve phase noise with only C1 and the DRO present; however, with more circuitry, the phase noise is degraded to a point where the improvement is insignificant. 220pF was chosen.
D1	Varactor diode used to allow tuning the VCO to different frequencies. As its voltage is increased, the capacitance of the varactor diode decreases, thus phase noise performance is better at higher control voltages than at lower control voltages.
L1	High Q inductor used to raise the frequency of oscillation. The total susceptance of the varactor diode and coupling cap (C2) is reduced thus improving phase noise while trading-off tuning range.
R1	Resistor used to reduce power supply noise from coupling into the VCO circuitry.
Dielectric Resonator (DRO)	The heart of VCO circuit. The higher Q resonators will deliver the best phase noise performance. Resonators come in 2mm, 3mm, 4mm, and 6mm sizes with the larger resonators providing the highest Qs

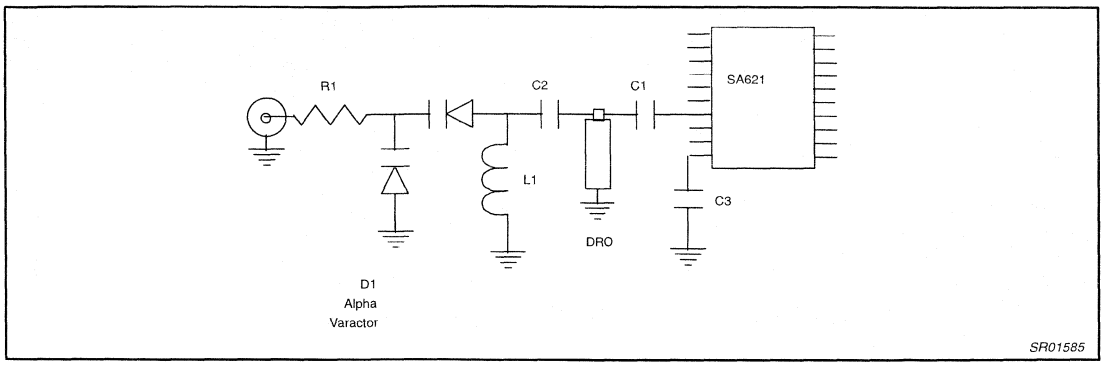


Figure 24 . SA621 VCO

Designers should be aware that this circuit was developed for demonstration purposes only. To limit spurious radiation and influence by stray magnetic fields (typically 50 or 60 Hz), the inductor would certainly require shielding. Shielding will also cause changes in VCO center frequency and tuning range, factors that would have to be accounted for in a real design.

CONCLUSION

This application note has presented a review of RF amplifier matching network design theory from a practical standpoint using S-parameters. For simplicity, unconditionally stable devices were considered, although the methods could easily be extended to conditionally stable devices as well. The Philips SA621/SA611 integrated UHF front-end chips were presented as typical devices. Stability and input gain and noise circles were defined with examples given for each. Note that output gain circles are also obtainable using techniques similar to those employed in finding the input gain circles, but this topic was not treated, since they are usually not required. The utility of input gain circles is obvious owing to their immediate value in graphical comparison to noise circles, as both types vary with changes in the input reflection coefficient Γ_S. Also, since useful noise performance data is often lacking in published device data sheets, an experimental method was presented that makes obtaining them for design purposes reasonably quick and accurate. Interested designers can easily construct calibration boards for rapid in-house evaluation of candidate devices when data sheet S-parameters or noise data are deemed insufficient for a particular application.

Layout and construction issues were also discussed from the standpoint of exploiting hybrid designs using a mix of transmission line segments and classic low-frequency lumped parameter elements in the form of surface mount inductors, resistors and capacitors. This technique can save considerable board real-estate but suffers from requiring much time to realize a suitable design. Understanding S-parameters, the Smith Chart, and layout issues can greatly decrease development and/or evaluation time without expensive simulation packages.

Also presented in this application note were trade-offs of the mixer and VCO circuits. This portion of the application note was intended to give the designer an intuitive feel of how to best implement the SA621 VCO. In summary, the SA611 and SA621 provide low-cost, high performance Front-End solutions for the growing wireless communications industry.

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UMA1015M low power dual 1GHz frequency synthesizer

AN93016

Author: Ir. J. J. Jacobs

SUMMARY

This application note is a guide for designing a phase locked loop based on the Philips UMA1015M dual frequency synthesizer. The UMA1015M is a low power single chip solution to dual frequency synthesis in the range 50 MHz to 1100 MHz and is primarily intended for use in analog wireless communications equipment, such as 900 MHz cordless telephone, CT1, CT1+ and cellular radio telephone AMPS, TACS and NMT.

A basic loop filter design method is discussed. Following this procedure a dual synthesizer at 900 MHz is designed and measurement results are presented.

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1 INTRODUCTION TO UMA1015M DUAL SYNTHESIZER

1.1 General Description

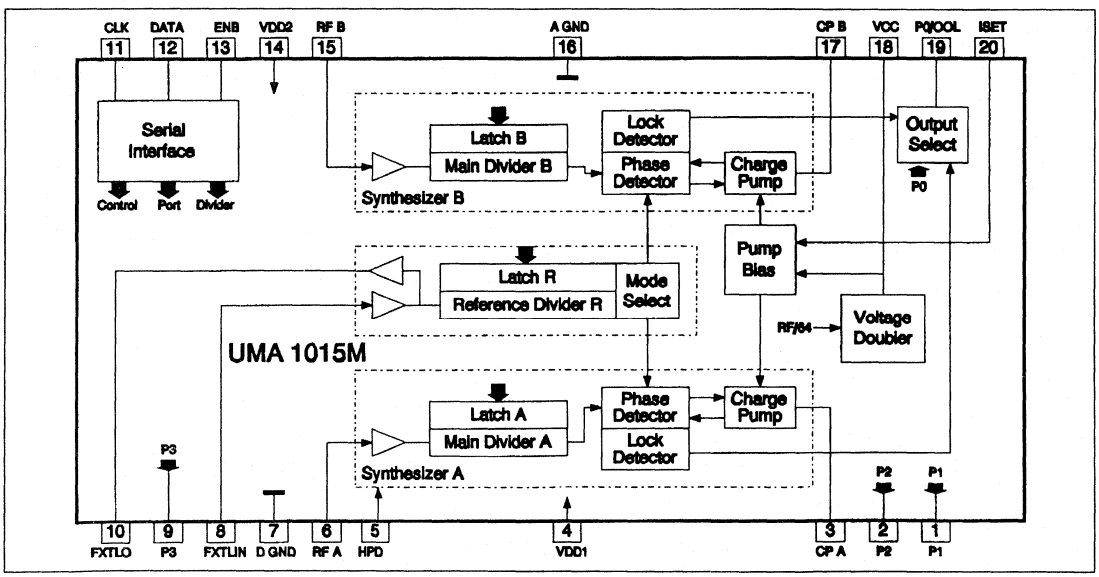


Figure 1. UMA1015M Dual Synthesizer for Mobile Radio Communications

The UMA1015M [1] is a low power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz. The IC is programmed via a 3-wire serial bus which works up to 10 MHz. The programmable charge pump currents are fixed by an external resistance at pin I_{SET}. The BiCMOS device is designed to operate from 2.6 (3 Ni-Cd cells) to 5.5V. Each synthesizer can be powered down independently via the bus to save current. It is also possible to power down the chip via the pin HPD.

1.2 FEATURES

- Two synthesizers in one package
- Integrated prescalers for each synthesizer, 50 MHz to 1.1 GHz
- Reference divider common for both synthesizers, 3 MHz to 35 MHz
- Serial bus (3-line bus: data, clock, enable) for fast programming (f_{max} = 10 MHz)
- Wide, continuous and independent ranges of division ratios:

- 17 bits for each main divider (integer ratios between 512 and 131071)
- 12 bits common reference divider (integer ratios between 8 and 4095)
- In addition to the reference divider an extra divide by 2 block is selectable to set the reference frequency ratio between both synthesizers (1:1 or 1:2).

- Simple passive loop filter for typical applications
- Charge pump output current under bus control, set by external resistor, 0.1 .. 2.4 mA
- Operating voltage range 2.6 to 5.5 V for battery powered operation
- Low current consumption, 8.5 mA typically at 3 V.
- Independent power down modes for both synthesizers
- 4 multifunction output ports
  - (bus controlled, open drain, also active in power down mode)
- Programmable Out Of Lock detector/Output port (open drain)
  - (OOL synth. A, OOL synth. B, OOL synth. A or B, logic '1', logic '0')
- SSOP20 Package
- Buffered output of reference signal (open drain)
- Integrated voltage doubler for high phase detector output voltage

1.3 Typical Application Architecture

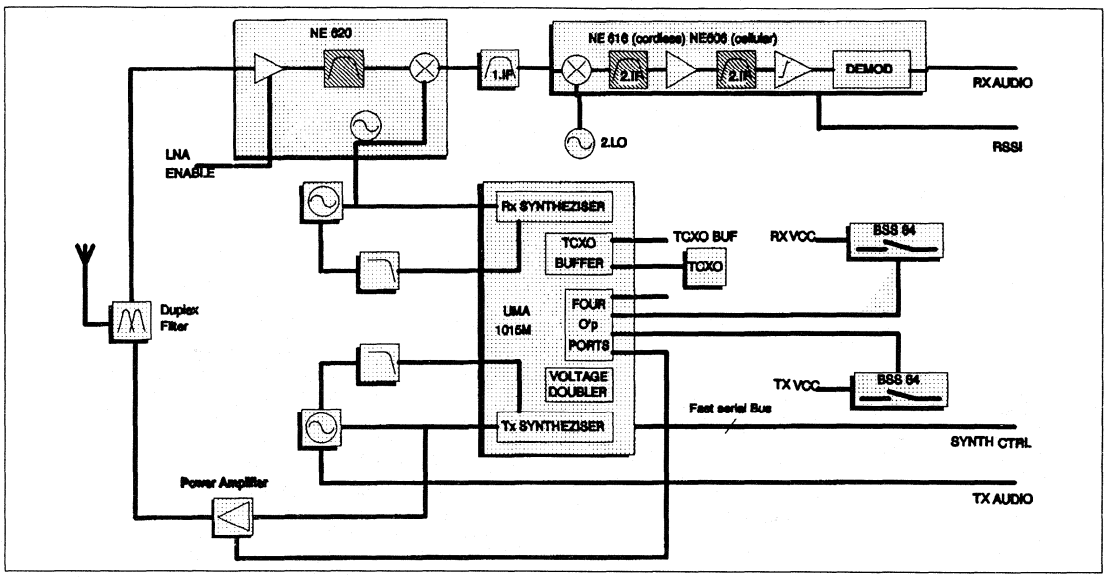


Figure 2. UMA1015M Dual Synthesizer in Typical Analog Transceiver Architecture

The UMA1015M dual synthesizer is processor controlled and notable for its flexibility in many different applications, e.g., CT1, CT1+, AMPS, TACS, NMT.

Figure 2 demonstrates the UMA1015M in an architecture commonly used in analog battery powered telecommunication equipment. The first local oscillator (LO) in the receive path and the carrier oscillator in the transmitter use PLL frequency synthesizers.

Four output ports allow processor control on miscellaneous functions in the transceiver, e.g. disable the transmit VCO or power amplifier.

The independent power down modes allow the transmit synthesizer to stand by while only the receiver periodically 'wakes up' to scan for incoming calls. When both synthesizers are in power down mode, the programmed data is retained in the synthesizer and current consumption is reduced to only 60 µA (maximum value).

For typical applications (900 MHz radio communications) a passive loop filter is sufficient, thus removing the need for operational amplifiers in the loop filter. The gain inside the loop is under bus control by switch-selecting the charge pump output current to either 12 or 24 times a value set by an external resistor at pin I_{SET}.

Programming the comparison frequency ratio select to 2:1 (as opposed to 1:1) allows optimized designs even for applications with half channel offset, such as CT1 and TACS. The comparison frequency may equal channel spacing in the receive synthesizer and half channel spacing in the transmit synthesizer.

In typical applications a temperature compensated reference oscillator will be used to provide the specified frequency stability. The reference input signal (pin 8, FXTLIN) is internally buffered and output to pin 10 (FXTLO). The buffered signal may be used as a

stable system clock or (after conversion) as the second local oscillator.

If a 9.6 MHz TCXO is used as a reference, a 1/8 divider is enough to generate a 1.2 MHz stable system clock for use in the Philips Cellular Chip Set [2].

The UMA1015M synthesizer features an on board voltage doubler. The primary use of the voltage doubler is in low voltage applications to generate VCO control voltages above the synthesizer supply voltage. The voltage doubler is enabled and disabled by programming the VDON bit via the bus. Programming the synthesizer into power down mode does not disable the voltage doubler. An external capacitor is required on pin VCC (pin 18) for smoothing. When the voltage doubler is enabled, thorough decoupling between synthesizer and VCO supply lines is necessary.

The P0/OOL signal can be used to switch the power amplifier enable line under control of the lock detect circuitry during normal 'conversation' mode to avoid false transmission if lock is unexpectedly lost. In other situations (for example when terminating a call) the processor can directly control the output of this pin by programming it to logic '1' or '0'.

Since the P0/OOL port is of open drain type, a wired-or configuration can be implemented to allow control of the transmitter to different devices, such as a micro controller. In a wired-or configuration, control of the transmitter is provided by a single line with controlling devices 'pulling low' to disable.

2 FUNDAMENTALS

2.1 Phase Lock Loop

Figure 3 depicts a generalized PLL block diagram.

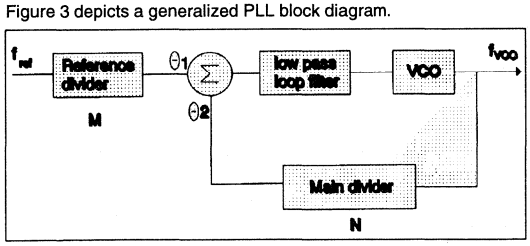


Figure 3. Main Components in Common PLL

The main parts in a common PLL are a phase detector, loop filter, voltage controlled oscillator, main divider and reference divider. In an in-lock situation the output frequency of the system is:

$$f_{VCO} = \frac{N}{M} \cdot f_{REF} \qquad (1.)$$

where f_{ref} = reference input frequency
f_{VCO} = VCO output frequency
M = reference divider division ratio
N = main divider division ratio

The inputs θ_2 and θ_1 to the phase detector are the comparison frequencies. The output of the phase detector is an error signal proportional to the difference in phase between the two input signals.

The keys for controlling the phase lock loop response are the time constants in the loop filter [3][4][5]. Frequency synthesis always involves PLL performance compromise: keeping loop bandwidth as wide as possible to reduce acquisition time and VCO noise, and at the same time suppressing reference frequency sidebands that can pass through wide bandwidths. But stability, being an absolute necessity, gets priority. The other two requirements, unfortunately, are inversely dependent and must be traded off against each other.

2.2 Phase comparator & charge pump

The two phase comparators in the UMA1015M dual synthesizer are sensitive to both phase and frequency. They react to small frequency differences between the inputs and have a highly linear response characteristic. The design responds to the full 360° range of phase inputs and control the charge pumps.

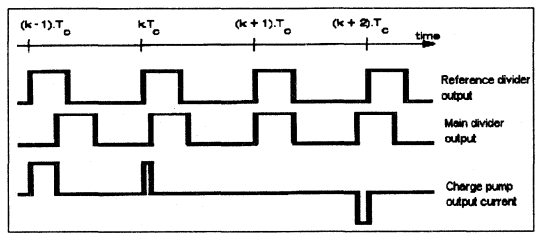


Figure 4. Timing Diagram

The phase comparator outputs are configured as charge pumps (current sources) so that the loop filters (integrators) can be designed with simple, passive components. The charge pumps drive the synthesizer loop filter to generate the VCO control voltages.

The operation principle of the phase detectors is depicted in figure 4. The comparison frequency f_c at the inputs of the phase comparator is typically the same as the system channel spacing. The phase comparison is performed once in each period of the reference signal. The duration between the comparisons is T_c, which is the reciprocal of f_c. Lower case letter k is an arbitrary index.

The charge pump outputs of the synthesizers are tri-state outputs. When in lock, i.e. when the phase error at the inputs of the phase comparator is zero, the charge pump output is in high impedance state. When the loop is unlocked the charge pump sources current pulses when the output of the reference divider is leading and sinks current pulses when lagging the main divider output. The duration of the pulses is proportional to the phase error. The sinking and sourcing pulses charge or discharge the capacitors in the loop filter.

To prevent cross talk between both synthesizers, the design of the chip assures that both charge pumps are never active simultaneously during normal operation.

The charge pump current (the 'height' of the positive or negative pulses in figure 4) is switch-selectable by software (bits CRA and CRB) and continuously adjustable via an external resistor.

The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature independent voltage of 1.2 volt is generated. R_{SET} should be between 12 kΩ and 60 kΩ to give an I_{SET} of 100 µA and 20 µA respectively. The charge pump current, I_{CP}, can be programmed for each synthesizer to be either (12 x I_{SET}) or (24 x I_{SET}) with the maximum being 2.4 mA.

Larger currents are used for fast switching. Smaller currents allow use of smaller capacitors but may make the system more susceptible to interferences and noise.

3 LOOP FILTER DESIGN

This chapter presents a loop filter design procedure in two parts:

- A basic design procedure yields approximate values for the main components.
- A PC based simulation program is used for analysis and optimization.

3.1 Basic Design Procedure

The basic design procedure yield approximate values for the components in the loop filter depicted in figure 5.

The procedure resorts to second-order loop approximations and describes the loop behavior in terms of its natural frequency f_n and damping ratio ζ. The natural frequency of the loop refers to the resonant frequency of the loop. The damping refers to the damping of this resonant frequency [3][4][5].

a: select basic loop and synthesizer parameters:

- output signal frequency, f_{VCO}, [Hz]
- VCO gain, K_{VCO}, [Hz/V]
- switching time, t_{sw}, [s]
- comparison frequency, f_{comp}, [Hz] (equals channel spacing or half channel spacing)
- loop damping factor, ζ , unitless (select ζ =0.707 for fastest switching, ζ =1 for low overshoot)
- charge pump output current, I_{CP}, [A]

b: calculate main division ratio and approximate natural frequency of loop from switching time requirement:

- main division ratio, $N = \frac{f_{VCO}}{f_{comp}}$ (2.)
- natural frequency, $f_n = \frac{2}{t_{SW}}$ (3.)

c: calculate resistor R_{SET} for setting charge pump output current

- resistor at I_{SET} pin, $R_{SET} = \frac{1.2 \cdot CRx}{I_{CP}}\ \Omega$ (4.)

where CRx = 24 if CRA/CRB bit is programmed to 1
CRx = 12 if CRA/CRB bit is programmed to 0

d: calculate approximate loop component values:

- main capacitor, $C_1 \approx K_{VCO} \cdot \frac{I_{CP}}{N \cdot (2\pi f_n)^2}$ (5.)
- damping resistor, $R_1 \approx 2 \cdot \zeta \sqrt{\frac{N}{K_{VCO} \cdot I_{CP} \cdot C1}}$ (6.)
- filter capacitor, $C_2 \approx \frac{C_1}{10}$ (7.)

The loop filter components calculated above are approximations and can be used as starting values for further analysis and optimization.

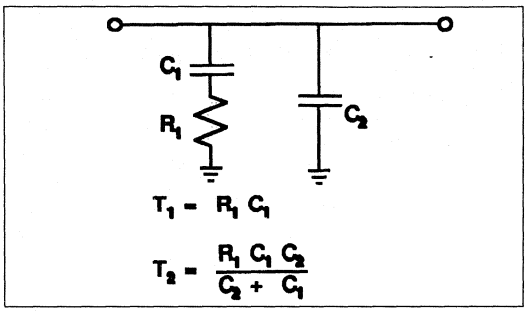


Figure 5. Second-Order Loop Filter

3.2 Analysis and Optimization

For analysis, optimization and worst case design of more complex filters, key loop parameters can be entered into a software analysis program to verify loop stability and switching time, for example SIMPATA [6]. Simpata is an interactive menu driven Phase Lock Loop design tool that runs on a personal computer and comes with a user manual. Among others the program can generate Bode Plots.

Figure 6 depicts a third order filter. The filter results from adding a low pass RC filter stage to the second order filter from the previous paragraph. The extra filter stage can reduce comparison frequency breakthrough spurs without slowing down the response of the loop.

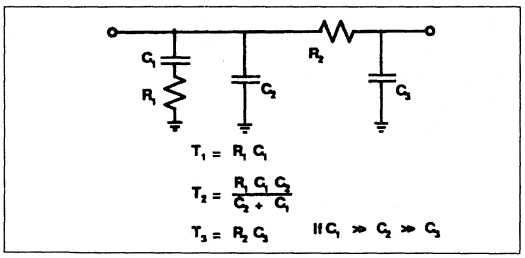


Figure 6. Third-Order Loop Filter

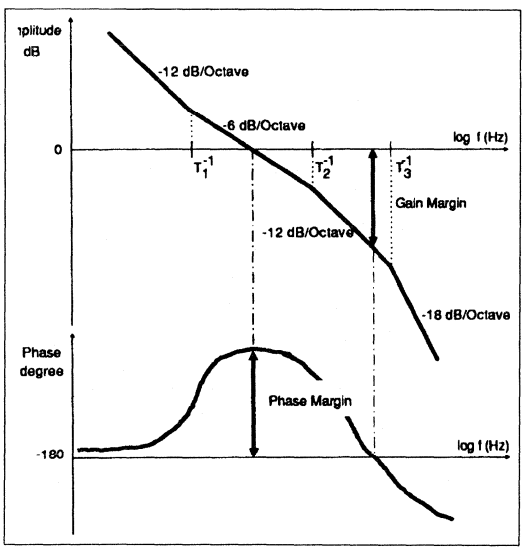


Figure 7. Bode Plot 4th-Order Open Loop Transfer Function Magnitude and Phase

A damping factor to control stability as in simpler second-order loops can not be readily defined in a higher-order loop. Instead, the phase margin becomes important.

The phase margin is easily evaluated and determined from the Bode plot. A Bode plot is a pair of graphs which displays the open loop transfer function magnitude and phase. In figure 7 shows Bode plot of a fourth order loop with third order filter and a pole in the origin due to the VCO.

The phase margin is defined as the difference between 180 and the phase of the open loop transfer function at the frequency where the logarithmic gain is 0 dB (gain cross over). The critical point for stability is a phase margin of 0 . The factor by which the system gain would have to be increased for the phase margin to reach the critical value of 0 is called the gain margin.

The time constants in the loop filter are the keys for controlling the loop performance and phase margin. The effects of different time constants can be evaluated from a Bode diagram. The reciprocal of the time constants of the loop filter in figure 6 are the breakpoints of the magnitude function in figure 7.

When increasing the time constant $T_3 = C_3.R_2$, the breakpoint T_3^{-1} will move left and the magnitude curve will start to roll off at a lower frequency. Therefore, the greater the time constant T_3, the better the comparison frequency breakthrough is suppressed. But increasing T_3 will force the point of inflection of the phase margin curve to move to the left as well, thus decreasing the phase margin and eventually making the system unstable.

Iteratively inspecting the Bode plot, adjusting the loop components and measuring performance, will yield a compromise between switching time and stability. Simulation programs may give reasonable approximations of PLL behavior, but their accuracy is always limited due to the fact that many practical imperfections and non linearities are not taken into account.

The phase margin should be between 30 and 70 for most applications. The larger the phase margin, the more stable the loop, and the slower the response.

A loop with a low phase margin is still stable but may exhibit other problems aside from outright oscillation. A low phase margin makes the transient response more oscillatory and requires very tight tolerances on all loop components, i.e. the phase margin must be positive over all variations in loop components.

A phase margin of 45° is often a good compromise between desired stability and the other generally undesired effects.

4 APPLICATION EXAMPLE

This chapter discusses the design and performance of the UMA1015M demo board.

The UMA1015M demo board demonstrates the UMA1015M dual synthesizer at frequencies in the AMPS (Advanced Mobile Phone System) cellular radio band. The circuit consists of two PLLs with 6 main parts: one temperature compensated crystal oscillator, one UMA1015M comprising two synthesizers, two loop filters and two VCOs.

Auxiliary functions are also demonstrated such as the output ports which can be programmed to power up/down the oscillators.

Circuit diagram and PCB layout are included in the appendix.

4.1 Loop filter design example

To accommodate for a fast receive synthesizer and a slower transmit synthesizer, the charge pump current I_{CP} to I_{SET} ratio is programmed to 12 for the transmitter and 24 for the receiver. On the demoboard the charge pumps currents are I_{CP} = 0.9 mA for the receiver (synthesizer A) and I_{CP} = 0.45 mA for the transmitter (synthesizer B).

Basic design procedure for AMPS receive synthesizer:

- VCO frequency, F_{VCO} = 920 MHz
- VCO gain, K_{VCO} = 11 MHz/V (from VCO specifications)
- Comparison frequency, F_{comp} = Channel spacing = 30 kHz (AMPS specification)
- Reference frequency, $F_{reference}$ = 9.6 MHz (arbitrarily, can have system advantage)

- switching time, t_s , 9 ms (indicative, for 10 MHz jump to within 1 kHz)
- I_{cp} , 0.9 mA, with CRA bit set to 1

Following the basic design procedure from paragraph 3.1 yields:

- main division ratio, $N = \frac{f_{VCO}}{f_{comp}} = \frac{918MHz}{30kHz} = 30,600$ (8.)
- natural frequency, $f_n = \frac{2}{t_{SW}}$

$$= \frac{2}{9 \cdot 10^{-3}} \approx 220Hz \quad (9.)$$

- resistor at pin I_{SET}: $\frac{1.2 \cdot CRx}{I_{CP}}$

$$= \frac{1.2 \cdot 24}{0.9 \cdot 10^{-3}} \approx 33k\Omega \quad (10.$$

The main components in the loop filter are:

- main capacitor, $C_1 \approx K_{VCO} \cdot \frac{I_{CP}}{N \cdot (2\pi f_n)^2}$

$$= 11 \cdot 10^6 \cdot \frac{0.9 \cdot 10^{-3}}{30,600 \cdot (2\pi \cdot 220)^2} \approx 180nF \quad (11.)$$

- damping resistor, $R_1 \approx 2\,\zeta \sqrt{\frac{N}{K_{VCO} \cdot I_{CP} \cdot C_1}}$

$$= 2 \cdot 0.707 \sqrt{\frac{30,600}{11 \cdot 10^6 \cdot 0.9 \cdot 10^{-3} \cdot 180 \cdot 10^{-9}}}$$

$$= 5.8k\Omega \quad (12.)$$

- filter capacitor, $C_2 \approx \frac{C_1}{10} \approx 18nF$ (13.)

The above values for the main components in the receive synthesizer are only approximations as they are based on second order assumptions. For further optimization both a computer simulation program as well as practical experiments are used.

For trying out different component values in the loop filter, adjustable components can be used. The PLL performance can then be evaluated for various component values in the loop filter to find an optimum compromise of loop filter components with respect to the required performances.

Capacitors with leakage currents, such as electrolytic capacitors and capacitors with piezo or delay effects are not preferred because of higher reference breakthrough spurious responses.

For designing the demo board the main performance criteria for optimization were: fast switching, low residual FM and low comparison frequency breakthrough as measured with respectively a time domain analyzer, a frequency modulation analyzer and a spectrum analyzer.

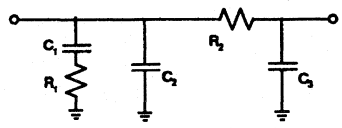
During the optimization process, the software simulation program SIMPATA was used to verify the stability of the design. Figure 9 depicts the Bode plot of synthesizer A on the demo board. The loop gains falls at 6 dB/Octave at the gain cross over point. The requirement for basic loop stability is fulfilled since the phase margin is 52°.

The design procedure of the transmit synthesizer is similar to the above procedure for the receive synthesizer. The main difference is that in typical applications restrictions are imposed on the bandwidth of the loop filter of the transmit synthesizer. To allow audio modulation of the VCO, the loop filter bandwidth must be well below the lowest audio frequency, i.e. well below 300 Hz.

The loop filter components on the UMA1015M demoboard are summarized in Table 1.

Table 1. Design Parameters and Simulation Results UMA1015M Dual Synthesizer Demoboard

Parameter		Slow Transmit Synthesizer B	Fast Receive Synthesizer A
Loop filter components (reference Figure 8 below)		C_1 = 200nF	C_1 = 200nF
		C_2 = 33nF	C_2 = 15nF
		C_3 = 6.8nF	C_3 = 2.2nF
		R_1 = 10kΩ	R_1 = 6.8kΩ
		R_2 = 6.8kΩ	R_2 = 22kΩ
VCO	Gain, K_{VCO}	11MHz/V	11MHz/V
	VCO center frequency, F_{VCO}	836MHz	926MHz
	VCO frequency range	25MHz	25MHz
Comparison frequency ratio synthesizer A : B		ratio 1 : 1	
Comparison frequency, f_{comp}		30kHz	30kHz
Charge pump	Current I_{CP}	0.45mA	0.9mA
	R_{SET}	33kΩ	
	I_{SET} ratio, bits CRA, CRB	12	24
Reference	Frequency (TCXO)	9.6MHz	
	Division ratio	320	
Unity gain phase margin (simulated)		42°	52°
Gain margin at 180° phase margin (simulated)		24dB	23dB
Unity gain phase margin (simulated)		225Hz	330Hz



$T_1 = R_1 C_1$

$T_2 = \frac{R_1 C_1 C_2}{C_2 + C_1}$

$T_3 = R_2 C_3$ If $C_1 \gg C_2 \gg C_3$

Figure 8. Loop Filter Components

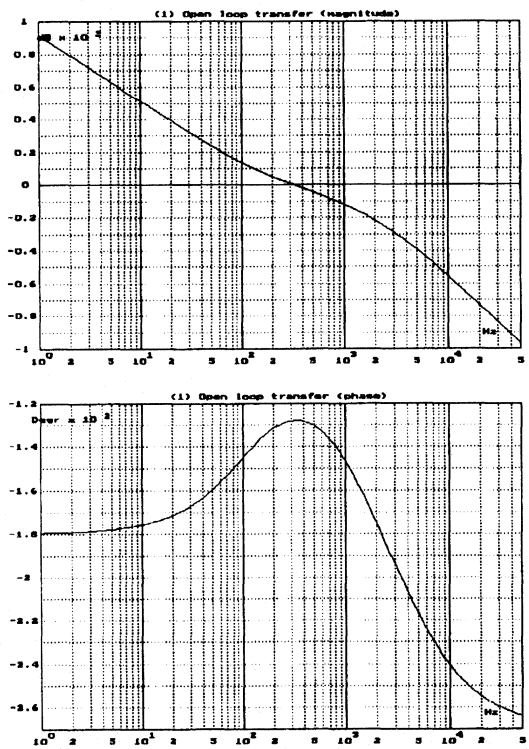


Figure 9. Simulated Bode Plot of 4th-Order Open Loop Transfer Function of Synthesizer A on UMA1015M Demoboard, Magnitude (above) and Phase (below) vs. Frequency

4.2 Performance of Design Example

This section describes the performance measured of the UMA1015M dual synthesizer demo board UMA1015M, designed in the previous paragraphs.

Important performance criteria for a frequency synthesizer are usually:

Close-in phase noise (i.e., noise level within the loop bandwidth relative to carrier)

Noise level at a specified distance from the carrier

Comparison breakthrough components

Switching time for specified frequency jump to within specified distance from target

Residual FM

Power consumption

It should be noted that these criteria can be traded off against each other to some extent to tailor overall performance, and that the performance described here is only one compromise between the various criteria. In general, the choice of a low loop bandwidth will improve the comparison frequency breakthrough and will filter out more of the close-in noise, but will result in a longer switching time. The use of a higher order filter can improve comparison frequency breakthrough with little effect on the noise or switching time. The noise floor at offsets significantly higher than the loop bandwidth is dominated by the VCO characteristics.

Table 2 summarizes the measurement results. Figures 10 to 12 show some measurement graphs from which the numbers in table 2 are read. During the recording of the measurement results, both synthesizers were enabled and locked.

Table 2. Results UMA1015M Dual Synthesizer Demoboard

Measurement results UMA1015M dual synthesizer demo board. Data are extracted from a limited number of engineering samples and do not indicate typical values. VCO supply voltage: 4.2V, both synthesizers enabled; UMA1015M supply voltage: 4.2V, room temperature.

Parameter		Fast Receive Synthesizer A	Slow Transmit Synthesizer B
VCO frequency range		914–939 MHz	824–849 MHz
Residual FM (CCITT weighted, RMS)		13.5 Hz RMS	8.5 Hz RMS
Comparison frequency breakthrough	at 30kHz	71 dBc	90 dBc
Switching time for frequency jump around center frequency to within 2.5kHz off the target frequency	30kHz (single channel)	2.6 ms	2.9 ms
	10MHz	6.2 ms	9.5 ms
	25MHz (maximum jump)	7.5 ms	10 ms
VCO noise level relative to carrier, at specified distance from carrier, normalized	120Hz (close-in)	–57 dBc/Hz	–57 dBc/Hz
	45kHz (adjacent channel)	–116 dBc/Hz	–116 dBc/Hz
Current consumption UMA1015M (Voltage doubler disabled)	Both synthesizers enabled	9.1 mA	
	Transmitter disabled; Receiver enabled	5.2 mA	
	Both synthesizers disabled	approx. 0.007 mA	

Figure 10 shows the transient response of synthesizer A for a 10 MHz frequency jump to within 2,5 kHz of the target to be 6.2 ms.

Figures 11 and 12 demonstrate the noise spectrum of synthesizer B with narrow (2 kHz) and wide (50 kHz) frequency span respectively. The markers in Figure 10 indicate the close-in noise to be 57 dB/Hz below carrier power level. Also from figure 10 the width of the noise plateau indicates that the loop band width is around 230 Hz, which is in accordance with design targets.

Figure 12 reveals an outstanding low comparison frequency (at 30 kHz) breakthrough of more then 90 dB below the carrier power level (below noise level). The low comparison frequency breakthrough allows a trade off of the comparison breakthrough against faster switching.

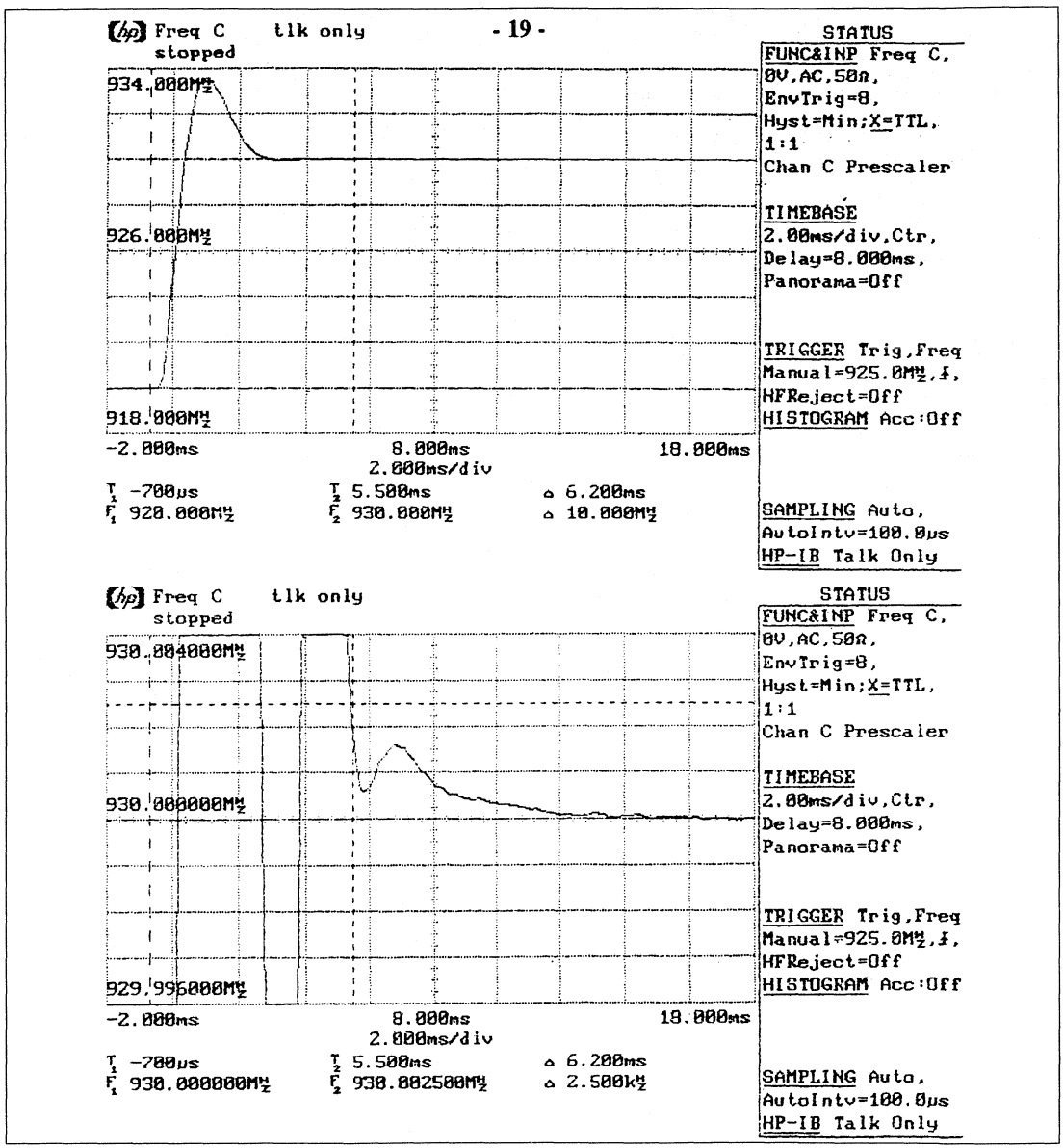


Figure 10. UMA1015M Demoboard, Transient Response Synthesizer A. 6.2ms for 10MHz Jump to Within 2.5kHz Off Target Frequency.

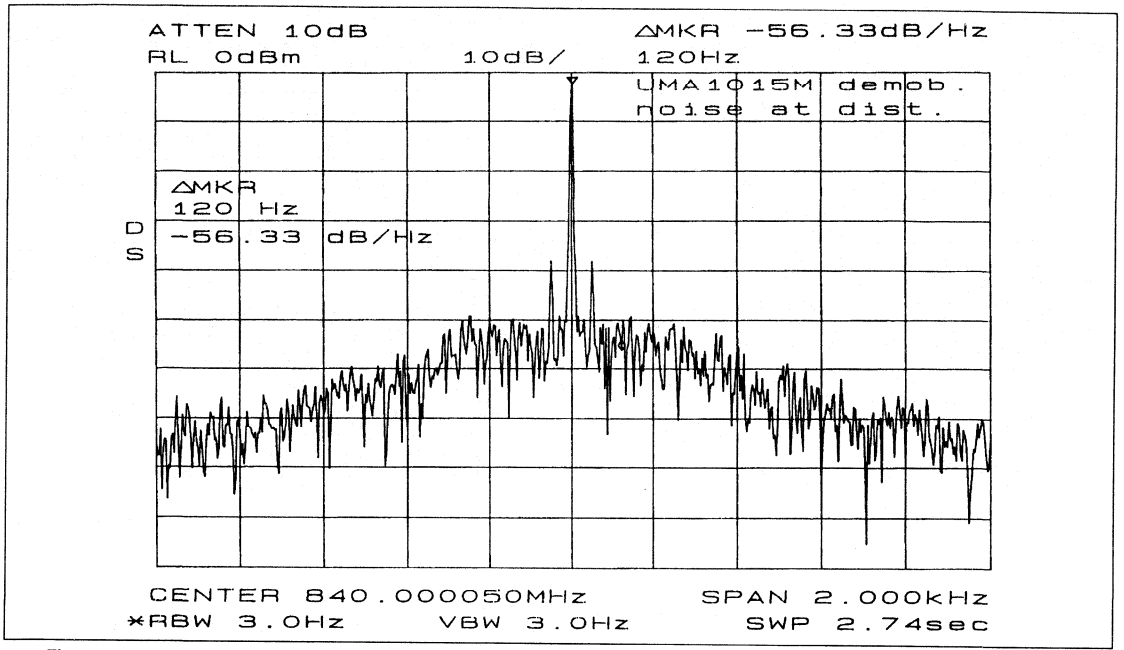


Figure 11. UMA1015M Demoboard, Frequency Spectrum Synthesizer B, 2kHz Span. Close-in Noise: 56dB/Hz Below Carrier.

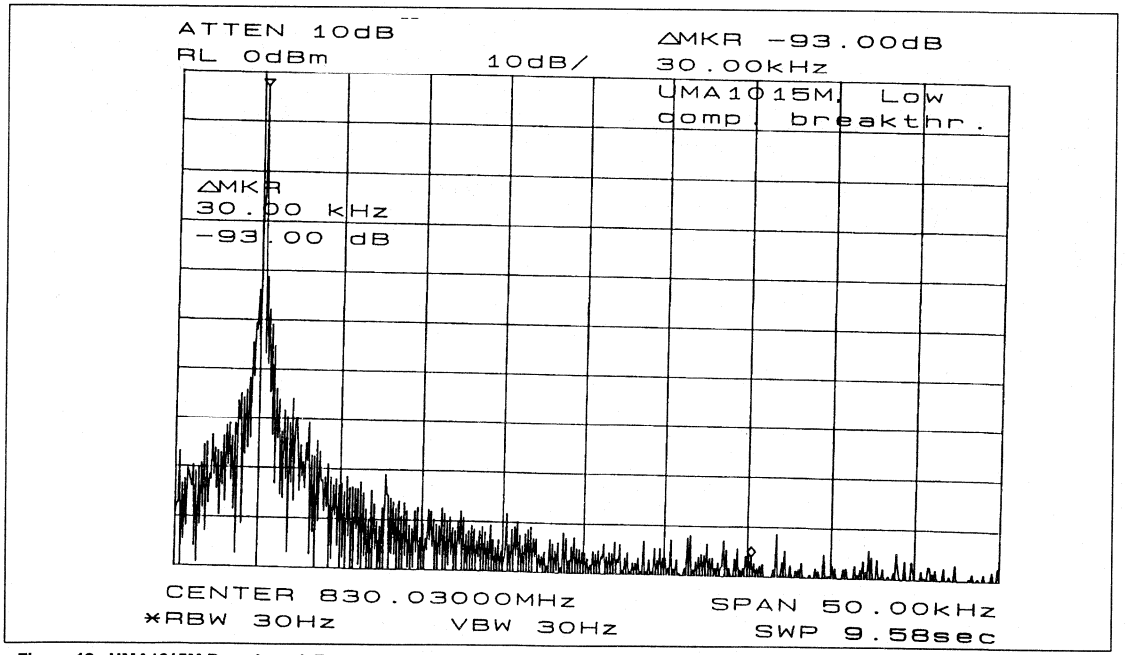


Figure 12. UMA1015M Demoboard, Frequency Spectrum Synth B, 50kHz Span. Low Comparison Breakthrough (below noise level)

5 FREQUENTLY ASKED QUESTIONS

Q. How to use the synthesizer with V_{DD} < 4.5V whereas pins DATA, CLK and ENB are at 5V logic?

A. A. Because of protection against electrostatic discharges, the input voltage for these logic pins can not be greater than V_{DD}+0.3V. An interface between the microcontroller and the synthesizer is then needed to reduce voltage at bus pins. A voltage divider is a simple and cheap solution to implement.

The design of this voltage divider (see below) involves performance compromise between the current consumption and the programming speed, which depend on R1, R2 and Cpar, a parasitic capacitance from the demo board.

A Technical Marketing Report (n° CTT94008) describes some measurements results : for different values of V_{DD} <4.5V, the current consumption and the programming speed are given.

Q. The example below shows a typical programming example of the UMA1015M with the following conditions :

– fxtal input frequency : 9.6 MHz

– Synthesizer A input frequency : 926.01 MHz

– Synthesizer A comparison frequency : 30 kHz

– Synthesizer B input frequency : 836.01 MHz

– Synthesizer B comparison frequency : 30 kHz

– Both synthesizers ON (sPDA = sPDB = 1)

– Out of lock indication from both synthesizer loops (OLA = OLB = 1)

– Charge pumps currents : $I_{CPA} = 24*I_{SET}$ (CRA = 1)

$I_{CPB} = 12*I_{SET}$ (CRB = 0)

– Voltage doubler disabled (VDON = 0)

Table 3. UMA1015M Register Data Allocations Expressed in Decimal and Hexadecimal

First In	Register Bit Allocation		Last In
dtl6	Data Field	dt10	Address
Test register (must be 0 if programmed)			0h
Control register = 0 0001 1100 0110 0000			1h
Synth A main divider coefficient = 30867d = 7893h			4h
Reference divider coefficient = 320 d = 140h			5h
Synth B main divider coefficient = 27867d = 6CDBh			6h

Table 4. UMA1015M Register Data Allocations Expressed in Binary

First In (MSB)							Data Field									Last In (LSB)	Address			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1
0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	1	1	0	1	0	0
0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	1
0	0	1	1	0	1	1	0	0	1	1	0	1	1	0	1	1	0	1	1	0

About Data Format

Special care has to be taken for correct programming when first applying power to the synthesizer.

The ENB signal should be held LOW and only taken HIGH after having programmed an appropriate register on first powering up. If this condition is not achieved, it may result in loading of random data from the serial bus shift register (programming register) into one of the synthesizers data registers/ addressed latches including the test register.

It should be noted that the test register does not normally need to be programmed. However, if it is programmed, all bits in the Data Field should be set to 0.

In case of random data being loaded into the test register, it is recommended to program a frame of zeros, on first powering up.

Q. How to use the TCXO output buffer stage to generate an harmonic of the crystal frequency?

A. The TCXO output is an open drain MOS output. The aim is to generate a signal at a multiple of the crystal input frequency. The most common method is to use a non-linear circuit, for instance a biased amplifier stage and to use a LC output circuit tuned to some multiple of the input frequency.

The following diagram is a proposal to obtain a third harmonic on pin fxtalo.

Q. About PCB layout considerations

Since careful PCB layout has a great impact on performances of RF circuitry, special attention should be paid when designing the frequency synthesizer layout.

To avoid crosstalk between synthesizers (A and B), the printed circuit board should have a solid ground plane on the non surface mount side (apart from isolated pads for non-grounded connections to leaded components). On the surface mount side of the board, the ground plane should be designed round each synthesizer, and underneath the integrated circuit so as to provide maximum isolation between two PLLs. A good number of plated-through holes must connect the two layers of the ground plane.

Power supply bypass capacitors (100 nF) in series with a small value resistor (12 Ω) should be located as close as possible to the device with short leads for pins 4 and 14.

Q. Out-of-lock indication

The Out-of-Lock functions works in such a way that :

– when $_e > T_{OOL}$ with $T_{OOL} = 80/f_{RF}$, the OOL signal goes LOW

– for coming back into lock, $_e$ has to be smaller than T_{OOL} during 8 reference cycles. Then, the OOL signal goes HIGH again. This procedure is described on the following diagram.

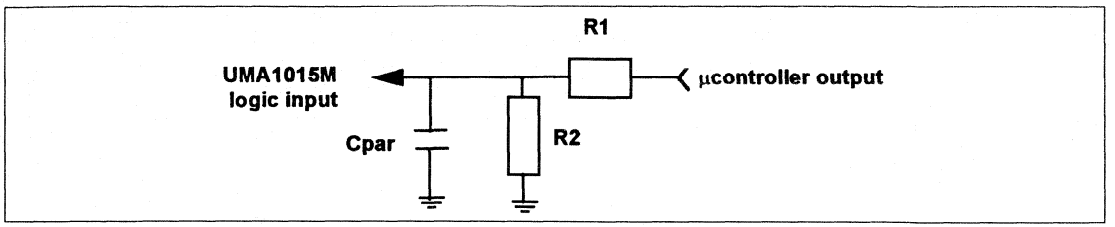


Figure 13. Out-Of-Lock Indication

6 REFERENCES

1. *Product Datasheet UMA1015M*, Philips Semiconductors, 22 June 1995.
2. Data Handbook 1993 *RF/Wireless Communications*, p. 851–895: Cellular Chip Set Design Guide, Philips Semiconductors 1993
3. Gardner, Floyd M., *Phaselock Techniques*, 2d ed., John Wiley & Sons, New York 1979
4. Rohde, Ulrich L., *Digital PLL Frequency synthesizers, Theory and Design*, Prentice–Hall, Englewood Cliffs, New Yersey 1983
5. Best, Roland E., *Phase–Locked Loops, Theory, design, and Applications*, 2d ed., McGraw–Hill, New York 1993, includes disk for PLL simulations
6. *SIMPATA*, PLL simulation program and manual, Philips CTT NatLab, Eindhoven, The Netherlands, 1992. Information or ordering: tel (+31)40–744212, fax (+31)40–744619
7. Technical Marketing Report (CTT94008), *Use the UMA1015M Synthesizer at V_{DD} under 4.5V with serial bus at 5V Logic*, Philips Semiconductors, 1994.

7 APPENDIX UMA1015M DEMOBOARD DATA SHEETS

UMA1015M demo board circuit diagram, PCB layout, component listings.

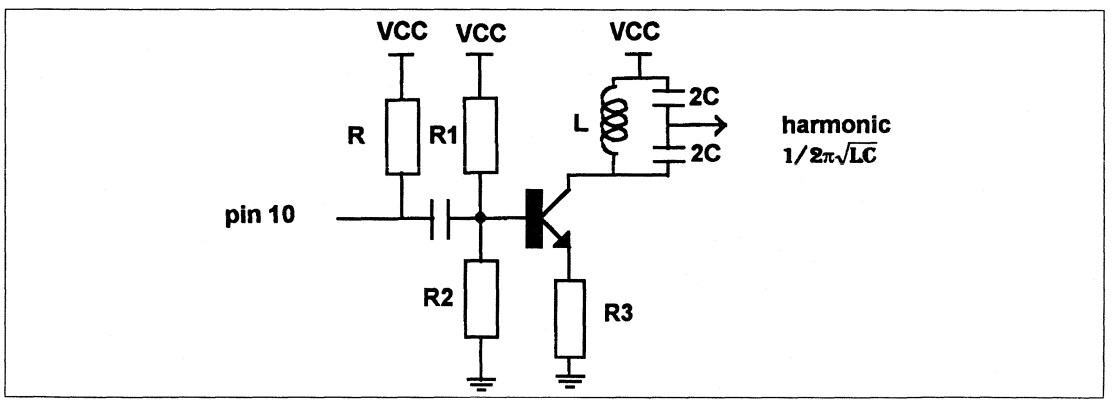


Figure 14.

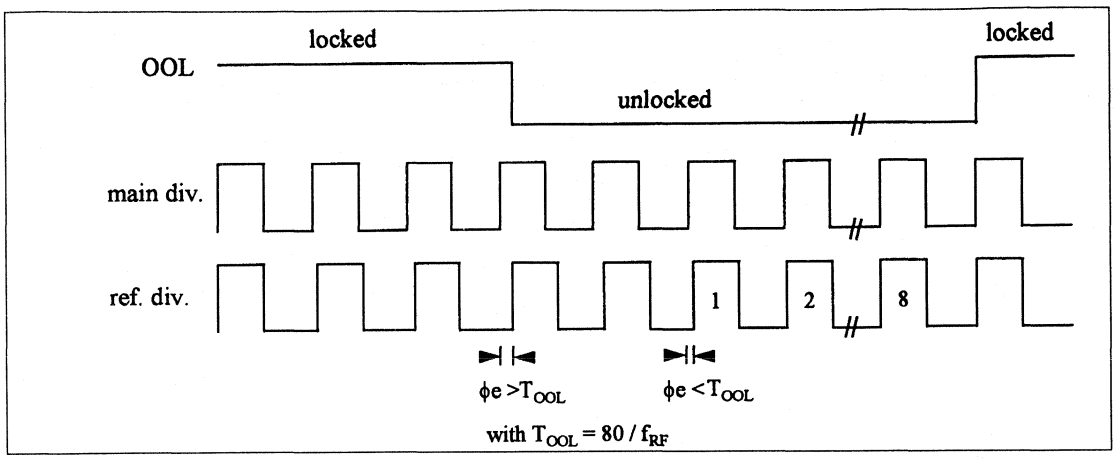

locked
locked
OOL
unlocked
main div.
ref. div.
1
2
8
φe >T_OOL
φe <T_OOL
with T_OOL = 80 / f_RF

Figure 15.

Appendix UMA1015M demo board data sheets

UMA1015M demo board circuit diagram, PCB lay-out, component listings.

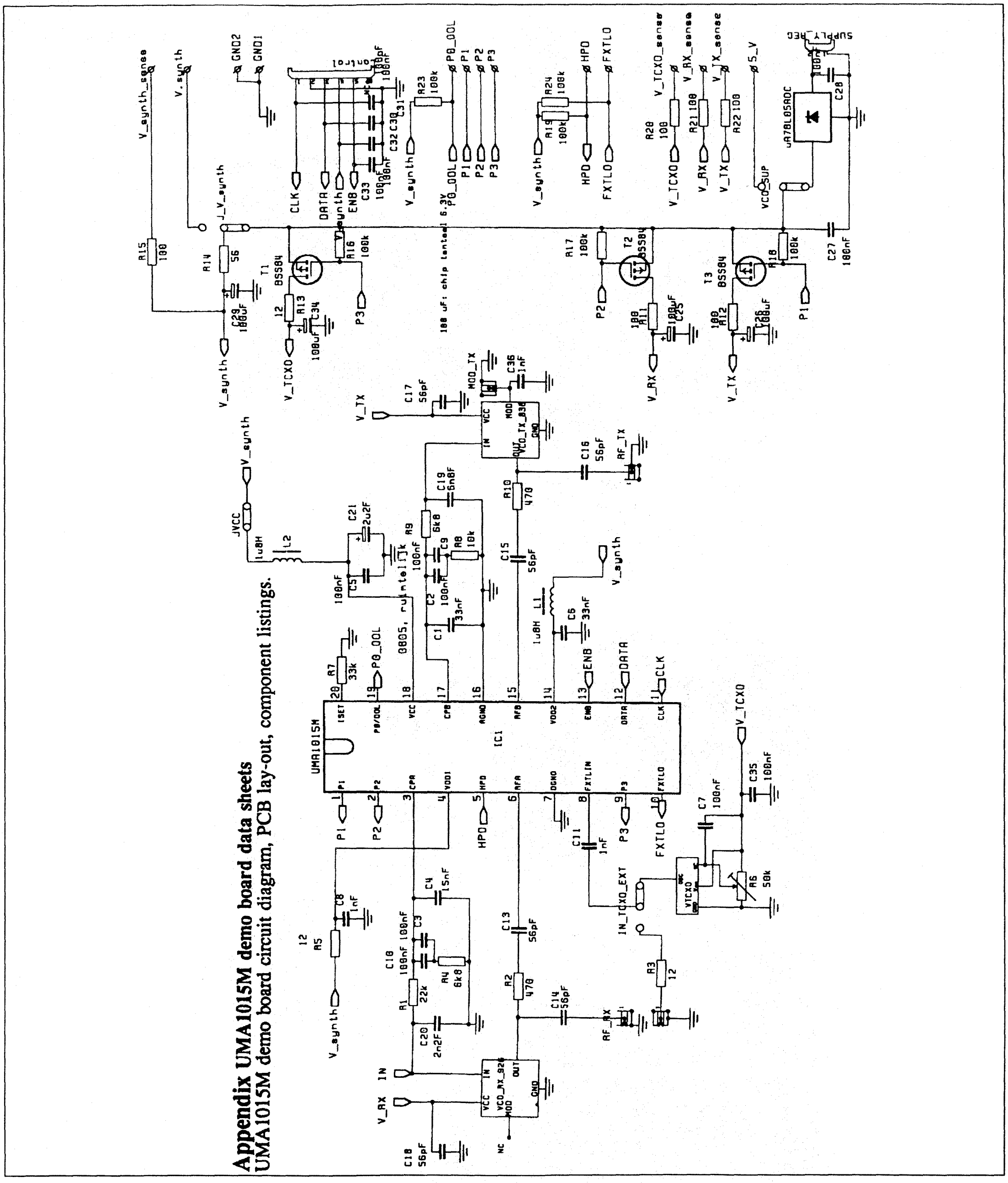


Figure 16.

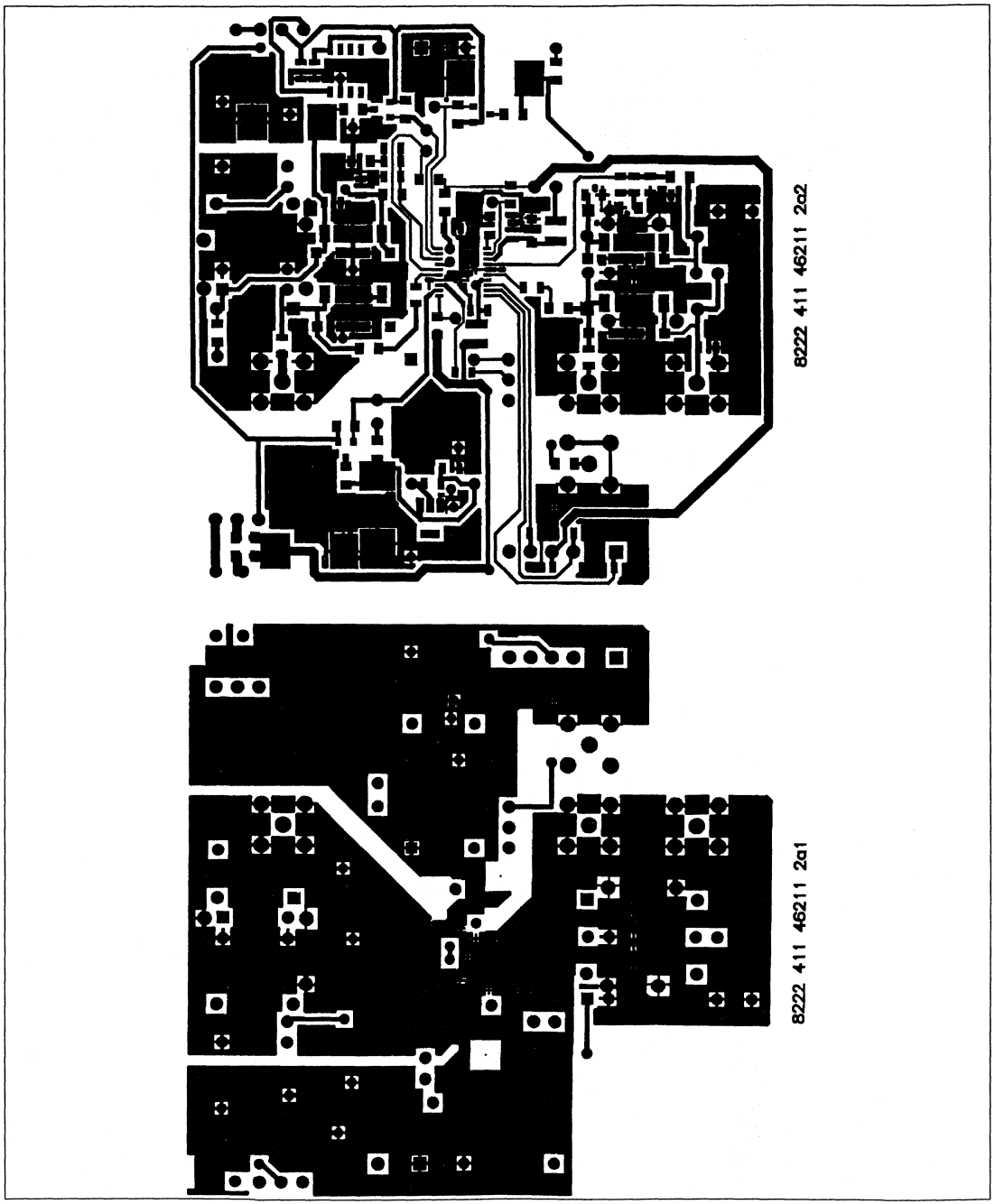
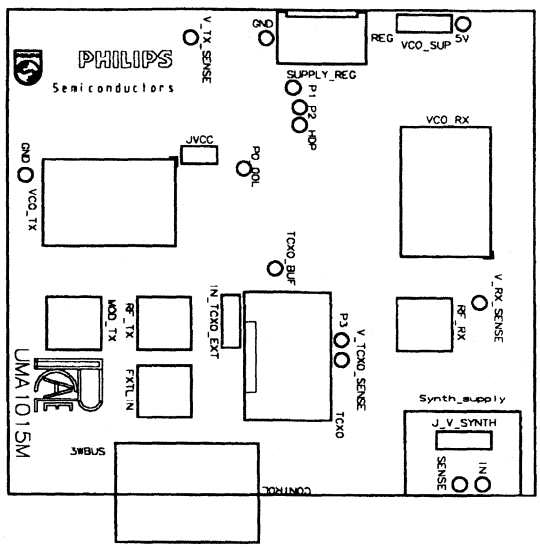


Figure 17.


PHILIPS
Semiconductors
V_TX_SENSE
GND
REG
VCO_SUP
5V
SUPPLY_REG
P1
P2
HOP
VCO_RX
JVCC
PD_PDL
GND
VCO_TX
TCXO_BUF
V_RX_SENSE
MOD_TX
RF_TX
IN_TCXO_EXT
P3
V_TCXO_SENSE
RF_RX
FXTL_IN
TCXO
Synth_supply
J_V_SYNTH
UMA1015M
3WBUS
CONTROL
SENSE
IN

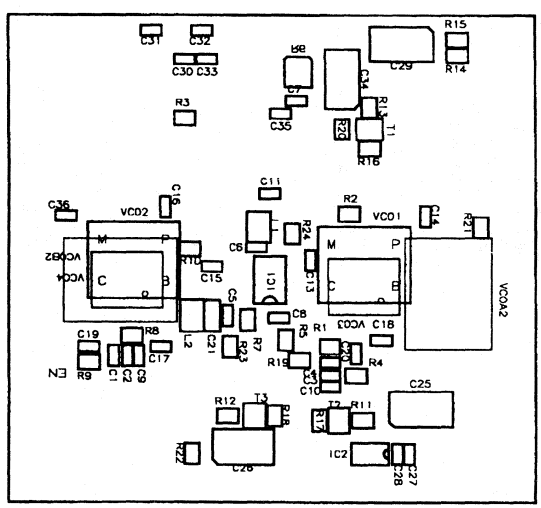
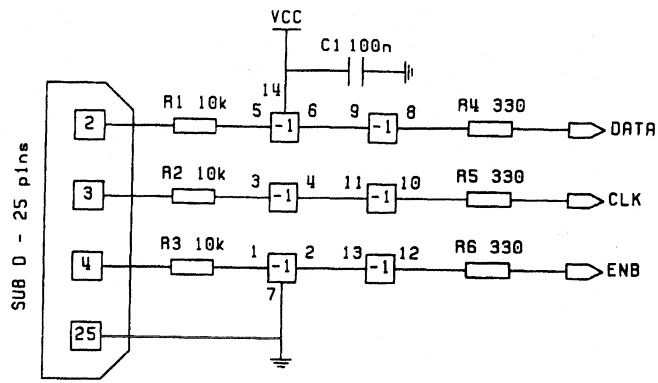
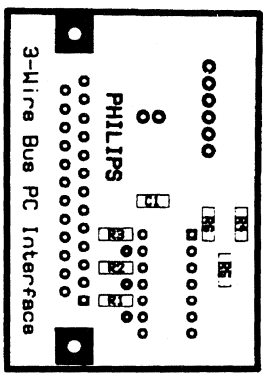
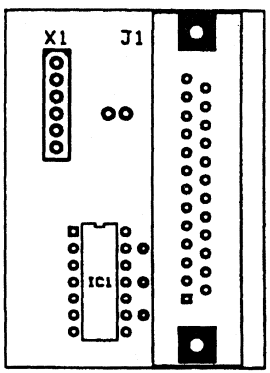
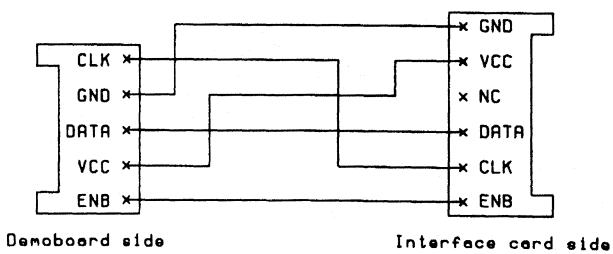

C31
C32
C30 C33
R15
R14
C29
R3
C35
T1
R16
C11
C36
VCO2
C16
R2
VCO1
C14
R21
R24
C6
C13
C15
C5
C8
C18
VCO3
VCOA2
C19
R8
R1
R5
R7
C21
C17
R19
R4
C10
C25
R12
T3
T2
R11
R18
R17
R27
C26
IC2
C28
C27

Figure 18.









Interface card pcb layout and cable connection.

Figure 19.

Summary:

A detailed description of the TEA1094 is given. In conjunction with a member of the TEA106x-family transmission circuits, it offers a handsfree function. It incorporates a microphone amplifier, a loudspeaker amplifier and a duplex controller with signal and noise monitors on the transmit and the receive channel. A cookbook gives the general application steps and also several application examples are given, including listening-in, cordless-base and answering machine.

Note:

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Chapter 1. Introduction

The TEA1094 is a circuit which, in combination with a member of the TEA106x transmission circuits, offers a handsfree function. It incorporates a microphone amplifier, a loudspeaker amplifier and a duplex controller with signal and noise monitors on the transmit and the receive channel. In contrarary with the Philips handsfree circuit TEA1093, the TEA1094 has no integrated supply. This makes the TEA1094 most suitable for applications with mains adapted supply, such as cordless telephones and answering machines.
The function of the handsfree circuit will be illustrated with the help of figure 1.1.

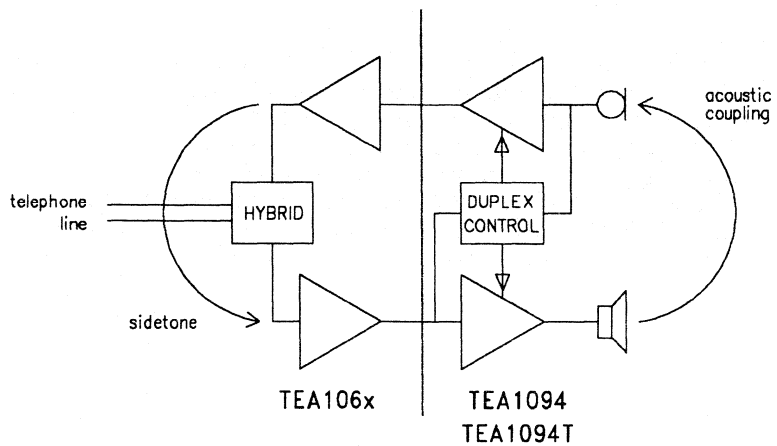


Figure 1.1: Handsfree telephone set principle

The left side of fig. 1.1 shows a principle diagram of a part of the TEA106x circuit by means of a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid. The right side of fig. 1.1 shows a principle diagram of a part of the TEA1094 handsfree circuit by means of a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from fig. 1.1, a closed loop is formed via the amplifiers, the anti side-tone network and the acoustic coupling between loudspeaker and microphone of the handsfree circuit. When the loopgain is higher than one, the set starts howling. In a full-duplex application, this would be the case. To avoid howling, the loop-gain has to be much lower than one and therefore has to be decreased. This is done by the duplex controller.

The duplex controller of the TEA1094 monitors the signal and noise on both the transmit and the receive channel in order to detect which channel contains the 'largest' signal. As a result the duplex controller reduces the gain of the channel which contains the 'smallest' signal. This is done such that the sum of the transmit and receive gain remains constant.

As a result, the circuit can be in three stable modes to be referred to throughout this report:

1. Transmit mode (Tx-mode): the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is reduced.
2. Receive mode (Rx-mode): the gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is reduced.
3. Idle mode (Ix-mode): the gain of the amplifiers are halfway their maximum and reduced value.

The difference between the maximum gain and the reduced gain is called the switching range.

This report gives a detailed description of the TEA1094 and its application with the TEA106x-family. The description is given by means of the block diagram of the TEA1094 (ch.2) and by discussing every detail of the sub-blocks (ch.3). The application is discussed by giving a guideline for application (the application cookbook ch.4) and by giving a number of worked-out applications including listening-in and cordless (ch.5). Also EMC aspects are discussed (ch.6). The appendices contain a measurement setup for the electro-acoustical adjustment of the TEA1094 handsfree application (A), quick reference data of the TEA106x family (B), a list of abbreviations (C) and application diagrams of the TEA1094 (D).

Chapter 2. Block diagram

In this chapter the block diagram of the TEA1094 is shown by means of figure 2.1. The pinning of the TEA1094 is given by means of figure 2.2. Also a short description of the block diagram is given including the function of the external components.

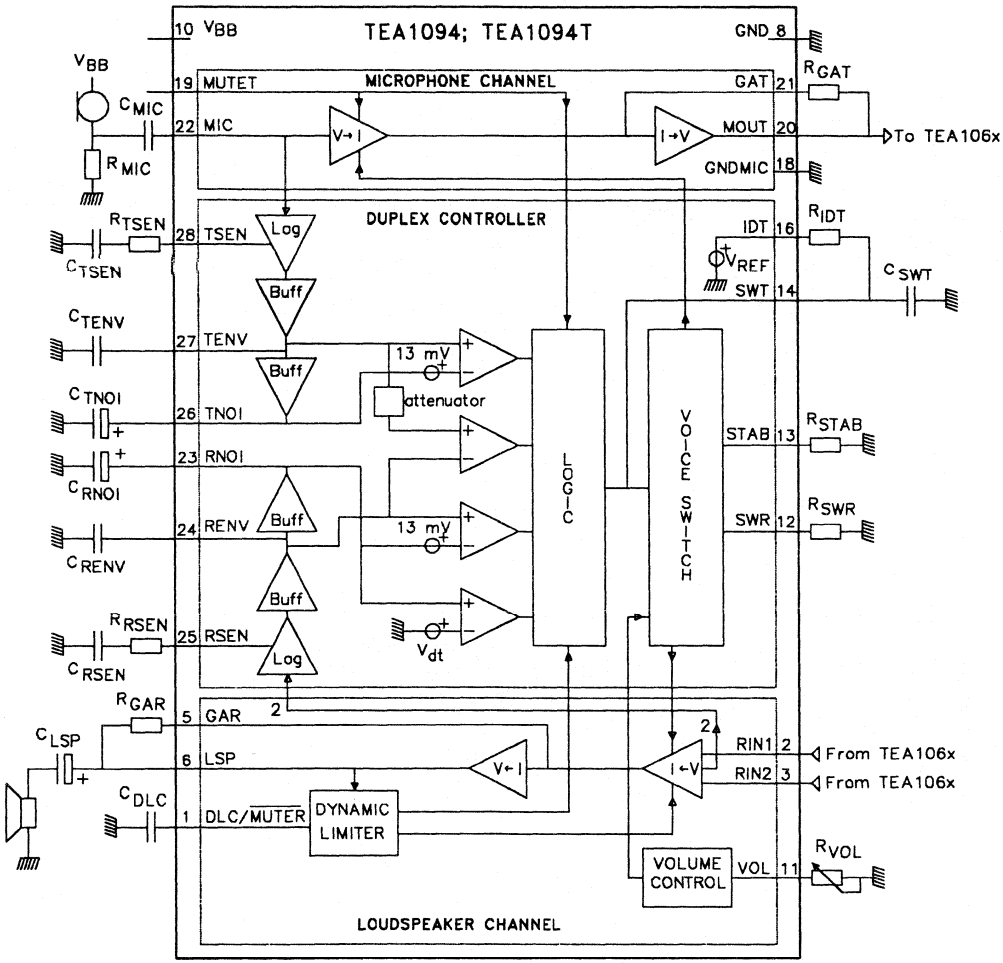
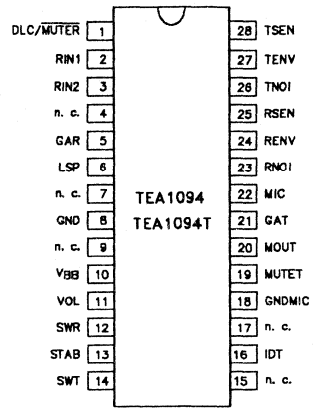


Figure 2.1: Block diagram of TEA1094



Pin	Name	Description
01	DLC/*MUTER*	Dynamic limiter timing adjustment, receiver channel mute input
02	RIN1	Receiver amplifier input 1
03	RIN2	Receiver amplifier input 2
04	N.C.	Not connected
05	GAR	Receiver gain adjustment
06	LSP	Loudspeaker amplifier output
07	N.C.	Not connected
08	GND	Ground reference
09	N.C.	Not connected
10	VBB	Supply output
11	VOL	Receiver volume adjustment
12	SWR	Switching range adjustment
13	STAB	Reference current adjustment
14	SWT	Switch-over timing adjustment
15	N.C.	Not connected
16	IDT	Idle-mode timing adjustment
17	N.C.	Not connected
18	GNDMIC	Ground reference for microphone amplifier
19	MUTET	Transmit channel mute input
20	MOUT	Microphone amplifier output
21	GAT	Microphone gain adjustment
22	MIC	Microphone input
23	RNOI	Receive noise envelope timing adjustment
24	RENV	Receive signal envelope timing adjustment
25	RSEN	Receive signal envelope sensitivity adjustment
26	TNOI	Transmit noise envelope timing adjustment
27	TENV	Transmit signal envelope timing adjustment
28	TSEN	Transmit signal envelope sensitivity adjustment

Figure 2.2: Pinning of the TEA1094

In figure 2.1 it can be seen that the IC consists out of four parts: the supply, the microphone amplifier, the loudspeaker amplifier and the duplex controller. These blocks will be shortly described below including the function of the external components. The detailed description will follow in chapter 3.

Supply:

The circuit is supplied from pin VBB. A supply can be connected between VBB and GND.

Microphone amplifier:

The handsfree microphone signal is amplified from pin MIC to pin MOUT. The signal reference is pin GNDMIC, a 'clean ground' which has to be connected to GND. The sensitivity of the microphone can be set via Rmic, the signal is coupled in via Cmic. The gain of the amplifier can be set with Rgat. The amplifier can be muted by making pin MUTET high.

Loudspeaker amplifier:

A loudspeaker can be connected between output pin LSP and GND. Capacitor Clsp is used to block DC. The gain from the symmetrical input RIN1 and RIN2 to the output can be set via resistor Rgar. The volume of the receive signal can be adjusted by means of a potentiometer Rvol. To minimize distortion of the receive signal a dynamic limiter is incorporated of which the timing can be set with the capacitor Cdlc. The amplifier can be muted by making pin DLC/*MUTER* low.

Duplex controller:

From both the transmit and receive signal, signal and noise envelopes are made. The transmit signal envelope is on pin TENV, the receive signal envelope on pin RENV. The transmit noise envelope is on pin TNOI and the receive envelope noise is on pin RNOI. The timing of the envelopes can be set by the capacitors Ctenv, Ctnoi, Crenv and Crnoi. The sensitivity of the envelope detectors can be set by means of the RC-combinations Rtsen with Ctsen for the transmit envelopes and by Rrsen with Crsen for the receive envelopes. The resistor sets the sensitivity and the capacitor blocks the DC-component. Also a high-pass filter is created.
The logic determines to which mode (Tx,Rx or Ix-mode) the set has to switch over. The timing for switching to the Tx and the Rx-mode is set with capacitor Cswt. The timing for switching to the Ix-mode is set by the combination of Cswt and Ridt. The switching range is set by the resistor Rswr. Resistor Rstab has a fixed value.

Chapter 3. Description of the TEA1093

This chapter describes in detail the four blocks of the handsfree circuit TEA1093: the supply (3.1), the microphone amplifier (3.2), the loudspeaker amplifier (3.3) and the duplex controller (3.4). For each block the principle of operation is described and its adjustments and performance are discussed.

All values given in this chapter are typical and at room temperature unless otherwise stated. For more details of the TEA1094 specification, see [Ref.4].

Chapter 3.1. Supply block

Principle of operation

The TEA1093 handsfree circuit, see [Ref.2], has an integrated supply which effectively stabilizes a supply voltage and powers the loudspeaker out of the linecurrent. The TEA1094 has no integrated supply. This makes the TEA1094 most suitable for applications where the handsfree circuit is supplied from an external voltage source.

In figure 3.1.1, the supply arrangement of a TEA1094 with a TEA106x is shown.

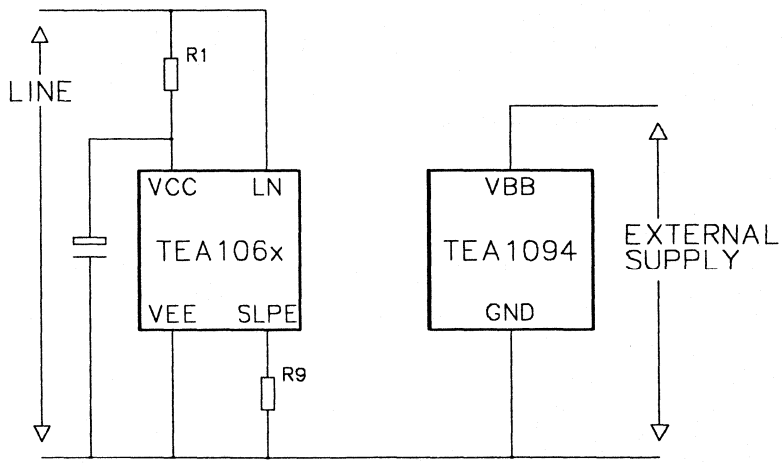


Figure 3.1.1: Supply arrangement TEA1094

As can be seen, the linecurrent flows through the TEA106x, while the TEA1094 is supplied from an external voltage source. The voltage source is connected between VBB and GND, while GND is connected to VEE of the TEA106x. In this way one reference for all signals is created.
It is also possible to connect the reference GND of the TEA1094 to pin SLPE of the TEA106x. In this way two references are created, SLPE and VEE. This makes the interconnection between the TEA1094 and the TEA106x less simple. This is also done in the line-powered applications of the TEA1093. Please refer to [Ref.5] for more details.

In case a line-powered handsfree application is made, preferably the TEA1093 is used because of its integrated supply. However, when the TEA1094 is used, the circuit can be supplied from the line via a large coil connected between the line and VBB. At VBB a capacitor has to be connected to serve as a reservoir. In this application, the TEA1094 has to be referenced to SLPE in order not to influence the transmission characteristics.

In figure 3.1.1 no galvanic seperation is drawn. When such is needed, the seperation can be done in the supply part or in the signal interfacing. In the supply part the galvanic seperation can be made in the mains-adapter. In the signal interfacing between the TEA1094 and the TEA106x, the galvanic seperation can be done either with transformers or opto-couplers. In chapter 5, application proposals which include galvanic seperation are given for a cordless telephone with handsfree base and for a telephone with answering machine.

Adjustments and performance

The voltage which can be applied between VBB and GND may vary between 3.3V and 12V. In case a lower voltage is applied, the circuit will strongly reduce the loudspeaker outputlevel, see chapter 3.3.3. The 12V is an absolute maximum rating. When a supply is used which, during transitions, can generate higher voltages, a 12V protection zener has to be applied between VBB and GND.

The current consumption of the TEA1094 is specified as Ibb=3.8mA at Vbb=5V. At higher voltages the current consumption slightly increases up to Ibb=4.8mA at Vbb=12V.

Chapter 3.2. Microphone amplifier block

In the first paragraph of this chapter the principle of operation of the microphone amplifier is described as well as its adjustments and performance. In the second paragraph, the mute transmit function is discussed.

3.2.1. Microphone amplifier.

Principle of operation

In figure 3.2.1 the block diagram of the microphone amplifier of the TEA1094 is depicted together with the interconnection with the TEA106x.

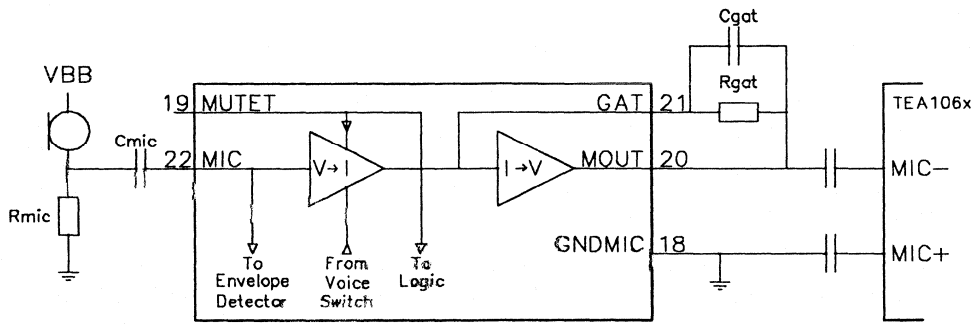


Figure 3.2.1: Block diagram of the microphone amplifier

As can be seen in figure 3.2.1, the microphone amplifier is referenced to pin GNDMIC instead of referenced to pin GND. This in order to prevent interference from other blocks within the TEA1094 (so called clean ground). The input and output signals of the microphone channel have to be referenced to GNDMIC. Pin GNDMIC itself has to be referenced to GND.

The input of the microphone amplifier is pin MIC. It is an a-symmetrical input well suited for electret microphones. Induced signals in the short wire between the microphone and pin MIC are assumed to be negligible. This in contrary with the handset microphone which is connected to the set via a long cord. The TEA106x family therefore has symmetrical microphone inputs.
The output of the microphone amplifier is pin MOUT. When interconnecting the TEA1094 and the TEA106x, pin MOUT is preferably connected to the TEA106x input pin MIC-. In that case the MIC+ pin of the TEA106x is connected to pin GNDMIC. It is advised not to reverse this interconnection.

As can be seen in figure 3.2.1, the microphone amplifier itself is built up out of two parts: a pre-amplifier and an end-amplifier. The gain of the pre-amplifier is determined by the duplex controller block, see chapter 3.4. The gain of the end-amplifier is determined by the external feedback resistor Rgat.

The overall gain (Atx) of the microphone amplifier from input MIC to output MOUT in Tx-mode is given as:

$$Atx = 20 * \log (0.674 * Rgat / Rstab).$$

With Rstab being the resistor at STAB of 3.65kΩ.

Adjustments and performance

A handsfree microphone, referenced to GNDMIC, can be connected to the input MIC via a DC blocking capacitor Cmic. Together with the input impedance of pin MIC of 20kΩ, Cmic forms a first order high-pass filter.
The handsfree electret microphone can be supplied from VBB. However, during normal operation VBB will contain a small ripple, for instance due to large loudspeaker signals. Electret microphones with a small power supply rejection ratio should therefore be connected via an RC smoothing filter as depicted in figure 3.2.2.

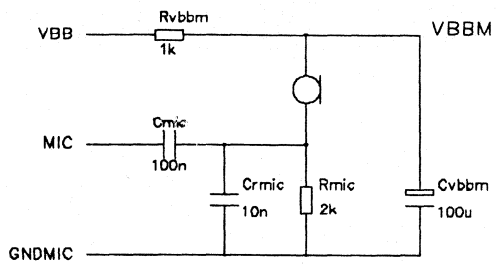


Figure 3.2.2: Supply arrangement for an electret microphone

As shown in figure 3.2.2, the RC smoothing filter is referenced to GNDMIC to have one ground reference for the whole microphone signal path. On the printed circuit board lay-out GNDMIC can best be connected with a separate wire to pin VEE of the TEA106x to reduce ground interference to a minimum.
The sensitivity of the electret microphone is set via resistor Rmic. By placing a capacitor Crmic over this resistor a first order low-pass filter is formed for the microphone signal.

Via the resistor Rgat, the gain of the microphone amplifier can be adjusted from 5dB to 25dB to suit application specific requirements. With resistor Rgat=30.1kΩ the gain equals 15dB with a tolerance of ±2dB.
Capacitor Cgat is applied in parallel with resistor Rgat to ensure stability of the microphone amplifier. Together with Rgat it also provides a first order low pass filter.

The input of the microphone amplifier can handle signals up to 18mVrms with 2% total harmonic distortion. However the microphone input signal is also used by the duplex controller, see chapter 3.4. At 10mVpeak at the input the positive part of the signal on pin TSEN starts clipping which might influence the switching behaviour. It is therefore advisory to keep the microphone input signal below this level.
The output drive capability at pin MOUT is 20μArms.

The output noise at MOUT of the TEA1094 is -100dBmp (psophometrically weighted P53-curve) at a gain of 15dB. With a sending gain of the TEA106x of 44dB the noise level on the line will be -56dBmp. The noise level of the TEA1094 is linear with the transmit gain. This means that at a transmit gain of 25dB the noiselevel at MOUT will be -90dBmp.
In transmit mode, the noise level will be at its maximum. In idle mode and receive mode, the noise level at MOUT will be lower because the contribution of the preamplifier is reduced then. However, the bottom level of the sending noise at MOUT is determined by the end-amplifier and is about -110dBmp, independent on gain.
The bottom level of the sending noise on the line is determined either by the TEA106x itself or by the noise at MOUT increased with the transmit gain of the TEA106x, whichever is largest. When, in receive mode, the noise on the line is determined by the noise at MOUT, it can be reduced by placing an attenuator between output MOUT and input MIC-. The attenuation has to be compensated by increasing the transmit gain of the TEA1094 with the same amount. Eventually, with enough attenuation, the bottom level of the sending noise on the line will be determined by the TEA106x itself. The use of an attenuator will not influence the amount of noise in transmit mode.
An application example with an attenuation network can be found in chapter 5. For the influence of the attenuator on the noise at the loudspeaker outputs, see chapter 3.3.1.

3.2.2. Mute transmit

During handsfree operation the microphone can be muted via MUTET so conversation cannot be heard by the other party. When the microphone amplifier is muted, automatically the TEA1094 switches over to Rx mode, see also chapter 3.4.
When a logic high is applied to MUTET, meaning the voltage on MUTET is higher than 1.5 Volts, the microphone pre-amplifier is muted. The end-amplifier can still be used by applying a signal on GAT. The obtained gain reduction is 80dB. The current which has to be sourced into pin MUTET when MUTET is high, is 5μA maximum.
When MUTET is a logic low, meaning the voltage on MUTET is lower than 0.3 Volts or pin MUTET is left open, the microphone amplifier is not muted.
The maximum allowable voltage on MUTET is VBB+0.4V, the minimum allowable voltage on MUTET is GND-0.4V.

Chapter 3.3. Loudspeaker amplifier block

The block diagram of the complete loudspeaker amplifier block is depicted in figure 3.3.1.

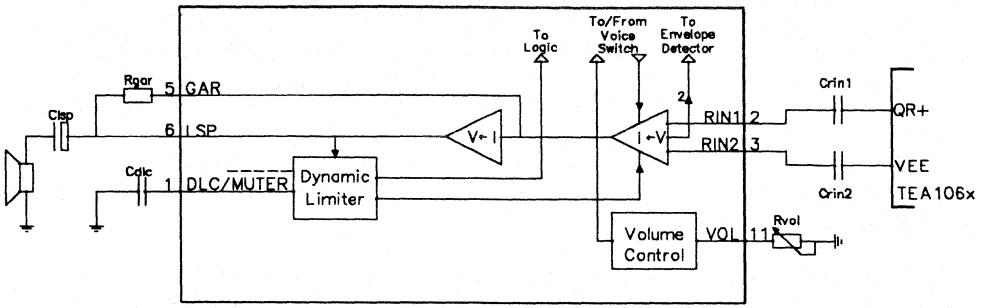


Figure 3.3.1: Principle of the loudspeaker amplifier

As can be seen in figure 3.3.1, the loudspeaker amplifier is built up out of three parts: the loudspeaker amplifier itself, volume control and dynamic limiter. In the first paragraph of this chapter the principle of operation of the loudspeaker amplifier is described as well as its adjustments and performance. In the second paragraph the same items are discussed of the volume control part and in the third paragraph of the dynamic limiter part. In paragraph 4 it is described how the receiver can be muted.

3.3.1. Loudspeaker amplifier

Principle of operation

As can be seen in figure 3.3.1 the input of the loudspeaker amplifier, pins RIN1 and RIN2, is symmetrical. The input RIN1 can be connected, via a capacitor, to the earpiece output QR+ of the TEA106x. When the TEA1094 is referenced to VEE, the other input RIN2 can be left open. In all other cases, RIN2 has to be connected, via a capacitor, to pin VEE of the TEA106x.
At the loudspeaker output LSP, the amplified receiving signal from QR+ is available. The output can drive a loudspeaker which is connected, via a capacitor, to GND.

As can be seen in figure 3.3.1, the amplifier itself is built up out of two parts: a pre-amplifier and an end-amplifier. The gain of the pre-amplifier is determined by the duplex controller block, see chapter 3.4. The gain of the end-amplifier is determined by the external feedback resistor Rgar. The overall gain of the loudspeaker amplifier (Arx) from inputs RIN1 and RIN2 to the output LSP in Rx-mode is given as:

$$Arx = 20 * \log (0.435 * Rgar / Rstab) \text{ dB}.$$

With Rstab being the resistor at STAB of 3.65kΩ.

Adjustments and performance

The input signal for the loudspeaker amplifier has to be coupled in via the capacitor Crin1 to block DC. Together with the input impedance of 20kΩ at RIN1, a first order high pass filter is introduced. When connecting the other input RIN2 to VEE, this also has to be done via a capacitor. This capacitor Crin2 preferably has the same value as Crin1 to obtain a good common mode rejection ratio. The input impedance of RIN2 is also 20kΩ.
The inputs can handle signals up to 390mVrms with a total harmonic distortion of 2%. Because of this it is advised not to connect RIN2 to QR- but only to VEE. The inputs RIN1 and RIN2 are biassed at around zero volts with respect to GND. By applying a signal to the inputs, they can become negative. The protection on these pins however is made different from other pins which makes it possible to make RIN1 and RIN2 as low as -1.2V without damaging the circuit.

A loudspeaker can be connected to the TEA1094 between LSP and GND. For the output is biassed at Vbb/2, a capacitor must be placed in series with the loudspeaker to block DC-current. Together with the impedance of the loudspeaker also a high pass filter is formed. Via the resistor Rgar, the gain of the loudspeaker amplifier can be adjusted from 3dB to 33dB. With resistor Rgar=66.5kΩ, the gain equals 18dB with a tolerance of ±2dB. A capacitor Cgar can be applied in parallel with resistor Rgar to provide a first order low pass filter.

In mains-adapted powered applications, the output power of the TEA1094 loudspeaker amplifier is limited by the maximum output current and the maximum output voltage swing. The maximum output current is dependent on the current the supply can deliver. The maximum output voltage swing is determined by the voltage supplied on VBB. For maximum voltage swing, the end-amplifier has a rail to rail output stage. The maximum voltage swing is dependent on the output current and the temperature, see also chapter 3.3.3.

In figure 3.3.2, the maximum output power in an 8Ω, 25Ω and 50Ω loudspeaker is depicted as a function of the voltage at VBB.

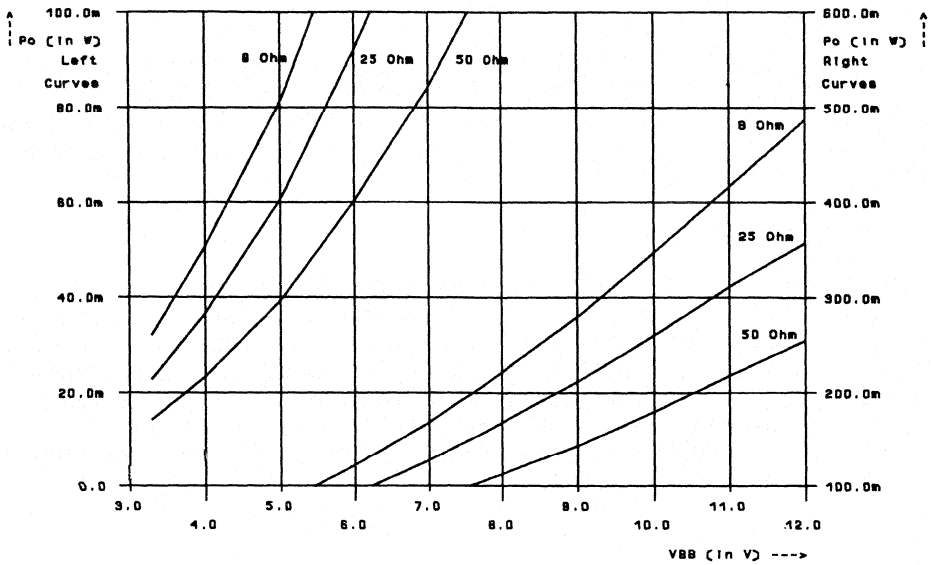


Figure 3.3.2: Maximum output power in the loudspeaker

The absolute maximum possible output power is limited by the maximum possible output current of the loudspeaker amplifier end-stage which is around 500mA peak. It is advised not to exceed this value since it might damage the output stage transistors.

The noise level at the output LSP is 80μVrms at a gain of 18dB and with the inputs RIN1 and RIN2 shorted with 200Ω. However in an application with the TEA106x, the noise at the outputs is larger than 80μVrms. This is due to the fact that the noise generated in the transmit channel of the telephone set is fed back via the sidetone network to the receive channel and is amplified to the loudspeaker outputs.
The maximum noise level at the loudspeaker outputs can be perceived in receive mode. With for instance an electrical sidetone of -12dB, and an overall receive gain of 24dB, the noise level at the loudspeaker output will be 12dB higher than the bottom level of the sending noise on the line. With the figures given in chapter 3.2.1 (-110dBmp at MOUT, transmit gain of the TEA106x of 44dB, thus -66dBmp on the line) this will lead to -54dBmp at the loudspeaker outputs. This level can be reduced by placing an attenuation network between MOUT and MIC- as described in chapter 3.2.1. Depending on the TEA106x used, the bottom level of the sending noise on the line can become lower than -77dBmp (44dB sending gain of the TEA106x) resulting in less than -65dBmp at the loudspeaker outputs.

3.3.2. Volume control

Principle of operation

Via the volume control block, the volume of the loudspeaker signal can be adjusted by the external potmeter Rvol connected to pin VOL. By turning the potentiometer, the gain of the loudspeaker pre-amplifier is varied. Volume control may not affect the transmit gain in transmit mode. To obtain this, the volume control acts upon the pre-amplifier via the duplex controller, see also chapter 3.4.

Adjustments and performance

Out of pin VOL a current Ivol, set by Rstab, see chapter 3.4, is flowing which is proportional to the absolute temperature (PTAT). At roomtemperature this current is around 10μA. Together with the resistance of the potmeter Rvol, the current Ivol creates a PTAT voltage on pin VOL. This PTAT voltage is processed by the volume control block. As a result, a temperature independent volume reduction in the loudspeaker signal of 3dB is obtained at approximately every 950Ω variation of the potentiometer Rvol.
This means that a linear potentiometer can be used to control the volume logarithmical, thus in dB's. With the advised value for Rvol of 10kΩ, the maximum gain reduction of the volume control is more than 30dB. The maximum gain reduction however is limited by the switching range, see chapter 3.4. When the resistor Rvol is zero, the receive gain is not influenced.

When digital volume control is desired this can be done as depicted in figure 3.3.3.

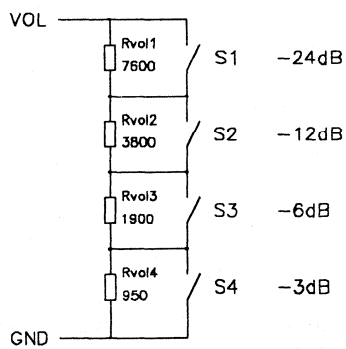


Figure 3.3.3: Digital volume control

With the 4 bit digital volume control of figure 3.3.3, 16 volume levels can be set via steps of 3dB (from 0dB to a maximum of 45dB of attenuation). The switches can be either MOSFETs or analogue switches, for instance the Philips HCT4066 type. It is advised not to use bipolar transistors as switches because of the saturation voltage of these devices. When a voltage is applied to pin VOL to control the volume, preferably this voltage has to be a PTAT voltage source. If not, the obtained gain reduction is no longer temperature compensated.

3.3.3. Dynamic limiter

Principle of operation

The dynamic limiter minimizes the distortion of the output signal by reducing the gain of the loudspeaker pre-amplifier when the output signal starts clipping or when too low supply conditions are detected. The amount of gain reduction is determined by the voltage on pin DLC/*MUTER*. This voltage is varied by charging and discharging the capacitor Cdlc. The combination of charge and discharge currents and the capacitance of Cdlc sets the timing of the dynamic limiter.

Clipping of the loudspeaker output signal occurs when the output transistors are driven into deep saturation. To prevent hard clipping, deep saturation has to be prevented. The saturation voltage of the output transistors strongly depends on the output current and the temperature. In the dynamic limiter of the TEA1094 these effects are taken into account to have maximum output swing under any condition.
When the dynamic limiter detects the beginning of saturation, the capacitor Cdlc is discharged fast with a current of approximately 1mA, see figure 3.3.4 left hand side. As a result, the gain of the loudspeaker amplifier is reduced. The loudspeaker amplifier stays in its reduced gain mode until the peaks of the loudspeaker signal no longer start to cause saturation. The gain then slowly returns to its normal value by charging Cdlc with a current of 1µA, see figure 3.3.4 right hand side. In this way it is ensured that always the maximum reachable output power can be obtained at low distortion.

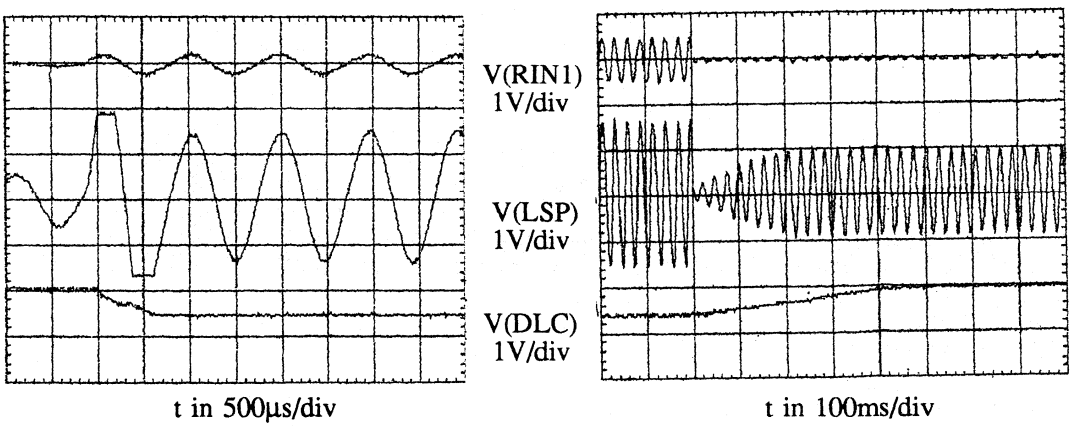


Figure 3.3.4: Action of the dynamic limiter clipping detector

Under too low supply conditions, the gain of the loudspeaker amplifier is reduced in order to prevent the TEA1094 from malfunctioning. Only the gain of the loudspeaker amplifier is affected since it is considered to be the major power consuming part. When the supply voltage drops below the internal threshold of 2.9V, the gain is reduced immediately regardless of the voltage on pin DLC. However, the capacitor Cdlc is also discharged to ensure stable operation of the limiter.

Adjustments and performance

The timing of the dynamic limiter is determined by the charge and discharge currents and by the capacitor Cdlc. The currents are internally fixed and cannot be changed. All charge and discharge time constants, and therefore the dynamic limiter timing, are proportional to the value of Cdlc. The only exception is when VBB drops below its threshold. In that case the gain is reduced immediately regardless of the voltage on Cdlc.
As a compromise between attack and release times of the dynamic limiter a capacitor of 470nF is advised. Larger values will give a smoother (slower) response while smaller values may lead to more distortion at lower frequencies. It is advised not to use a capacitor with a high leakage current in order not to influence the behaviour of the dynamic limiter.
If only a faster attack time is desired, it is possible to connect a low ohmic resistor in series with Cdlc of maximum 100Ω. In that case the relatively high discharge currents (200μA-1mA) will cause an instantaneous drop on pin DLC/$\overline{MUTER}$ when limiting action is needed. The instantaneous drop caused by the small charge current of 1μA will be negligible.

With Cdlc=470nF, the attack time for the clipping detector is in the order of a few milliseconds. The attack time when the circuit runs out of current is in the order of several seconds. The attack time when the supply voltage VBB drops below the threshold of 2.75Volts is less than 1 millisecond. The release time in all cases is in the order of a few 10 milliseconds.

When the dynamic limiter is acting, in practice the distortion of the output stage will stay below 5%. The dynamic limiter does not limit the distortion of the input stage.

Start-up behaviour

When the TEA1094 is started up, the starter of the dynamic limiter charges the capacitor Cdlc with a current of approximately 80μA. The starter stops when the voltage at DLC/$\overline{MUTER}$ has reached a value of around 1.6V. Then a current of 1μA charges the capacitor further, up to a voltage of around 1.9V. At that point the voltage on DLC/$\overline{MUTER}$ is limited. The starter restarts when the voltage at DLC/$\overline{MUTER}$ drops below 200mV.

3.3.4. Mute receive

The loudspeaker amplifier can be muted by making pin DLC/$\overline{MUTER}$ lower than 200mV. As a result the gain of the loudspeaker amplifier is reduced with 80dB. Also the circuit is internally forced into Tx-mode.
Pin DLC/$\overline{MUTER}$ can be made low by placing a switch over the capacitor, for instance a simple transistor.
When the switch is open, nothing is influenced. When the switch is closed and DLC/$\overline{MUTER}$ is put below 200mV, the loudspeaker pre-amplifier is muted. The end-amplifier can still be used by applying a signal on GAR. Because the starter is reactivated when the voltage on DLC/$\overline{MUTER}$ is smaller than 200mV, the switch must be able to sink approximately 80μA. When the switch is opened again, the starter will recharge the capacitor Cdlc.
The minimum allowable voltage on DLC/$\overline{MUTER}$ is GND-0.4V.

Chapter 3.4. Duplex controller block

In this chapter the principle of operation of the complete duplex controller will be discussed as well as its adjustments and performance. This will be done with the aid of figure 3.4.1, where the complete duplex controller is depicted.

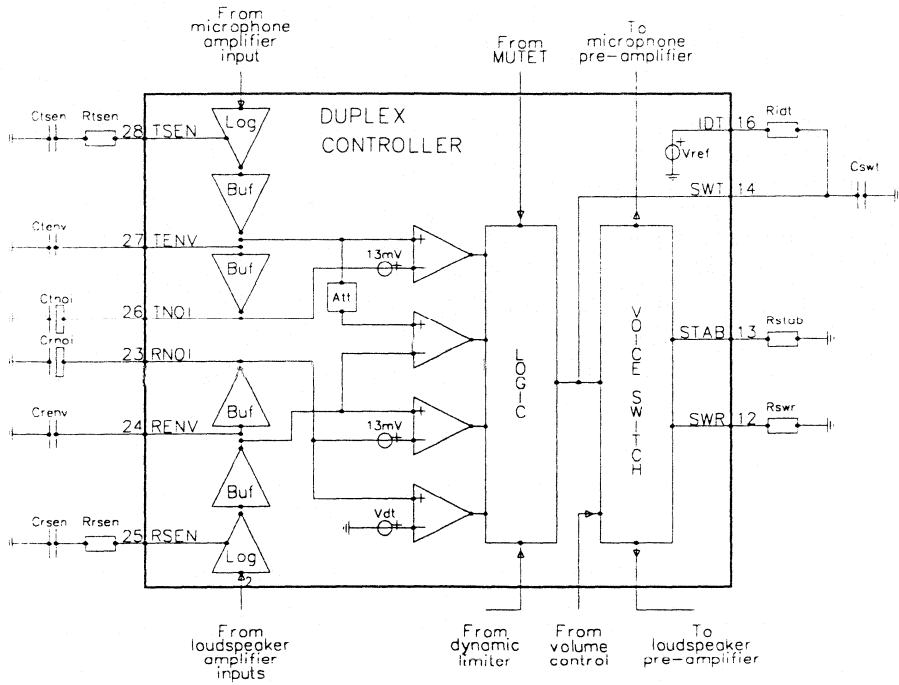


Figure 3.4.1: Principle of the duplex controller

As can be seen in figure 3.4.1, the duplex controller is built up out of signal and noise envelope detectors, decision logic and a voice switch.
The signal and noise envelope detectors determine the signal envelope and the noise envelope of both the transmit and receive signal. These envelopes are used by the decision logic to determine to which mode the set has to switch over (Tx, Rx or Ix-mode). The logic charges and discharges the capacitor Cswt and the resulting voltage on pin SWT controls the voice switch. The voice switch switches over the set between the three modes while keeping the loopgain constant.
In paragraphs 3.4.1 to 3.4.3, the principle of operation of the three parts is given. In paragraph 3.4.4, the adjustments and performance of the complete duplex controller is given.

3.4.1. Signal and noise envelope detectors

The signal and noise monitors of the transmit and receive channel are globally the same. The principle of the detectors therefore will be explained with the help of one of them: the signal and noise envelope detector of the transmit channel.
The microphone signal on MIC is connected to the first stage of the detector, see figure 3.4.1. The first stage amplifies the microphone signal from MIC to TSEN with an internally fixed gain of 40dB. Via the RC combination RtsenCtsen the signal on TSEN is converted into a current. This conversion determines the sensitivity of the envelope detectors. The current is logarithmically compressed and internally converted to a voltage. This voltage thus represents the compressed microphone signal. At roomtemperature, an increase of the microphone signal with a factor of 2 will increase the signal envelope with 18mV if the current through TSEN stays between 0.8μArms and 160μArms. Outside this region the compression is less accurate.
The compressed microphone signal is buffered by the second stage to pin TENV. Because the buffer can source maximum 120μA and sink maximum 1μA, the signal on TENV follows the positive peaks of the compressed signal. This is called the signal envelope. The time constants of the signal envelope are therefore determined by the combination of the internal current sources and the capacitor Ctenv.
The voltage on TENV is buffered by the third stage to pin TNOI. Because this buffer can source maximum 1μA and sink maximum 120μA, the signal on TNOI follows the negative peaks of the signal on TENV. This is called the noise envelope because it represents the background noise. The time constants of the noise envelope are therefore determined by the combination of the internal current sources and the capacitor Ctnoi. Both capacitors Ctnoi and Crnoi are provided with a start circuit. During startup the capacitors are charged with approximately 40μA up to 1.9V. The starter will restart when the voltage on the capacitor drops below 0.9V.
As can be seen in figure 3.4.1, the principle of operation of the signal and noise envelope detectors of the receive channel is equal to that of the transmit channel. However, the gain of the first stage (inputs to pin RSEN) is 0dB and not 40dB as in case of the transmit channel.

The behaviour of the envelopes is illustrated in figure 3.4.2, where the signal and noise envelope of the receive channel (RENV, RNOI) are depicted together with the input signal on RIN1.

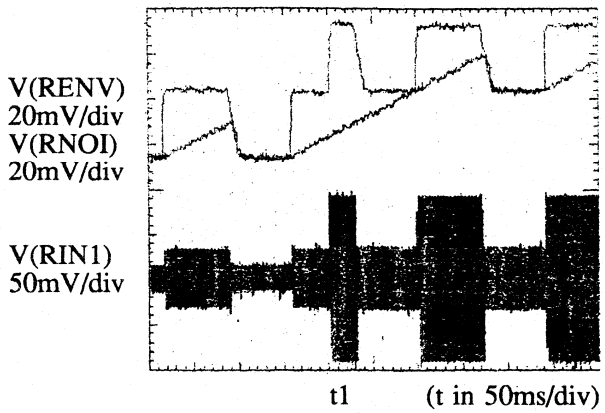


Figure 3.4.2: Typical behaviour of the signal and noise envelope detectors

In figure 3.4.2, the amplitude of the 1kHz input signal at RIN1 is modulated with 10dB and at moment t1 an extra 10dB is added. When, during modulation, the input signal is raised with 10dB, the signal envelope at RENV immediately follows. When the input signal drops with 10dB, the signal envelope drops less quick, thus reducing the influence of room echo. The noise envelope at RNOI slowly follows the signal envelope but never crosses it. When at t1 the extra 10dB is added, the signal envelope also increases but due to the logarithmic compression, the variation in the signal envelope due to the 10dB modulation is the same before and after t1.

3.4.2. Decision logic

The signal and noise envelopes of the transmit and receive signal are used by the decision logic to determine in which mode the TEA1094 has to be.
The output of the logic is a current source which charges or discharges the capacitor Cswt. If the logic determines Tx-mode, the capacitor Cswt is discharged with 10μA. When Rx-mode is determined, Cswt is charged with 10μA. When Ix-mode is determined, the current source is zero and the voltage on SWT becomes equal to the voltage on IDT via the resistor Ridt. The time constants of the duplex controller are therefore determined by the combination of the internal current source, the capacitor Cswt and the resistor Ridt.

As can be seen in figure 3.4.1, the envelopes are not used directly by the decision logic. First, to have a clear choice between signal and noise, the signal is considered as speech when its envelope is more than 4.3dB above the noise envelope. At room temperature, this is equal to a voltage difference of 13mV. This so called speech/noise threshold is implemented in both the transmit and receive channel. At the end of paragraph 3.4.4 a way to increase this threshold is discussed.
Second, the signal on MIC contains both the signal of the talker using the set as well as the signal coming from the loudspeaker (acoustic coupling). In Rx-mode, the contribution of the loudspeaker overrules the contribution of the talker using the handsfree telephone set. As a result, the signal envelope on TENV is mainly formed by the loudspeaker signal. To correct this, an attenuator is placed between TENV and the TENV/RENV comparator. This attenuation equals the attenuation applied to the microphone amplifier gain. Thus

when the TEA1094 is in Rx-mode the attenuation equals the switching range.
Third, when a dial tone is present on the line, without measures this would be recognized as noise. This would happen because it is a signal with a constant level during a long period. As a result the TEA1094 would go to Ix-mode and the user of the set would hear the dial tone fade away. Therefore, a dial tone detector is incorporated which does not consider input signals as noise when they have a level higher than the dial tone level. The dial tone level is adjustable by Rrsen.
When these three corrections are made, the signal and noise envelopes are used by the comparators and the logic. As already explained the output of the logic is a current source. The relation between the current source and the output of the comparators is given in the table of figure 3.4.3. If, for instance, TENV>RENV (transmit signal is larger than receive signal) and TENV>TNOI (transmit signal more than 4.3dB larger than noise level), then the output current will be -10μA.

Comparator TENV / TNOI	1	x	x	0	x
Comparator TENV / RENV	1	0	0	1	0
Comparator RENV / RNOI	x	1	x	x	0
Comparator RNOI / Vdt	x	x	1	x	0
Output current	-10μA	+10μA	+10μA	0μA	0μA

Figure 3.4.3: Truth table of the decision logic

When MUTET is made high, see paragraph 3.2.2, the output current is forced to be 10μA, which forces the TEA1094 into Rx-mode and mutes the microphone amplifier. When pin DLC/*MUTER* is made lower than 200mV, see paragraph 3.3.4, the output current is forced to be -10μA which forces the set into Tx-mode and mutes the loudspeaker amplifier. When both MUTET is made high and DLC/*MUTER* is made low the output current is forced to be -10μA and both channels are muted.
The voltage on pin SWT is internally limited to IDT+400mV and IDT-400mV.

3.4.3 Voice switch

With the voltage on SWT, the voice switch regulates the gain of the microphone pre-amplifier and the loudspeaker pre-amplifier in such a way that the sum of the transmit and receive gain is kept constant. This is done to keep the loopgain of a handsfree telephoneset constant, see also the introduction chapter 1. The switch-over behaviour of the voice switch will be described with the aid of figure 3.4.4.

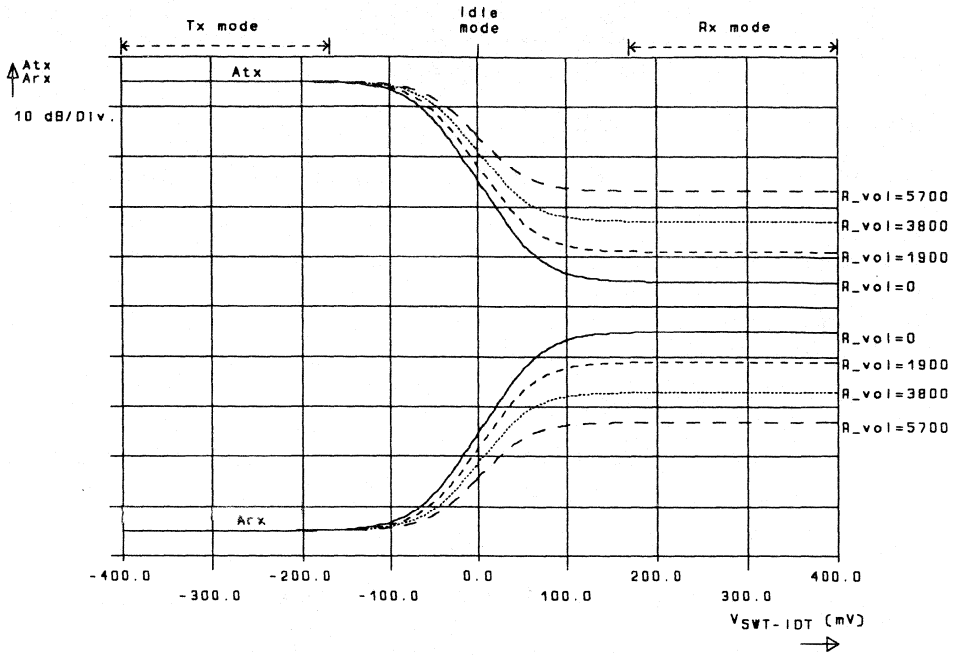


Figure 3.4.4: Switch-over behaviour

When the voltage on SWT is more than 180mV below the voltage on IDT, the TEA1094 is fully switched to Tx-mode (gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum). When the voltage on SWT is more than 180mV above the voltage on IDT, the TEA1094 is fully switched to Rx-mode (gain of the microphone amplifier is at its minimum and the gain of the loudspeaker amplifier is at its maximum). The TEA1094 is considered to be in Ix-mode when the voltage on SWT equals the voltage on IDT. When the capacitor Cswt is charged or discharged, the voltage on SWT varies and as a result the voice switch will smoothly switch over between the modes.

The difference between the maximum and minimum gain of the loudspeaker or microphone pre-amplifier is called the switching range. This range is determined by the ratio of Rswr and Rstab, see paragraph 3.4.4. Both Rswr and Rstab set internally used reference currents which are proportional to absolute temperature (PTAT).

As already stated in chapter 3.3, the volume control does not directly act upon the loudspeaker amplifier gain but via the voice switch. As a result, the loopgain of the handsfree set is kept constant when the volume of the loudspeaker signal is adjusted. The voice switch however, is designed such that the volume control has no influence in Tx-mode. Therefore during transmit, the gain of the microphone amplifier of the TEA1094 is not affected. In the extreme case, which is not plotted in figure 3.4.4, that the volume of the loudspeaker signal is reduced with the switching range, the TEA1094 virtually does not switch over. It also follows from this plot that when it was possible to have a volume

reduction larger than the switching range, the gain of the loudspeaker amplifier would be smaller in Rx-mode than in Tx-mode. To avoid this, the volume control range of the TEA1094 can not be made larger than the switching range.

3.4.4. Adjustments and performance

The adjustment of the duplex controller has to be performed according the following recipe:

1. Determine switching range
2. Determine dial tone detector level
3. Determine sensitivity
4. Determine timings.

Ad 1. Determine switching range

The switching range Asw is determined by the ratio of the two resistors Rstab and Rswr according:

$$Asw = 20 * \log (Rswr / Rstab) \text{ (in dB)}.$$

The resistor Rstab has to be taken 3.65kΩ. The resistor Rswr can be varied between 3.65kΩ and 1.5MΩ resulting in a switching range between 0dB and 52dB. With Rswr is 365kΩ, the switching range is set to 40dB with a tolerance of ±3.5dB.

The switching range is calculated out of the loopgain (Aloop). In a handsfree application the loopgain has to be smaller than 1 (equivalent to 0dB) and can be calculated as follows:

$$Aloop = Atx1094 + Atx106x + Ast + Arx106x + Arx1094 + Aac - Asw \text{ (in dB)}.$$

With Atx1094 = sending gain of the TEA1094 (MIC to MOUT)
Atx106x = sending gain of the TEA106x (MIC+/- to LN)
Ast = electrical sidetone
Arx106x = receive gain of the TEA106x (LN to QR+)
Arx1094 = receive gain of the TEA1094 (RIN1/2 to LSP)
Aac = electro-acoustic coupling from loudspeaker to microphone (LSP to MIC)
Asw = switching range.

For safety, the switching range Asw has to be chosen such that the maximum loop gain is far below 0dB (between -10dB and -20dB). Therefore, in calculations the worst case Ast and Aac have to be taken.
The electrical sidetone is the difference (in dB's) between the wanted receive signal on pin IR of the TEA106x and the unwanted part of the transmit signal on pin IR while having an equal signal level on pin LN for both the transmit and the receive signal. The electrical sidetone is dependent on linelength and frequency. The worst case sidetone can be found by measuring the sidetone over the telephonyband for several linelengths. The acoustic coupling is dependent on the environment of the telephoneset. A way of determining the worst case acoustic coupling is to move a hand to the set as if pushing a button.
When automatic line loss compensation (AGC) is used, the transmit and receive gain of the TEA106x are reduced at high line currents (short lines), see [Ref.1]. This will reduce

the loopgain at high line currents and makes the use of a smaller switching range possible. If a certain minimum volume control range is required, the switching range must not be chosen smaller than the required volume control range.
In appendix A, a method for measuring the required switching range is given.

Ad 2. Determine dial tone detector level

The dial tone detector level is determined by the value of Rrsen according:

$$Vdialtone = 12.7\mu * Rrsen \text{ (in Vrms)}.$$

With an Rrsen of 10kΩ, the dial tone detector level will be 127mVrms. This means, a continuous signal on the inputs RIN1 and RIN2 larger than 127mVrms will be recognized as a dial tone.

Ad 3. Determine sensitivity

The sensitivity is set by Rrsen and Rtsen. The resistor Rrsen is already determined by the dial tone detector level. It must however be checked if the chosen value for Rrsen is a practical one. The reason for this is the dynamic range of the logarithmic compressor. A 'linear' compression is guaranteed when the currents flowing through pin RSEN are between 0.8μArms and 160μArms. This means that at nominal receiving signals the current through RSEN is preferably around 11μArms. This gives a maximum dynamic range of plus and minus 23dB. The same counts for pin TSEN.

The resistor Rtsen has to be chosen in such a way that both channels have the same priority for the duplex controller. This can be obtained by choosing Rtsen according:

$$20 * \log(Rtsen) = 20 * \log(Rrsen) - Atx1094 - Atx106x - Ast - Arx106x + Atsen + \tfrac{1}{2} * Aloop \text{ (in dB)}.$$

With Atsen = internal gain from MIC to TSEN = 40dB.

In this relation, the maximum loopgain and the worst case sidetone are used, see also Ad1. If it is preferred to give the transmit channel priority above the receive channel, Rtsen has to be made smaller. When the opposite is the case, Rtsen has to be made larger. With respect to the calculated setting, resistor Rtsen can be varied with plus and minus ½ * Aloop (in dB's).
In appendix A, a method for measuring the required Rtsen is given.

The capacitors Ctsen and Crsen form a first order high pass RC-filter with Rtsen and Rrsen respectively to reduce the influence of low frequency bumps on the switching behaviour. It is advised to choose the capacitors Ctsen and Crsen such that the corner frequency of the RC-filters are equal.

When the calculated sensitivity setting is implemented, subjective tests with a real telephone line will be necessary to come to the optimal sensitivity setting.

Ad 4. Determine timings.

The timings which can be set are: signal envelope timing and noise envelope timing for both channels, switchover timing and idling timing.

The signal envelope timing is set by the capacitors Ctenv and Crenv. Because of the logarithmic compression between TSEN and TENV respectively RSEN and RENV, the timing can be expressed in dB/ms. At roomtemperature the following relation counts:

Timing ≈ I / (3 * C) (in dB/ms).
With I = charge or discharge current from pin TENV, RENV, TNOI or RNOI (in A)
C = timing capacitor Ctenv, Crenv, Ctnoi or Crnoi (in F).

With the advisory signal envelope timing capacitors Ctenv and Crenv of 470nF, the maximum attack-timing of the signal envelopes will be around 85dB/ms (I=120μA). This is enough to track normal speech. The release-timing will be 0.7dB/ms (I=1μA). This is enough to smoothen the signal envelope and to eliminate the influence of room-echoes on the switching behaviour.

With the advisory noise envelope timing capacitors Ctnoi and Crnoi of 4.7μF, the attack-timing of the noise envelopes will be 0.07dB/ms (I=1μA). This is small enough to track background noise and not to be influenced by speech bursts. The maximum release-timing will be 8.5dB/ms (I=120μA). This is enough to track the signal envelope during release because the signal envelope release timing is 0.7dB/ms which is a factor smaller.
It is advised to choose the signal envelope timing and the noise envelope timing of both channels equal for optimum operation of the duplex controller. To have clearly determined timings, it is advised not to use capacitors with a high leakage current.

The switch-over timing is determined by the value of the switch-over capacitor Cswt. The idling timing is determined by the combination of Cswt and the idling resistor Ridt.
If the output current of pin SWT is Iswt, a voltage difference over Cswt can be obtained according:

$\delta Vswt/t = Iswt / Cswt$ (mV/ms).

With the advised value for Cswt of 220nF, the obtained voltage difference is 45mV/ms. The switch-over time is dependent on the voltage difference which has to be generated on SWT. Suppose the set is in full Tx-mode, then the voltage on SWT will be V(IDT)-400mV, see figure 3.4.4. To reach Rx-mode a voltage difference of 580mV must be generated to end up at a voltage of V(IDT)+180mV. So in this case the switch over time will be 13ms. When the set is in Ix-mode the voltage on SWT equals the voltage on IDT. In that case Rx-mode or Tx-mode will be reached within 4ms.
The idling timing is determined by an RC-time constant. It is supposed that Ix-mode is reached when a time (Tidt) is passed of:

Tidt = 4 * Ridt *Cswt.

With the advised value for Ridt of 2.2MΩ, an idling time of around 2 seconds is obtained. To have a clearly determined idling timing, it is advised not to use a capacitor with a high leakage current.

Miscellaneous

When a handsfree telephone set is used at one end of the subscriber line and a conventional set at the other end, the user of the conventional set will think that the line is 'dead' when the handsfree set stays in receive mode while no signal on the line is present. This is avoided when the handsfree set switches over to a so called idle mode. This mode is incorporated in the TEA1094 and is placed exactly in between the transmit and receive mode. When it is desired to have an idle mode which is closer to transmit than receive mode, the circuit of figure 3.4.5 can be applied.

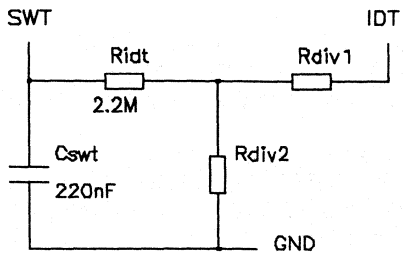


Figure 3.4.5: Circuitry for shifting the idle mode

With the circuit of figure 3.4.5, in idle mode, the voltage on SWT will not go to the voltage on IDT but to the voltage on IDT minus the voltage drop over Rdiv1. The voltage drop over Rdiv1 determines the shift of the idle mode (in dB's). This shift can be read from figure 3.4.4, when the voltage drop over Rdiv1 is taken as the x-axis value. The voltage on IDT is approximately 1.2V, so with for instance Rdiv1=33kΩ and Rdiv2=1MΩ the shift will be approximately 10dB. When dimensioning the resistor divider, it is advised not to choose Rdiv2 smaller than 1MΩ in order to limit the current drawn from IDT. By connecting Rdiv2 to VBB instead of to GND, the idle mode is shifted towards the receive mode.

In noisy environments, like offices, a handsfree set can show a popping behaviour in idle-mode (unwanted switching over from Ix to Tx-mode). This can be caused for instance by footsteps in the corridor. In the TEA1094, this popping behaviour is reduced by the implemented speech/noise threshold of 4.3dB. However, when a larger threshold is desired this can be achieved by connecting a resistor Rtnoi in series with Ctnoi.
When there is only noise present at the input of the envelope detector, the voltages on pins TENV and TNOI are equal. When, suddenly, a signal is present, the voltage on TENV will increase. Without Rtnoi, the voltage on TNOI will increase slowly because of the charging of Ctnoi by the 1μA internal current source. When a resistor Rtnoi is placed in series with Ctnoi, under the same conditions, this 1μA current source will cause a voltage jump on TNOI. This jump determines the shift of the speech/noise threshold.
As depicted in figure 3.4.1, at roomtemperature, the 4.3dB threshold equals 13mV. A resistor Rtnoi in series with Ctnoi will add an extra voltage to this threshold of 1μA*Rtnoi. When for instance a resistor of 10kΩ is chosen, the speech/noise level is increased up to 23mV which is equal to 7.6dB at roomtemperature. The new speech/noise threshold is slightly dependent on temperature and the spread of the internal current source and therefore not as accurate as the internal 4.3dB. It is advised not to use a resistor larger than 15kΩ.

Chapter 4. Application cookbook

In this chapter the procedure for making a basic application with a speech-transmission circuit of the TEA106x-family and the handsfree circuit TEA1094 will be given. With the aid of figure D.1 in appendix D, the design flow is given as a number of steps which should be made. As far as possible for every step also the components involved and their influence on every step are given. The preferred value is given between brackets { }. More information on the setting of the TEA1094 can be found in the chapters given at every step. More information on the setting of the TEA106x-family see data handbook [Ref.1] and appendix B.

The application of figure D.1 is an application of the TEA1094 handsfree circuit together with the TEA106x speech-transmission circuit. Switches are incorporated to switch over between handsfree operation and handset operation. A microcontroller and an interruptor are not incorporated.
As can be seen in figure D.1, only a few components have a fixed value. These are the zener diode of 12Volts protecting the TEA106x and the resistors R5 and Rstab setting reference currents for the TEA106x and TEA1094 respectively. All other values will follow from the cookbook of figure 4.1.

Worked out examples of applications of the TEA1094, following the cookbook are discussed in chapter 5.

STEP	ADJUSTMENT
DC-settings: Adjust the DC setting of the TEA106x to the local PTT requirements.	
Voltage LN-SLPE DC-slope Supply point VCC Artificial inductor	R17 R9 {20Ω}, R10 (also current protection) C1 {100µF} C3 {4.7µF}
Impedance and sidetone: After setting the set impedance, the sidetone has to be optimized for mean linelength and linetype. Also AGC can be chosen.	
Set impedance Sidetone AGC	Z1; R10 is in series R2, R3, R8, R11, R12, C12 R6
TEA106x Microphone and earpiece amplifiers, see appendix B: After the sensitivity of the microphone is adjusted, the gain can be adjusted to the desired value. Also the frequency curve can be set. The same counts for the earpiece.	
Sensitivity microphone Microphone gain Frequency curve and stability Earpiece gain Frequency curve and stability	R20,R21; microphone dependent R7; depends on TEA106x used C6; low pass with R7+3.5kΩ C20; stability for C20=10*C6 C8, C9, R14; high pass with input impedance R4; depends on TEA106x used C4; low pass with R4 C7; stability for C7=10*C4 C5; highpass with input impedance IR C2; highpass with earpiece impedance
TEA1094 Microphone amplifier, see chapter 3.2: After the sensitivity of the microphone is adjusted, the gain can be adjusted to the desired value. Also the frequency curve can be set.	
Sensitivity microphone Transmit gain Frequency curve and stability	Rmic Rgat; Atx=20log(0.674*Rgat/Rstab) (dB) Cgat; low pass with Rgat, also stability Crmic; low pass with Rmic Cmic; high pass with input impedance (20kΩ)

STEP	ADJUSTMENT
TEA1094 Loudspeaker amplifier, see chapter 3.3: The loudspeakergain can be adjusted to the desired value. Also the frequency curve can be set. The volume control potentiometer can be chosen as well as the dynamic limiter timing to have a minimal distortion.	
Receive gain Frequency curve and stability Volume control Dynamic limiter timing	Rgar; Arx=20log(0.435*Rgar/Rstab) (dB) Cgar; low pass with Rgar Crin1; high pass with input impedance (20kΩ) Crin2 {Crin1} Clsp; high pass with loudspeaker impedance Rvol {10kΩ}; 3dB reduction for each 950Ω Cdlc {470nF}
TEA1094 Duplex controller, see chapter 3.4 and appendix A: When all gains are adjusted the switching range can be determined by measuring the loopgain. Then the dialtone detector level can be set as well as the sensitivies of the duplex controller. Finally the timings of the envelopes and the switching are adjusted.	
Switching range Dial tone Sensitivity Signal Envelope Noise envelope Switch-over timing Idle mode timing	Loopgain: Aloop=Atx1094+Atx106x+Ast+ Arx106x+Arx1094+Aac-Asw<0 (dB) Choose Asw with safety margin of 10-20 (dB) Adjust Rswr; Asw=20log(Rswr/Rstab) (dB), with Rstab is fixed to 3.65kΩ Rrsen; Vdialtone=12.7μA*Rrsen (Vrms) Rtsen; For equal sensitivities of Tx and Rx: 20log(Rtsen)=20log(Rrsen)-Atx1094-Atx106x-Ast -ArxTEA106x+40+½Aloop (dB) Ctsen; high pass with Rtsen Crsen; high pass with Rrsen Ctenv {470nF}, Crenv {470nF}; Maximum attack: 120μ/(3*Cenv) (dB/ms) Release: 1μ/(3*Cenv) (dB/ms) Ctnoi {4.7μF}, Crnoi {4.7μF}; Attack: 1μ/(3*Cnoi) (dB/ms) Maximum Release: 120μ/(3*Cnoi) (dB/ms) Cswt {220nF}; ‖ΔVswt‖/t=10μ/Cswt (mV/ms) Ridt {2.2MΩ}; timeconstant: 4*Ridt*Cswt

Figure 4.1: Steps in the design flow of the TEA106x+TEA1094

Chapter 5. Application examples

In this chapter some application examples of the TEA1094 handsfree circuit are given. In all examples only the essential elements are given. For instance no ringer or interruptor is included. The setting of the examples is made by following the cookbook of chapter 4. The lower corner frequencies are chosen between 200Hz and 300Hz and the higher corner frequencies around 4kHz. Components which are not mentioned have the advised value. In appendix B the gains and DC-settings of the TEA106x family can be found.

Figure D.2 gives the basic handsfree application of the TEA1094 together with a speech transmission circuit of the TEA106x family. This basic application only incorporates handsfree telephony.

DC-settings: R17 is chosen 39.2kΩ which makes 4.5V to 5.0V after the bridge at 15mA of line current, depending on the TEA106x used, see appendix B. Resistor R10 is 12Ω for current protection.

Impedance and sidetone: The set impedance is made approximately 600Ω for the telephony band with R1 and R10. The optimized sidetone bridge for this impedance in combination with a 5km cable of 0.5mm diameter copper twisted pair (176Ω, 38nF per km) is taken from [Ref.1]. Also AGC is set with R6=110kΩ. This gives optimum result for an exchange of 48V and 600Ω in combination with the 0.5mm diameter cable (1.2dB attenuation per km).

TEA106x amplifiers: The microphone gain is set to the lowest value with R7=27.4kΩ (44dB for TEA1060/2/4/7/8). The receive gain is set to its maximum value of -1dB with R4=100kΩ (-32dB attenuation by the anti sidetone-bridge and 31dB gain from IR to QR+ for TEA1062/4/7).

TEA1094 amplifiers: The transmit gain is set to 5dB with Rgat=9.53kΩ. The receive gain is set to 25dB with Rgar=150kΩ. This results in an overall receive gain from line to loudspeaker output LSP of 24dB.

TEA1094 duplex controller: By measuring the loopgain following appendix A, the switching range can be determined. The loopgain is, of course, very dependent on the acoustic coupling between loudspeaker and microphone. With the set used for the measurements in appendix A, a switching range of 40dB (Rswr=365kΩ) leads to a gainmargin of 18dB. The dialtone detector level was chosen 89mVrms on the inputs RIN1 and RIN2 (meaning 100mVrms on the line). This results in Rrsen=6.81kΩ.
When using the sensitivity measurement result of appendix A, 20log(vtsen/vrsen)=4dB, the resistor Rtsen follows out of 20log(Rtsen/Rrsen)= 4dB-(18dB/2)=-5dB or Rtsen=3.92kΩ.

Figure D.3 gives the handsfree/handset application of the TEA1094. This application incorporates both handsfree and handset operation. As an example the receive gain of the TEA106x is made 4dB lower with respect to figure D.2. The receive gain of the TEA1094 is raised with 4dB to have the same overall receive gain. To detect a dial tone of 100mVrms at the line, due to the lowered receive gain of the TEA106x, the resistor Rrsen is changed into 4.75kΩ. As can be seen in the formulas of chapter 3.4.4, Rtsen does not need to be changed.
The switches can be either mechanical or electronic ones.

Figure D.4 gives the handsfree/handset/listening-in application. In listening-in operation an acoustical loop is formed by the loudspeaker and the handset microphone. Without measures this loop can cause howling when the handset is close to the loudspeaker. This situation is quite similar to the handsfree howling problem, see figure 1.1. Therefore, the TEA1094 can also be used to prevent howling in listening-in operation. This is done by connecting the handset microphone to the TEA1094 instead of connecting it directly to the TEA106x. The switching is now introduced in the listening-in loop. This switching has no effect on the earpiece level. Switch-over between the different modes is possible by the external switches.
The setting of the application is quite similar to the previous application examples. The receive channel is not changed. In the transmit channel an attenuator of 20dB is placed between the TEA1094 and the TEA106x. This is done to reduce the sending noise on the line in receive mode, see chapter 3.2.1. To end up with the same overall transmit gain as in the previous examples, the transmit gain of the TEA1094 itself is raised with 20dB. To have a correct transmit gain during handset mode, the sensitivity of the handset microphone has been adjusted (R20, R21). In practice there will be no need for changing the switching range for listening-in operation with respect to handsfree operation.

Figure D.5 gives a blockdiagram of a cordless telephone with handsfree base-unit. The line-interface is supplied by the telephoneline, while the handsfree and cordless part are mains supplied. The galvanic seperation between the two parts is done with opto-couplers but it can also be done with transformers. The signals which are coupled are the transmit (Tx) and receive (Rx) signals, the dial-pulse signal (DP), the ring detect signal (Rdet) and the on/off-hook information (Hook). The ground of the line-interface part is VEE, while GND is the ground of the rest of the base.
In a cordless telephone with handsfree-base, it must be possible to transmit the signals of the handset to both the line and the base (intercom). Also, it must be possible to have a handsfree conversation with the far-end user. To make this possible, a switch-block is depicted. The mode of the set (thus the mode of the switches, the TEA1094 and the handset) is defined by the microcontroller (uC). To save opto-couplers, DTMF dialling is done via the MIC+/- inputs of the TEA106x.

Figure D.6 gives a blockdiagram of a telephoneset with answering machine. The line-interface and the handset are supplied by the telephoneline, while the handsfree and answering machine part are mains supplied. The galvanic seperation between the two parts is done with opto-couplers but it can also be done with transformers. The signals which are coupled are the transmit (Tx) and receive (Rx) signals, the dial-pulse signal (DP), the ring detect signal (Rdet) and the on/off-hook information (Hook). Also a signal defining handset or handsfree/answering mode is coupled (MODE) which sets the block with switches. The ground of the line-interface part is VEE, while GND is the ground of the rest of the set.
In a telephone with answering machine, it must be possible to transmit an outgoing message to both the line and the loudspeaker. Also, it must be possible to record incoming messages as well as to have a handsfree conversation with the far-end user. To make this possible, a switch-block is depicted. The mode of the set (thus the mode of the switches, the TEA1094 and the handset) is defined by the microcontroller (uC). To save opto-couplers, DTMF dialling is done via the MIC+/- inputs of the TEA106x.

Chapter 6. Electromagnetic compatibility

With respect to electromagnetic compatibility (EMC) no common European or international specification yet exists. Also the measurement methods differ and are not always reproducible. At the application laboratory in Eindhoven (PCALE) the German current injection method is used (VDE 0878 part 200). It is a reliable method of measuring and is highly reproducible. The method is described in [Ref.3]. The hints for EMC of the TEA106x-TEA1094 combination given in the second paragraph of this chapter are based on this method. The same counts for the hints of the printed circuit board design given in the first paragraph.

6.1. Printed circuit board

In the current injection method, radio frequency (RF) signal currents enter the telephone set at the a/b wires and leave the set via any capacitive coupling to ground. Normally, in a telephone set the handset has the largest capacitance to ground and thus the main part of the RF signal current flows to ground via the handset. However, in handsfree operation the handset is not used. The RF signal current then flows to ground via the groundplane of the printed circuit board (PCB) and partly via the wires of the loudspeaker and microphone. Therefore, a proper PCB layout is essential for good EMC.

The first measure to be taken is to create a groundplane on the PCB. The RF signals entering the PCB should be decoupled immediately to this groundplane. Preferably this groundplane is homogeneous and is not cut into parts by interconnection wires. To reach this a double layered PCB, with interconnection wires on one side of the board and a groundplane on the other side, is a minimum. When interconnection wires within the groundplane are inevitable, the continuity of the groundplane should be restored. This is done by cross coupling these interconnection wires by jumpers and wires at the interconnect side of the PCB. In this way RF signal currents can flow freely over the groundplane.

Another measure is to keep the length of the wires between the different components as short as possible. Of course this measure is especially important for those wires which interconnect one or more RF signal sensitive parts, in particular the wire connected to SLPE which is also the reference for the TEA1094. As any current, RF signal currents prefer to flow to ground via the lowest ohmic path. Therefore, it should be noted that a wire of 10mm corresponds to an inductor of 10nH.
The wires to the handsfree microphone and the loudspeaker should be kept as short as possible as well. Normally, this is not a problem since loudspeaker, microphone and PCB are all within the same cabinet.

6.2. TEA106x-TEA1094 combination

All measures in this paragraph are based upon EMC experience and measurements at the TEA106x-TEA1094 application of figure D.7. This figure only gives the essential EMC components and it is just an example for a solution for better EMC performance since other applications and or different PCB layouts will demonstrate different behaviour. This paragraph should therefore be interpreted as a guidance to reach proper EMC design.

This paragraph is split into two parts. In the first part the standard measures for the

TEA106x are given. In the second part it is explained how to improve the EMC behaviour of the TEA1094. When, after the proposed measures are taken, the EMC behaviour has to be optimized, it is advised to start with the transmit direction of the telephoneset and to optimize the receive part thereafter. This because, due to sidetone, signals demodulated by the transmit channel will be seen in the receiver channel.
In the text below it is supposed that the printed circuit board on which the TEA106x-TEA1094 is built, is provided with a groundplane which is connected to VEE. It is preferred to place the components meant for EMC as close as possible to the pins, except when otherwise stated.
For more details on the EMC performance of the TEA106x, see [Ref.3].

TEA106x

RF signals entering the printed circuit board at the a/b wires should be decoupled to the groundplane via capacitors, preferably placed as close as possible to the a/b connection. Since these capacitors will be in parallel with the set impedance, their value is limited. In practice, a total capacitance of 10nF between the a/b wires may be applied without degrading the balance return loss.
Between the a/b wires and the groundplane two capacitors of 4.7nF each are placed. Another capacitor of 2.2nF is placed between pin SUP of the TEA1094 and the groundplane. Also a coil of 22μH is placed in series with the line.

RF signals entering the inputs of the transmit channel (MIC+, MIC-) will be demodulated and amplified to the line. Because of the high gain (in the order of 50dB) the transmit channel is very sensitive to RF signals. Therefore, decoupling at the inputs is essential. The inputs MIC+ and MIC- can best be decoupled by 2 capacitors of 10nF connected to the groundplane. Also series resistors can be applied which in combination with the capacitors form low pass filters towards the inputs. Resistors of 1kΩ are advised which reduce the gain setting with less than half a dB, depending on the input impedance of pins MIC+ and MIC-. This can be compensated by adapting the transmit gain adjustment resistor R7 of the TEA106x.
In case a handset microphone is connected to the TEA106x microphone inputs via a long cord, extra decoupling is needed. This can be done by adding two capacitors of 10nF each, placed between the cord connection and the groundplane, preferably as close as possible to the cord connection.

RF signals entering the inputs of the receive channel (IR) will be demodulated and amplified to the earpiece and, via the TEA1094, to the loudspeaker. Therefore, decoupling at the input is essential.
At the input IR of the TEA106x a capacitor of 2.2nF connected to the groundplane is advised.
In case an earpiece is connected to the TEA106x via a long cord, extra decoupling is needed. This can be done by adding two capacitors of 10nF each, placed between the cord connection and the groundplane, preferably as close as possible to the cord connection. To prevent the remaining RF signals from entering the earpiece outputstage of the TEA106x via the QR pin, and thus the loudspeaker amplifier inputs of the TEA1094, a series resistor should be applied to create a high ohmic path. The value of this resistor is dependent on the type of earpiece capsule used. When a dynamic capsule of 150Ω is used, a resistors of 22Ω is advised. This will reduce the gain setting with 1.19dB. This can be compensated by adapting the receive gain adjustment resistor R4 of the TEA106x.

Besides these essential measures some additional measures can be taken. A capacitor between GAS2 and the groundplane of 100pF can improve EMC in the transmit direction. A series combination of a resistor of 365Ω and a capacitor of 4.7nF connected between STAB and the groundplane can improve EMC for both transmit and receive direction.

TEA1094

The reference for the TEA1094 is GND, connected to VEE. When GND is connected to SLPE, this reference has to be decoupled to obtain a good EMC behaviour. This can be achieved by using a coil-capacitor combination between SLPE, GND and VEE. It is advised to use a coil of a value between 5μH and 33μH and a parasitic series resistance smaller than 5Ω. The capacitor has an advised value of 4.7nF.
The reference current source of the TEA1094 must have a high immunity because it sets the transmit and receive gains. Therefore, pin STAB must be decoupled. This can be done with a series combination of a resistor of 365Ω and a capacitor of 4.7nF connected between STAB and GND.

RF signals entering the input of the transmit channel (MIC) will be demodulated and amplified to the line. Because of the high gain (in the order of 50dB) the transmit channel is very sensitive to RF signals. Therefore, decoupling at the input is essential.
At the input MIC a capacitor of 4.7nF connected to GND, is advised. Also a series resistor can be applied which, in combination with the capacitor, will form a low pass filter towards the MIC input. A resistor of 1kΩ is advised which reduces the gain setting with 0.42dB. This can be compensated by adapting the resistor Rgat.
In case a handset microphone is connected to the TEA1094 microphone inputs, for instance with the application of figure D.4, extra decoupling is needed. This can be done in the same way as in case the handset is connected to the TEA106x (thus extra decoupling to the groundplane).

RF signals entering the volume control pin VOL will modulate the receive gain. Therefore, the pin VOL has to be decoupled. This can be done by connecting a capacitor of 4.7nF between VOL and GND.

Besides these essential measures some additional measures can be taken. When the stabilized supply is not connected very close to pin VBB, a small capacitor of 4.7nF connected close to pin VBB will improve EMC behaviour.
To improve the EMC behaviour in the receive channel, the inputs RIN1 and RIN2 can be decoupled. This can be done by connecting 2 capacitors of 10nF each between the inputs and the groundplane. Also series resistors can be applied which in combination with the capacitors form low pass filters towards the inputs. Resistors of 1kΩ are advised which reduce the gain setting with 0.42dB. This can be compensated by adapting the resistor Rgar of the TEA1094.
To improve EMC behaviour in the transmit channel, pin GAT can be decoupled to GND via a capacitor with the same value as capacitor Cgat. The influence of this capacitor on the transmission parameters can be neglected.

Chapter 7. References

[Ref.1] Philips Semiconductors Data Handbook
Semiconductors for telecom systems - IC03
Philips Semiconductors, 1993

[Ref.2] TEA1093 Handsfree IC
Final device specification
May 1993, version 3.0

[Ref.3] Measures to meet EMC requirements for TEA1060-family speech transmission circuits
M. Coenen, K. Wortel
PCALE reportnumber: ETT89016

[Ref.4] TEA1094 Handsfree IC
Tentative device specification
February 1994, version 2.1

[Ref.5] Application of the TEA1093 handsfree circuit
C.H. Voorwinden, K. Wortel
PCALE reportnumber: ETT/AN93015

Extended application information on the speech transmission circuits can be found in:

1. TEA1060 family versatile speech/transmission ICs for electronic telephone sets
Designers' guide by P.J.M. Sijbers
July 1987, 12NC 939834110011

2. Application of the versatile speech/transmission circuit TEA1064 in full electronic telephone sets by F. van Dongen and P.J.M. Sijbers
PCALE reportnumber: ETT89009

3. Application of the speech-transmission circuit TEA1062
P.T.J. Biermans
PCALE reportnumber: ETT89008

More information on the Philips cordless telephony products can be found in:

4. CT1 Evaluation board OM4735
J. Soree
PCALE reportnumber: ETT/AN93014

Appendix A. Measurement setup

This appendix describes how both the loopgain and the sensitivity setting can be measured. These measurements give a starting point for obtaining the final values which however, only can be reached by performing subjective tests.

For determining the loopgain the worst-case acoustical coupling and sidetone must be measured. This can be done with the measurement setup of figure A.1.

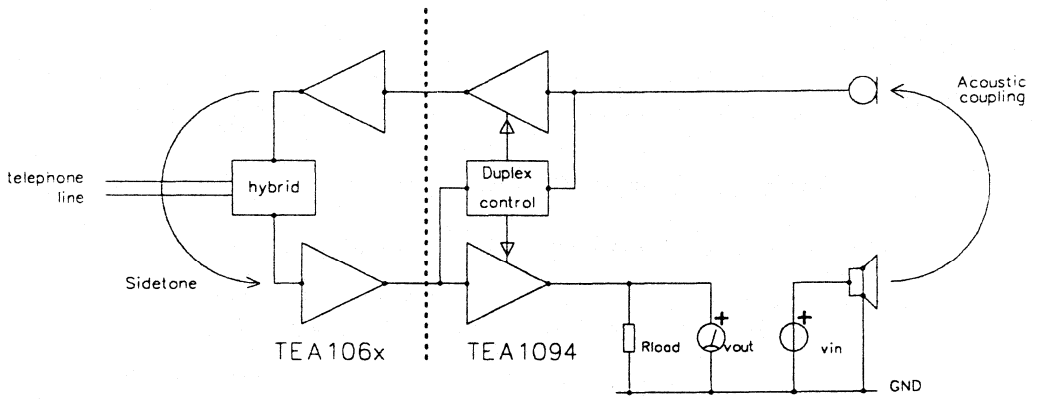


Figure A.1: Simplified measurement setup for measuring the loopgain

The loudspeaker is disconnected from the set and an electrical signal is applied to it. The acoustical signal coming from the loudspeaker is coupled to the microphone (Aac), transmitted to the line (Atx1094 + Atx106x), returns via sidetone (Ast) and is amplified again to the loudspeaker output of the TEA1094 (Arx106x + Arx1094). The output is loaded with a loudspeaker equivalent (Rload). The total gain of this loop is reduced with the switching range (Asw).
The gain from the loudspeaker connection (vin) to the loudspeaker equivalent (vout) is the loopgain (Aloop), given as:

$$20 * \log (vout/vin) = Aloop,$$
$$Aloop = Aac + Atx1094 + Atx106x + Ast + Arx106x + Arx1094 - Asw.$$

When this measurement is done with a vin of 100mVrms and between 100Hz and 10kHz, this will result in a curve such as displayed in figure A.2.

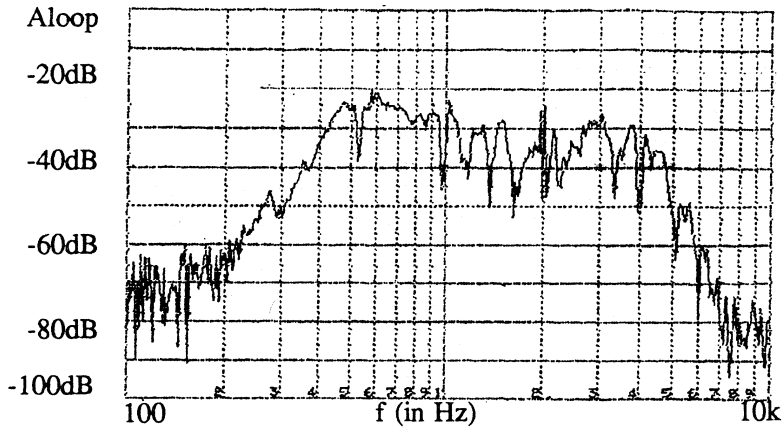


Figure A.2: Example of loopgain versus frequency

The highest value of the loopgain gives an indication of the gain margin.

The measurement of the loopgain Aloop has to be done with fixed transmit and receive gains, a fixed switching range and worst case acoustic coupling and sidetone.
The transmit and receive gains of the TEA106x and TEA1094 are supposed to be set, the switching range however, can only be set after the measurement. Therefore, during measurement the switching range Asw must be set to a certain value. An advised value for measurements is 40dB. This means that the resistor Rswr must be set to 365kΩ. The mode of the TEA1094 is not of influence on the measurement.
The worst case acoustical coupling can be found by moving around the set. A fairly good way of determining it, is keeping a hand close to the set as if pushing a button.
The worst case sidetone can be found by measuring the loopgain for several linelengths, for instance every kilometer, while maintaining the worst case acoustical coupling.
When AGC is used, the loopgain for short lines, smaller than 5km, will be lower than without AGC. As an effect, the switching range for a set with AGC can be made smaller than for a set without AGC.
The measurement combining both worst case sidetone and acoustical coupling gives the worstcase loopgain and thus the gain margin. The switching range now can be adapted to fit the gain margin desired.

When the correct switching range is set, the sensitivity setting can be determined.
For determining the sensitivity, calculations can be done as described in chapter 3.4.4. It is also possible measuring the correct sensitivity setting. This can be done with the measurement setup of figure A.3.

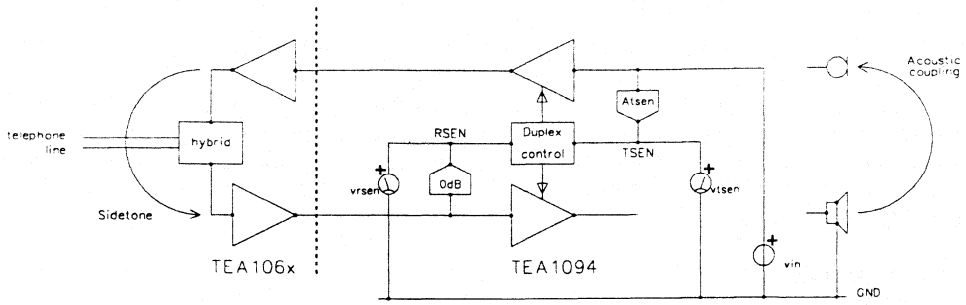


Figure A.3: Simplified measurement setup for determining sensitivity

Both the loudspeaker and microphone are disconnected from the set. An input signal (vin) is applied to the microphone input. This signal is amplified to pin TSEN (Atsen). It is also transmitted to the line, returns via the sidetone, amplified by the TEA106x to the TEA1094 receive inputs and buffered to pin RSEN. The ratio of the signals on pin TSEN (vtsen) and RSEN (vrsen) is given as:

$$20 * \log (vtsen/vrsen) = Atsen - Atx1094 - Atx106x - Ast - Arx106x.$$

When this measurement is done with a vin of 1mVrms and between 100Hz and 10kHz, this will result in a curve such as displayed in figure A.4.

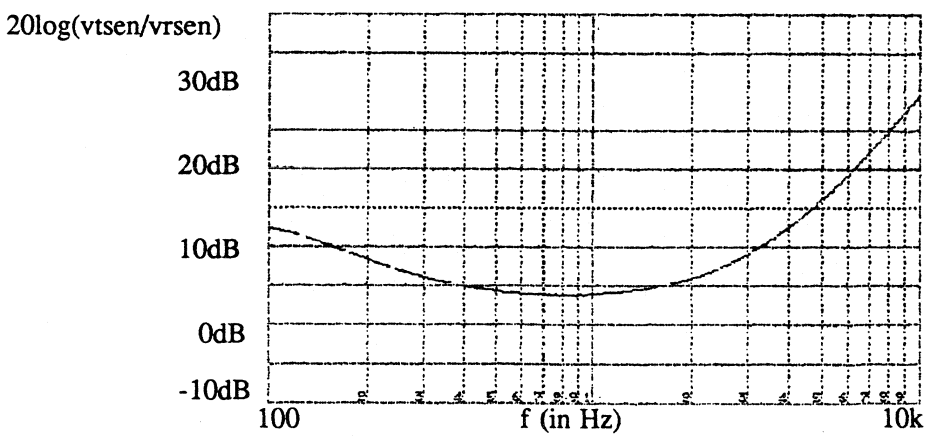


Figure A.4: Example of 20log(vtsen/vrsen) versus frequency

This is a smooth curve because the acoustical coupling is not in it. During this measurement the set must be in Tx mode. This can be done by making DLC/$\overline{MUTER}$ lower than 200mV. This will mute the receiver, and puts the set into Tx mode, but will not effect the signal on RSEN.

Out of the measured ratio of vtsen and vrsen it follows, see also chapter 3.4.4, Ad 3:

$$20 * \log (Rtsen/Rrsen) = 20 * \log (vtsen/vrsen) + Aloop/2.$$

This means that the optimal Rtsen is dependent on frequency because both the ratio of vtsen and vrsen as well as Aloop are frequency dependent. However, this can be simplified by using the lowest value of 20*log(vtsen/vrsen) and the highest value of Aloop to obtain the correct Rtsen. This will lead to the same answer as will be obtained by performing the calculations of chapter 3.4.4, Ad 3.

The value for Rtsen found, is a starting point for obtaining the final value which only can be reached by subjective tests with a real telephone line.

Appendix B. TEA106x quick reference data

	DC-CHARACTERISTICS (with slope resistance R9=20Ω)		
Member	V(LN-VEE) (in V) at Iline=15mA	V(LN-VEE) (in V) at R(REG-LN)=68kΩ	V(LN-VEE) (in V) at R(REG-SLPE) (in Ω)
TEA1060	4.45 ± 0.20	3.80 + 0.25/-0.30	5.0 ± 0.30 at 39k
TEA1062	4.00 + 0.25/-0.45	3.50 ±	4.5 ± .... at 39k
TEA1064B	3.50 ± 0.25	---	4.4 ± 0.35 at 20k
TEA1067	3.90 ± 0.25	3.40 ± 0.30	4.5 ± 0.30 at 39k
TEA1068	4.45 ± 0.25	3.80 ± 0.30	5.0 ± 0.35 at 39k

	SENDING GAIN		RECEIVE GAIN (from IR to QR+)	
Member	Setting range (in dB)	Gain (in dB) with R7=68kΩ	Setting range (in dB)	Gain (in dB) with R4=100kΩ
TEA1060	44 - 60	52 ± 1	17 - 33	25 ± 1
TEA1062	44 - 52	52 ± 1.5	20 - 31	31 ± 1.5
TEA1064B	44 - 52	52 ± 1	20 - 39	31 ± 1
TEA1067	44 - 52	52 ± 1	20 - 39	31 ± 1
TEA1068	44 - 60	52 ± 1	17 - 33	25 ± 1

	SENDING NOISE	
Member	Noise (in dBmp) with R7=68kΩ	Noise (in dBmp) with sending gain of 44dB
TEA1060	-70	-78
TEA1062	-69	-77
TEA1064B	-72	-80
TEA1067	-72	-80
TEA1068	-72	-80

For more data see datahandbook [Ref.1].

Appendix C. List of abbreviations and definitions

Aac	Electro-acoustic coupling (electrically measured)
AGC	Automatic line loss compensation of the TEA106x
Aloop	Loopgain of a handsfree telephone set (must be < 0dB)
Arx	Receive gain of the TEA1094 (3dB to 39dB)
ArxTEA106x	Receive gain of the TEA106x
ArxTEA1094	Receive gain of the TEA1094 (3dB to 39dB)
Ast	Electrical sidetone
Asw	Switching range (0dB to 52dB)
Atsen	Gain from MIC to TSEN of 40dB
Atx	Gain of the transmit channel of the TEA1094 (5dB to 25dB)
AtxTEA106x	Gain of the transmit channel of the TEA106x
AtxTEA1094	Gain of the transmit channel of the TEA1094 (5dB to 25dB)
BTL	Bridge tied load (loudspeaker between LSP1 and LSP2)
Cdlc	Dynamic limiter timing capacitor (470nF advised)
Cgat	Capacitor over Rgat
Clsp	DC blocking capacitor for loudspeaker
Cmic	Coupling capacitor at microphone input
Crenv	Capacitor determining the receive signal envelope (470nF advised)
Crin1,Crin2	Couple capacitors at receiver input
Crmic	Capacitor over Rmic
Crnoi	Capacitor determining the receive noise envelope (4.7µF advised)
Crsen	DC-blocking capacitor of receive sensitivity setting
Cswt	Switchover timing capacitor (220nF advised)
Ctenv	Capacitor determining the transmit signal envelope (470nF advised)
Ctnoi	Capacitor determining the transmit noise envelope (4.7µF advised)
Ctsen	DC-blocking capacitor of transmit sensitivity setting
dBmp	0 dBmp equals 1 milliWatt in 600Ω, psophometrically weighted
DLC/*MUTER*	Dynamic limiter timing adjustment and receiver channel mute pin
DP	Dial pulse, output pin on microcontroller
δVswt	Voltage difference on SWT
EMC	Electro Magnetic Compatibility: the collective noun for the susceptibility and the radiation of a circuit/apparatus.
GAR	Receiver gain adjustment pin
GAT	Microphone gain adjustment pin
GND	Ground reference pin
GNDMIC	Ground reference pin for microphone amplifier
HCT4053	Philips IC containing 3, 2-channel analogue switches
HCT4066	Philips IC containing 4 analogue switches
IDT	Idle-mode timing adjustment pin
IR	Receive input pin of the TEA106x
Iswt	Current through pin SWT (typical 10µA)
Ix-mode	Idle-mode: the mode which is halfway Tx-mode and Rx-mode.
LN	Positive line terminal pin of the TEA106x
LSP	Loudspeaker amplifier output pin
MIC	Microphone input pin
MIC+, MIC-	Microphone inputs pins on the TEA106x
MOSFET	Metal oxide field effect transistor
MOUT	Microphone amplifier output pin

MUTET	Transmit channel mute input pin
PCALE	Product concept & application laboratory Eindhoven
PCB	Printed circuit board
Power Down	Reduced current consumption mode during pulse dialling or flash
PTAT	Proportional to absolute temperature
PTT	Telephone company
QR,QR+	Telephone earpiece output on TEA106x
RIN1,RIN2	Receiver amplifier input pins
RENV	Receive signal envelope timing adjustment pin
Rgar	Resistor setting receive (loudspeaker) gain (66.5kΩ for 18dB SEL)
Rgat	Resistor setting transmit (microphone) gain (30.1kΩ for 15dB)
Ridt	Resistor setting idle mode timing (2.2MΩ advised)
RF	Radio frequencies
Rload	Loudspeaker equivalent load resistor used for measurements
Rmic	Resistor setting the microphone sensitivity
RNOI	Receive noise envelope timing adjustment pin
Rrsen	Resistor setting sensitivity of the receive envelopes
RSEN	Receive signal envelope sensitivity adjustment pin
Rstab	Resistor setting an internally used PTAT current (3.65kΩ)
Rswr	Resistor determining switching range
Rtnoi	Resistor for increasing speech/noise threshold
Rtsen	Resistor setting sensitivity of transmit envelopes
Rvol	Volume control potentiometer (10kΩ advised)
Rx-mode	Receive-mode: the gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is reduced
SLPE	DC slope pin on TEA106x
STAB	Reference current adjustment pin
Switching range	The difference between the maximum and the minimum gain in a channel as a result of the switching of the duplex controller (Asw)
SWR	Switching range adjustment pin
SWT	Switch-over timing adjustment pin
TEA106x	IC of the TEA106x speech transmission family: TEA1060/61, TEA1062, TEA1063, TEA1064, TEA1065, TEA1066, TEA1067, TEA1068.
TENV	Transmit signal envelope timing adjustment pin
THD	Total harmonic distortion
Tidt	Idle mode timing
TNOI	Transmit noise envelope timing adjustment pin
TSEN	Transmit signal envelope sensitivity adjustment pin
Tx-mode	Transmit-mode: the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is reduced
VBB	Supply output pin
VCC	Supply pin of the TEA106x
Vdialtone,Vdt	Dialtone detector level at the inputs RIN1 and RIN2
VEE	Reference pin on TEA106x
VOL	Receiver volume adjustment pin

Appendix D. Figures

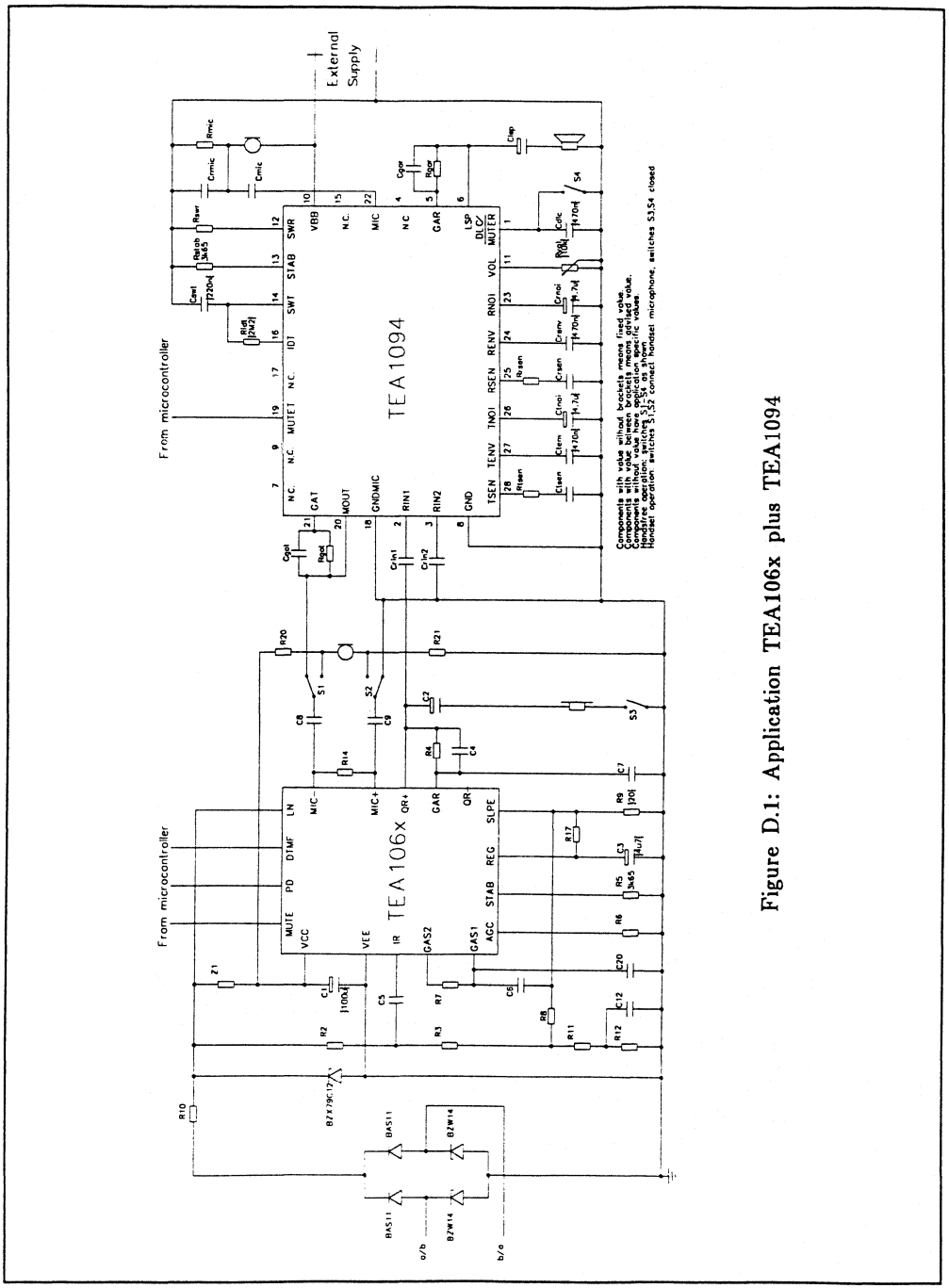


Figure D.1: Application TEA106x plus TEA1094

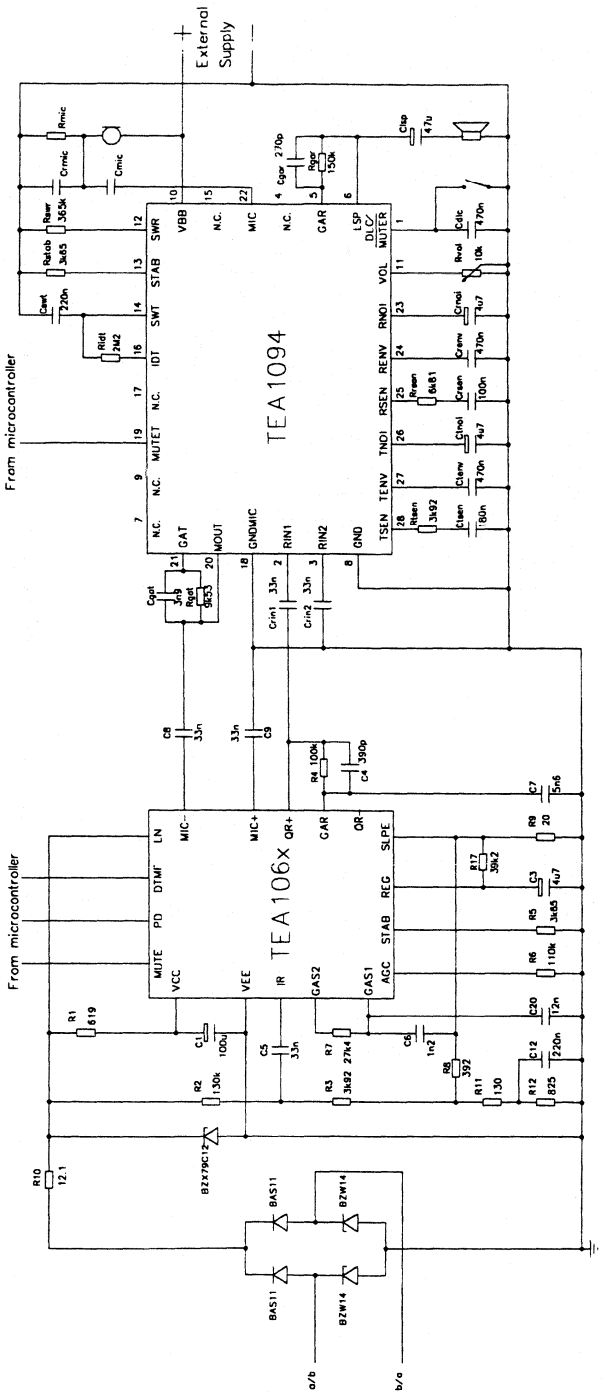


Figure D.2: Basic handsfree application of the TEA1094

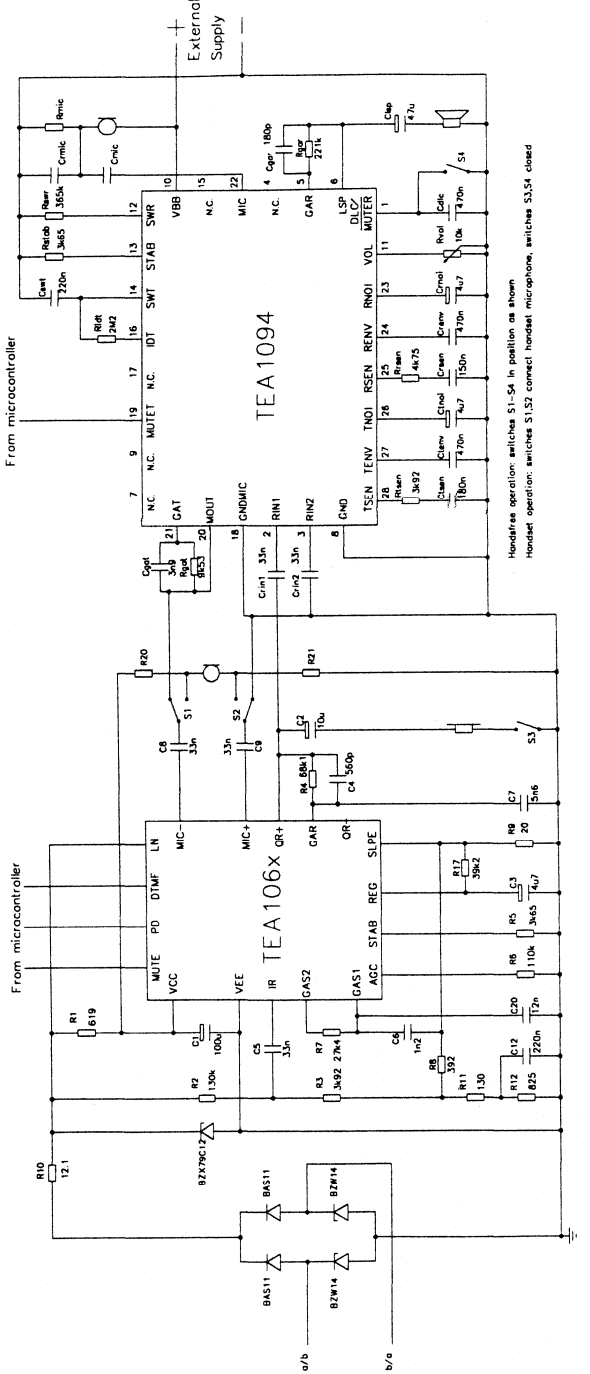


Figure D.3: Handsfree/handset application of the TEA1094

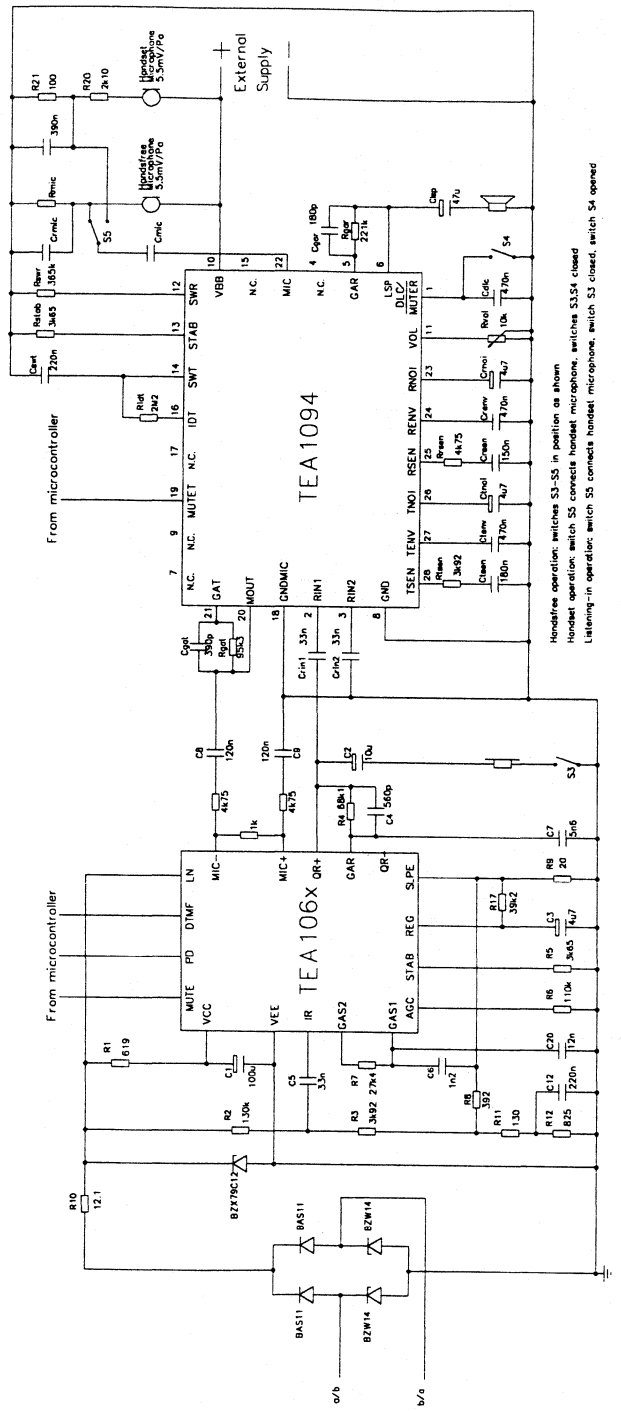


Figure D.4: Handsfree/handset/listening-in application of the TEA1094

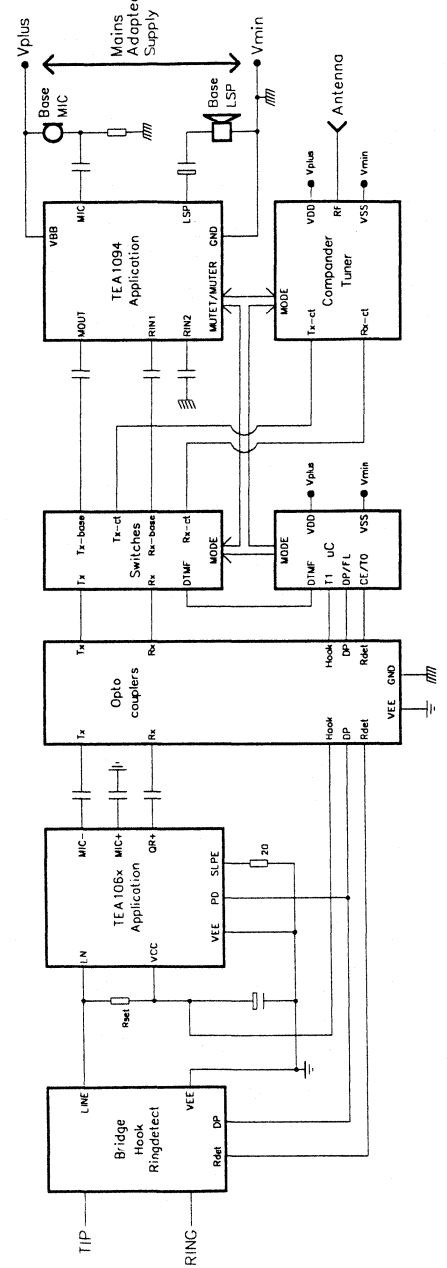


Figure D.5: Application proposal for cordless telephone with handsfree base

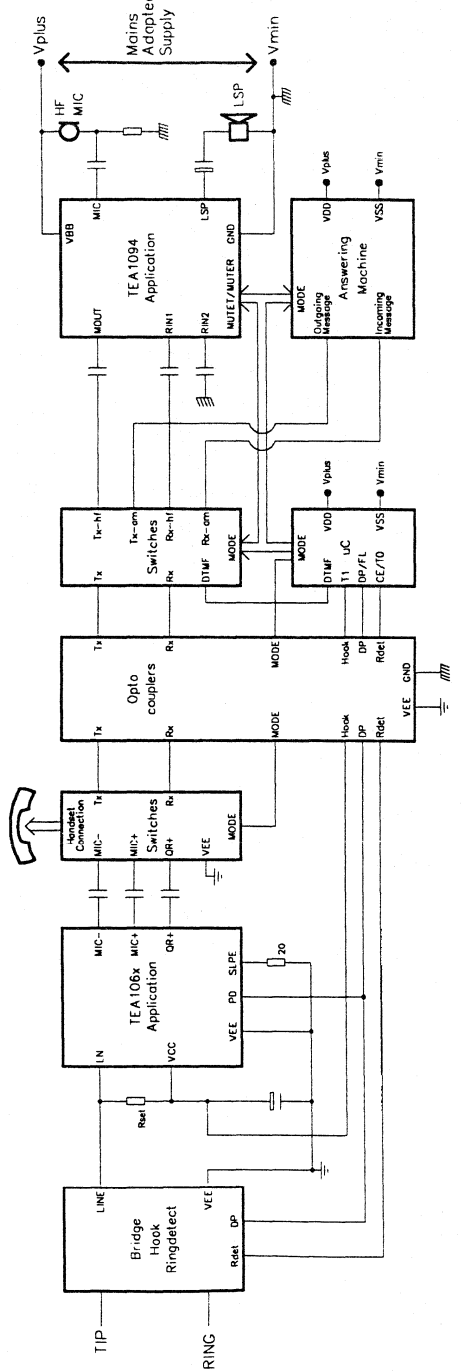


Figure D.6: Application proposal for corded telephone with answering machine

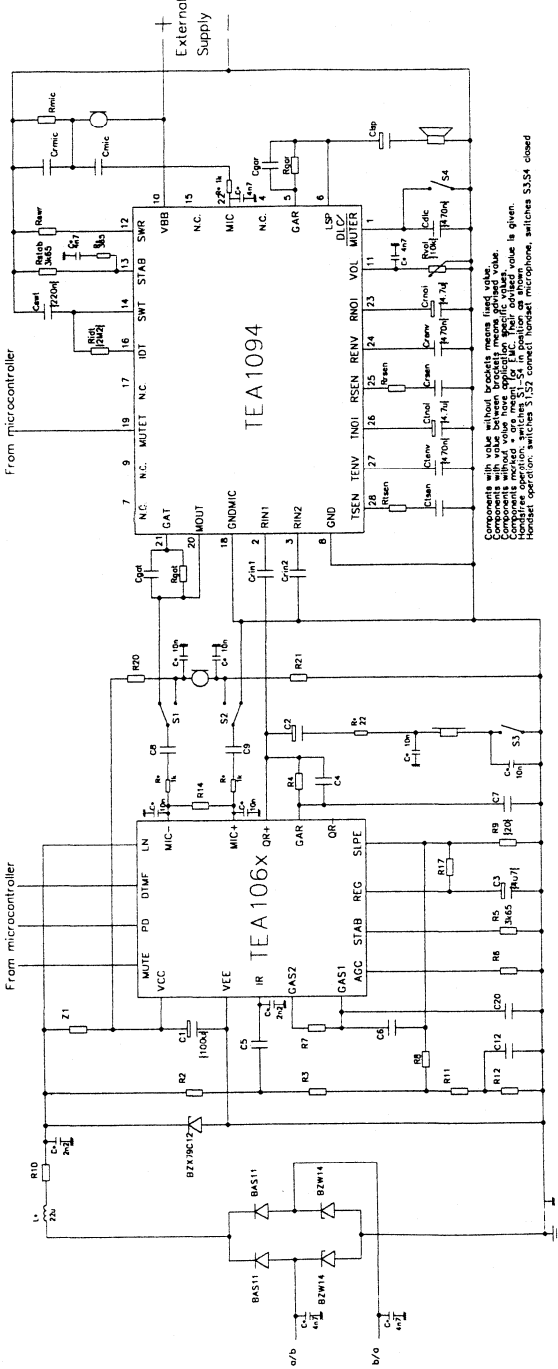


Figure D.7: Proposal for EMC of the TEA106x plus TEA1094 application

433MHz front-end with the SA601 or SA620 AN95021

Author: Rob Bouwer

ABSTRACT

Although designed for 1GHz, the SA601 and SA620 can also be used in the 433MHz ISM band. The SA601 performs amplification of the antenna signal and down conversion to a first IF. The SA620 has the same functionality, but also has a VCO on-chip. This VCO drives the mixer, so no external LO signal is required.

Applying the SA601 or SA620 means that a receiver with high sensitivity and wide dynamic range can be built without a lot of external components. The design will be easier compared with discrete Front Ends.

Combined with an IF system like the SA676, a high performance dual conversion receiver can be built. This receiver can operate from 2.7 to 5.5V allowing the use of a 3-cell battery. IF frequencies can be chosen according to one's needs with a maximum first IF of 100MHz and a maximum second IF frequency of 2MHz.

This application note explains how to use the SA601 or SA620 at 433MHz. The performance at 433MHz is discussed. The application circuit diagrams that are used to obtain the measurement results are shown.

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1. INTRODUCTION

The SA601 and SA620 address high performance applications at 1GHz like cellular and cordless phones. The SA601 comprises a Low Noise Amplifier (LNA) and a Mixer. The SA620 comprises, besides an LNA and Mixer, a VCO (Voltage Controlled Oscillator). Although intended for 1GHz, it is possible to apply these Front-Ends at lower frequencies.

This paper describes the performance of these devices at 433MHz. This band is being used for remote control systems, car alarms, telemetry, wireless audio links, etc.

By using the SA601 or SA620 followed by, for example an SA676 FM IF, a low voltage, high performance receiver for FM, AM, FSK, ASK demodulation can be built. The Front-Ends require only a few passive components for decoupling and signal handling. No extra circuitry is required for compensation for temperature and power supply variations. This will ease your 433MHz receiver design without trading off performance, and give you fast time to market.

2. SA601

The SA601 comprises a 1.2GHz LNA and Mixer. The block diagram is shown in Figure 1. In a receiver it performs the amplification of the antenna signal and the down conversion to the first IF frequency. This signal can then be handled by an IF system like the SA676 which takes care of AM and FM demodulation.

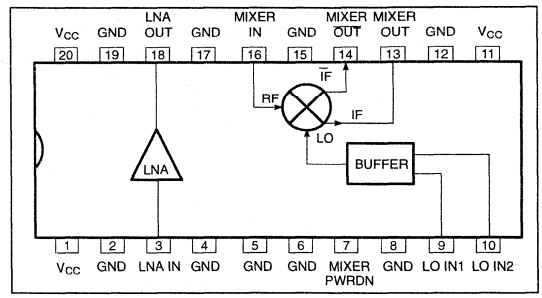

Figure 1. SA601 Block Diagram

Using the SA601 at 433MHz will show the following differences compared to the performance at 900MHz:

- The LNA will show a higher gain while having the same Noise Figure (NF)
- Because of this higher gain, the Intercept point (IP3) becomes less

The higher gain increases the sensitivity of the receiver. It also offers the possibility to allow some mismatch at the LNA input and hence, some gain loss. This means that a 50Ω source can be connected directly to the LNA input without matching. In case you do want to calculate the matching circuits for the LNA and mixer input, Table 1 shows the S-parameters of the LNA and mixer input at 433MHz.

The IP3 performance of the SA601 at 433MHz is worse than at 1GHz. However, it is still more than sufficient for applications in the 433MHz band.

Table 1. SA601 and SA620 S-parameters

	LNA				Mixer
	S_{11}	S_{22}	S_{21}	S_{12}	S_{11}
	R + j X	R + j X			R + j X
433MHz	34.0Ω - 62.8Ω	55.1Ω - 47.4Ω	5.4U ∠ 128°	62mU ∠ 68°	9.9Ω + 5.4Ω

2.1 Application circuit

The application circuit diagram is shown in Figure 2.

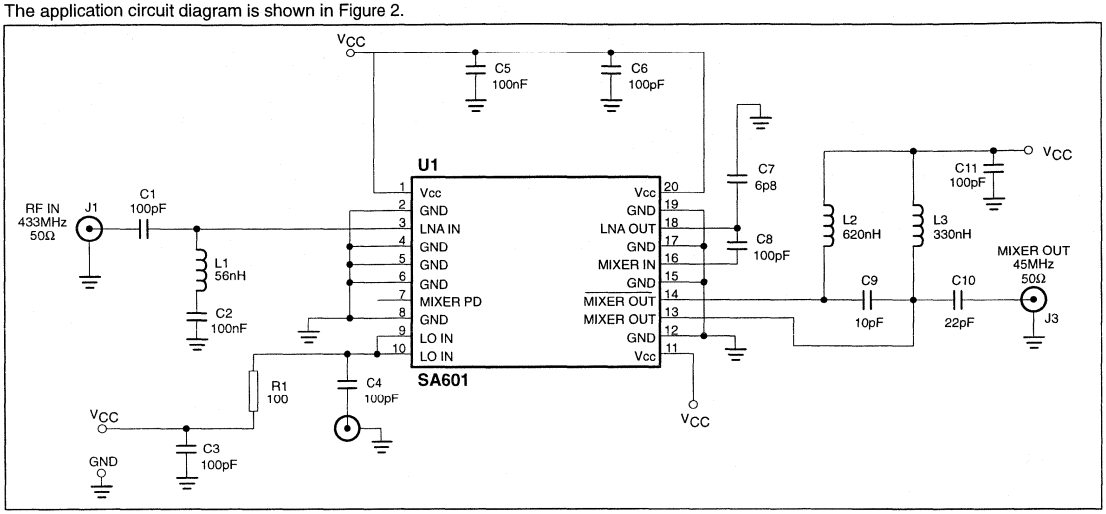

Figure 2. Application Circuit Diagram

Table 2. SA601 Application Components

C1	DC blocking	C9	Mixer output current combiner
C2	Time constant for LNA compensation loop	C10	Mixer output match to 50Ω load
C3	V_{CC} decoupling	C11	V_{CC} decoupling
C4	DC blocking	R1	LO input match
C5	Vcc decoupling	L1	AC blocking
C6	Vcc decoupling	L2	Mixer output current combiner
C7	LNA to Mixer input match	L3	Mixer output current combiner
C8	DC blocking		

Table 2 shows that most of the external components are for blocking DC at the in- and outputs and decoupling of the power supply. In your actual receiver the DC-blocking capacitors for RF IN, LO IN and MIXER OUT can be removed if there is no DC path present.

Capacitor C2 determines the bandwidth of the compensation loop of the LNA. The LNA is stabilized for temperature and power supply variations. To achieve a compensation loop which controls the LNA gain, the bandwidth of this control loop must be low compared to the actual input frequency. Otherwise the compensation loop and, thus, the LNA gain would be affected by the RF input signal.

To isolate C2 from the LNA input for 433MHz signals an inductor L1 is included. This forms a short for the compensation loop frequencies and an open for the 433MHz frequencies.

If there is already a DC path at the LNA input (J1) to ground, then L1 and C2 can be omitted. In that case C1 must be increased to 100nF. C1 has two functions then: block DC from the LNA input, and determine the bandwidth of the compensation loop.

The LNA output is matched to the Mixer input with a 6.8pF capacitor (C7) to ground and a series inductor of 9nH. This inductor is realized by the traces between LNA out and Mixer and the inductance of C8.

The SA601 mixer has differential outputs. This means that a direct interface with a symmetrical filter or symmetrical gain stage is possible. However, most filters are asymmetrical, therefore, a transformation from differential to single-ended is required. With a current combiner circuit[1], the differential output currents are shifted such that they are in phase. These currents are then combined to create a single-ended output. L2, L3 and C9 form this current combiner circuit.

The inductor can be calculated as follows:

- Choose a value for C9: 10pF
- F is 45MHz
- Calculate L for appropriate current combining

$$F = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot 2 \cdot C}}$$

$$L = \frac{1}{(2 \cdot \pi \cdot F)^2 \cdot 2 \cdot C} = \frac{1}{(2 \cdot \pi \cdot 45MHz) \cdot 2 \cdot 10pF}$$

$$L = 625nH$$

1. A current combiner circuit for better mixer conversion gain, Sheng Lee, Alvin K. Wong, Michael G. Wong, Philips Semiconductors

Figure 3 shows the implementation of the calculated component values.

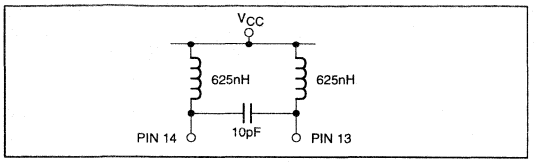

Figure 3. Current Combiner Circuit

After designing the current combiner circuit, the next step is to match the mixer output to the impedance of the load. In the application circuit the load is assumed to be 50 Ω. This is done to make evaluation more simple since most RF measurement equipment have 50 Ω inputs.

In addition to the impedance of the load (50 Ω), it is also important to know what the optimum load impedance is for the mixer output. For the SA601 mixer output this is 600 Ω. To create a matching from 600 to 50 Ω the circuit from Figure 4 is applied.

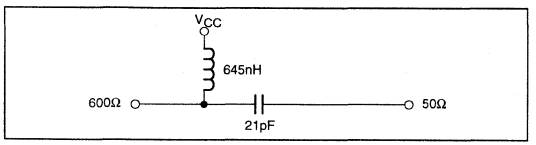

Figure 4. Mixer Output Match to 50Ω Load

The circuits from Figures 3 and 4 can be merged into one circuit as is shown in Figure 5. The values between brackets are the actual component values applied in the application circuit diagram.

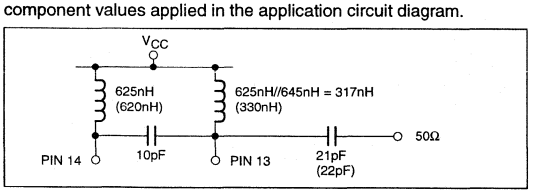

Figure 5. Mixer Output Circuitry With Current Combiner and 50Ω Matching

2.2 Measurement Results

For the measurements a power supply of 3V is applied. The RF frequency is 433MHz and the LO frequency is 478MHz with a level of -7dBm.

The current consumption of this application is 7.8mA.

2.2.1 Conversion gain, Noise Figure and IP3

In Table 3 the performance of the LNA and mixer is shown together with the overall performance.

Table 3. LNA, Mixer Measurement Results

	LNA	Mixer	LNA & Mixer	Units
Gain	15.4	9.2	24.7	dB
Noise Figure	1.5	12	2.5	dB
IIP3	-14.3	+1.7	-18.1	dBm

The results show that this Front-End offers 25dB of power gain with a noise figure contribution of only 2.5dB at 433MHz.

2.2.2 Isolation

Another important parameter for a Front-End receiver is the isolation between the Local Oscillator and the Antenna (LNA input). For 433MHz applications the requirement[2] is that spurious signals generated by the receiver have a maximum level of -57dBm for frequencies below 1GHz. The LO level measured at the LNA input is -53dBm. This means only 4dB extra suppression is required to meet the requirements. Because the Local Oscillator is offset 45MHz of the RF frequency, a simple bandpass filter, or the selectivity of the antenna, is already sufficient.

3. SA620

The SA620 comprises a 1.2GHz LNA, Mixer and VCO. The block diagram is shown in Figure 6. In a receiver the SA620 performs the amplification of the antenna signal and the down conversion to the first IF frequency. The VCO can be part of a phase-lock-loop or set to a fixed frequency by using a resonator. The output signal of the mixer can be handled by an IF system like the SA676 which takes care of AM and FM demodulation.

The S-parameters of the LNA and mixer input are the same as for the SA601. These parameters are shown in Table 1.

The LNA performance of the SA620 is the same as for the SA601. The mixer performance, however, is different. This is due to the output structure of the mixer. Figure 6 shows that there is one mixer output. Remember the SA601 has 2 mixer outputs which were combined using the current combiner circuit. Therefore, the mixer conversion gain is higher for the SA601 mixer. Furthermore, the SA620 incorporates a buffered VCO output (Pin 11) which can be used to drive the input of a frequency synthesizer.

3.1 Application circuit

Figure 7 shows the application circuit for a 433MHz receiver with a 478MHz VCO design.

2. ETSI I-ETS 300 220 Annex A.1.3.

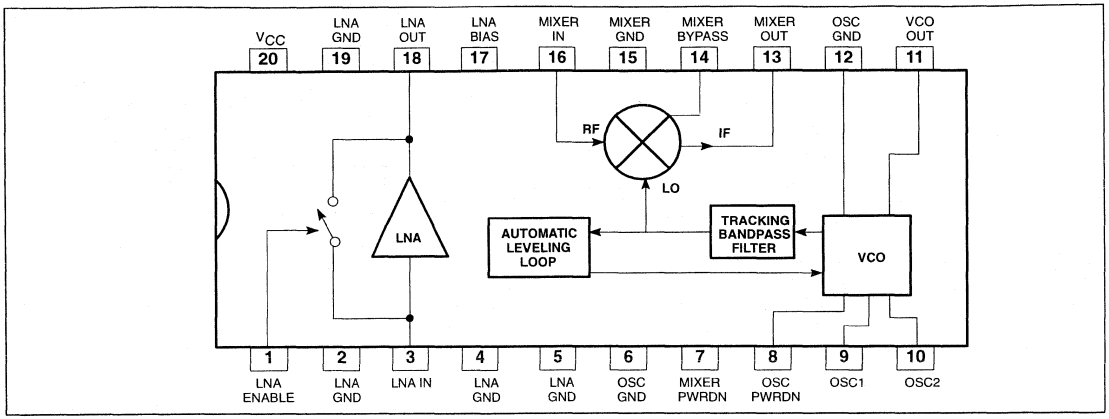

Figure 6. SA620 Block Diagram

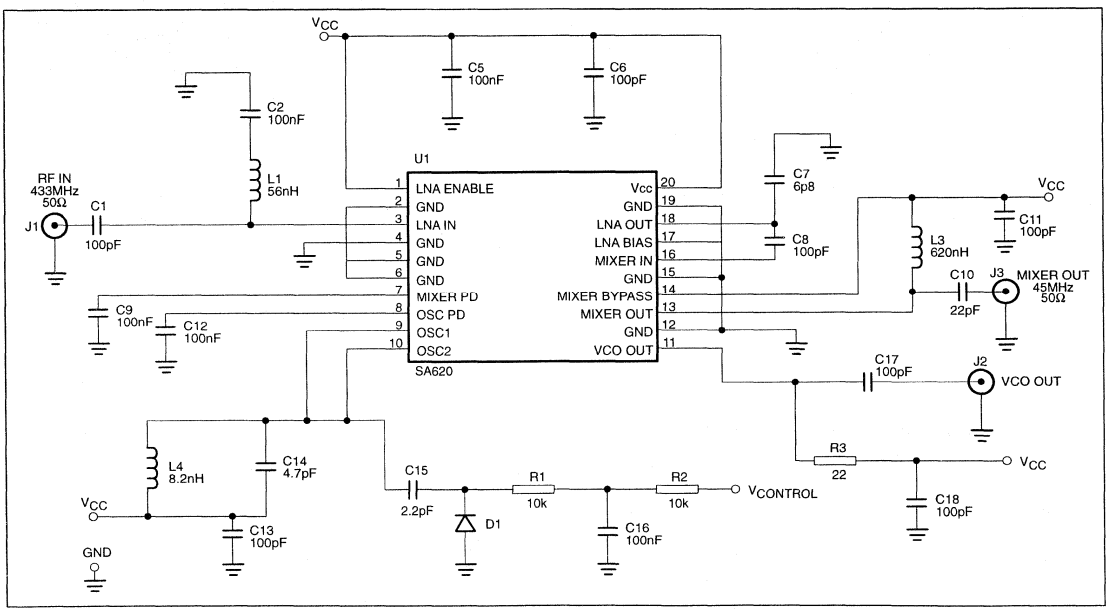

Figure 7. Application Circuit Diagram

Table 4 shows that most of the external components are for blocking DC at the in- and outputs and decoupling of the power supply. In your actual receiver the DC-blocking capacitors for RF IN, LO IN and MIXER OUT can be removed if there is no DC path present.

As with the SA601 capacitor, C2 determines the bandwidth of the compensation loop of the LNA. The LNA is stabilized for temperature and power supply variations. To achieve that a compensation loop controls the LNA gain. The bandwidth of this control loop must be low compared to the actual input frequency. Otherwise the compensation loop and, thus, the LNA gain, would be affected by the RF input signal. To isolate C2 from the LNA input for 433MHz signals, an inductor L1 is included. This forms a short for the compensation loop frequencies and an open for the 433MHz frequencies.

Table 4. SA620 Application Components

C1	DC blocking
C2	Timeconstant for LNA compensation loop
C5	V_{CC} decoupling
C6	V_{CC} decoupling
C7	LNA to Mixer input match
C8	DC blocking
C9	Mixer Bias decoupling
C10	Mixer output match to 50 Ω load
C11	V_{CC} decoupling
C12	VCO Bias decoupling
C13	V_{CC} decoupling
C14	Tuning capacitor
C15	Limits tuning range of VCO
C16	Filters noise at $V_{control\ line}$
C17	DC blocking
C18	V_{CC} decoupling
L1	AC blocking
L3	Mixer output match to 50 Ω load
L4	Tuning inductor
R1	Prevents loading of Tank circuit by the $V_{control\ line}$
R2	Filters noise at $V_{control\ line}$
D1	Varactor SMV 1204-099 Alpha Industries

If there is already a DC path at the LNA input (J1) to ground, then L1 and C2 can be omitted. In that case, C1 must be increased to 100nF. C1 has two functions then: block DC from the LNA input, and determine the bandwidth of the compensation loop.

The LNA output is matched to the Mixer input with a 6.8pF capacitor (C7) to ground and a series inductor of 9nH. This inductor can be realized by the traces between LNA Out and Mixer In and the parasitic inductance of C8.

The mixer output is matched to 50 Ω at 45MHz with L3 and C10.

The VCO output, Pin 11, delivers -20dBm into a 50 Ω load. The output level is set with R3. A lower output level can be achieved by reducing the value of this resistor. A higher value for R3 is not recommended because this will affect the VCO performance.

The components that determine the actual frequency of the VCO are L4, C14, C15 and D1 according to:

$$F = \frac{1}{2 \cdot \pi \cdot \sqrt{L4 \cdot \left(C14 + \left(\frac{C15 \cdot CD1}{C15 + CD1}\right)\right)}}$$

Figure 8.

The formula shows that the influence of the varactor D1 on the VCO frequency depends on the value of C15. That means that, if the tuning range of the VCO is too wide, it can be scaled back by reducing the value of C15.

The SA620 VCO can easily oscillate from 300 to 1.2GHz, so it is important to have only one resonance circuit at Pins 9 and 10. Also, parasitic resonances must be prevented, which can be accomplished by putting the components close to Pins 9 and 10, and by decoupling the power supply close to L4 and C14.

3.2 Measurement Results

For the measurements a power supply of 3V is applied. The RF frequency is 433MHz and the VCO frequency is tuned to 478MHz.

The current consumption of this application is 11.3mA.

3.2.1 Conversion gain, Noise Figure and IP3

In Table 5 the performance of the LNA and mixer is shown together with the overall performance.

Table 5. Measurement Results

	LNA	Mixer	LNA & Mixer	Units
Gain	15.5	4.5	19.5	dB
Noise Figure	1.5	8.5	2.6	dB
IIP3	-14.2	0.0	-18.5	dBm

The results show that this Front-End offers 19.5dB of power gain with a noise figure contribution of 2.6dB at 433MHz.

3.2.2 Isolation

The isolation between the LO signal and antenna input is -59dBm. The requirement[3] for 433MHz ISM band is -57dBm at the antenna input for signals outside the 433MHz band and below 1GHz. This means that, without any selectivity at the antenna input, this requirement is already met. In practice there will be selectivity from the antenna filter or the antenna itself, meaning the LO signal is further suppressed.

4. CONCLUSION

The advantages of using the SA601 or SA620 as a 433MHz Front End are:

- Ease of design
- Good performance
- Minimum amount of external components
- Power supply operation from 2.7 to 5.5V

When there is an external Local Oscillator available, the SA601 is the best choice because it has higher overall gain than the SA620. This is because the SA601 mixer has a differential mixer output. The SA620 has the benefit of having a VCO on-chip. With this VCO the LO frequency is generated, so no extra VCO module is required.

Both the SA601 and SA620 come in an SSOP20 and are in full volume production.

3. ETSI I-ETS 300 220 Annex A.1.3.

TEA1095 VOICE SWITCHED SPEAKERPHONE IC Application Note

Abstract

The TEA1095 is a high performance, low power consumption voice switched speakerphone IC designed for integration of a handsfree function in terminal environments.

A detailed description of the IC, advices on adjustments and a worked-out application example are contained in this report.

Summary

A detailed description of the TEA1095 is given. In conjunction with TEA1096 (transmission circuit with built-in loudspeaker amplifier), it offers a handsfree function. The TEA1095 incorporates a microphone amplifier and a duplex controller with signal and noise monitors on the transmit and receive channels. A cookbook gives the general application steps.

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1. INTRODUCTION

The TEA1095 is a circuit which, in combination with TEA1096 (transmission circuit with built-in loudspeaker amplifier), offers a handsfree function. It incorporates a microphone amplifier, a volume control of the receive channel and a duplex controller with signal and noise monitor on the transmit and receive channel. In contrary with the Philips handsfree circuits TEA1093 and TEA1094, the TEA1095 has neither integrated supply nor loudspeaker amplifier. This makes the TEA1095 more flexible for implementation in applications with external loudspeaker amplifier, external supply, such as cordless telephones and answering machines.

The function of the handsfree application will be illustrated with the help of fig 1.1.

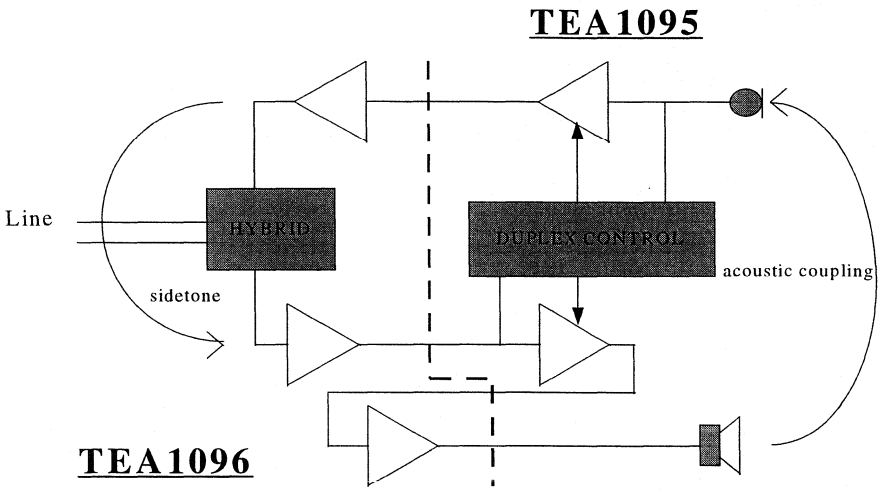


Fig.1.1 Handsfree telephone set principle

The left side of fig 1.1 shows a principle diagram of a part of the TEA1096 circuit by means of a receiving amplifier, a transmit amplifier, the loudspeaker amplifier and the hybrid. The right side of fig 1.1 shows a principle diagram of a part of the TEA1095 circuit by means of the microphone amplifier and the duplex controller.

As can be seen from fig 1.1, a closed loop is formed via the amplifiers, the antisidetone network and the acoustic coupling between loudspeaker and microphone. When the loop-gain is higher than one, the set starts howling. In a full-duplex application, this would be the case. To avoid howling, the duplex controller reduces the loop-gain to a value much lower than one.

The duplex controller of the TEA1095 monitors the signal and noise on both the transmit and the receive channel in order to detect which channel contains the 'largest' signal. As a result, the duplex controller reduces the gain of the channel which contains the smallest signal. This is done such that the sum of the transmit and the receive gains remains constant.

As a result, the circuit can be in three stable modes to be referred to throughout this report::

1. Transmit mode (Tx-mode): the gain of the microphone amplifier is at its maximum and the gain of the receive path (to loudspeaker amplifier) is reduced.

2. Receive mode (Rx-mode): the gain of the receive path is at its maximum and the gain of the microphone amplifier is reduced.
3. Idle mode (Ix-mode): the gain of the microphone amplifier and of the receive path are halfway their maximum and reduced values.

The difference between the maximum gain and the reduced gain is called the switching range.

This report gives a detailed description of the TEA1095 and its application with the TEA1096. The description is given by means of the block diagram of the TEA1095 (&2) and by discussing every detail of the sub-blocks (&3). The application is discussed by giving a guideline for application (the application cookbook &4) and by giving an application example (&5). EMC aspects are also discussed (&6). The appendices contain a measurement setup for the electro-acoustical adjustment of the TEA1095 handsfree application (A), a list of abbreviations (B) and application diagrams of the TEA1095 (fig. C1, C2).

2. BLOCK DIAGRAM

In this chapter, the block diagram of the TEA1095 is shown by means of fig.2.1. The pinning of the TEA1095 is given by means of fig.2.2. A short description of the block diagram is given including the function of the external components.

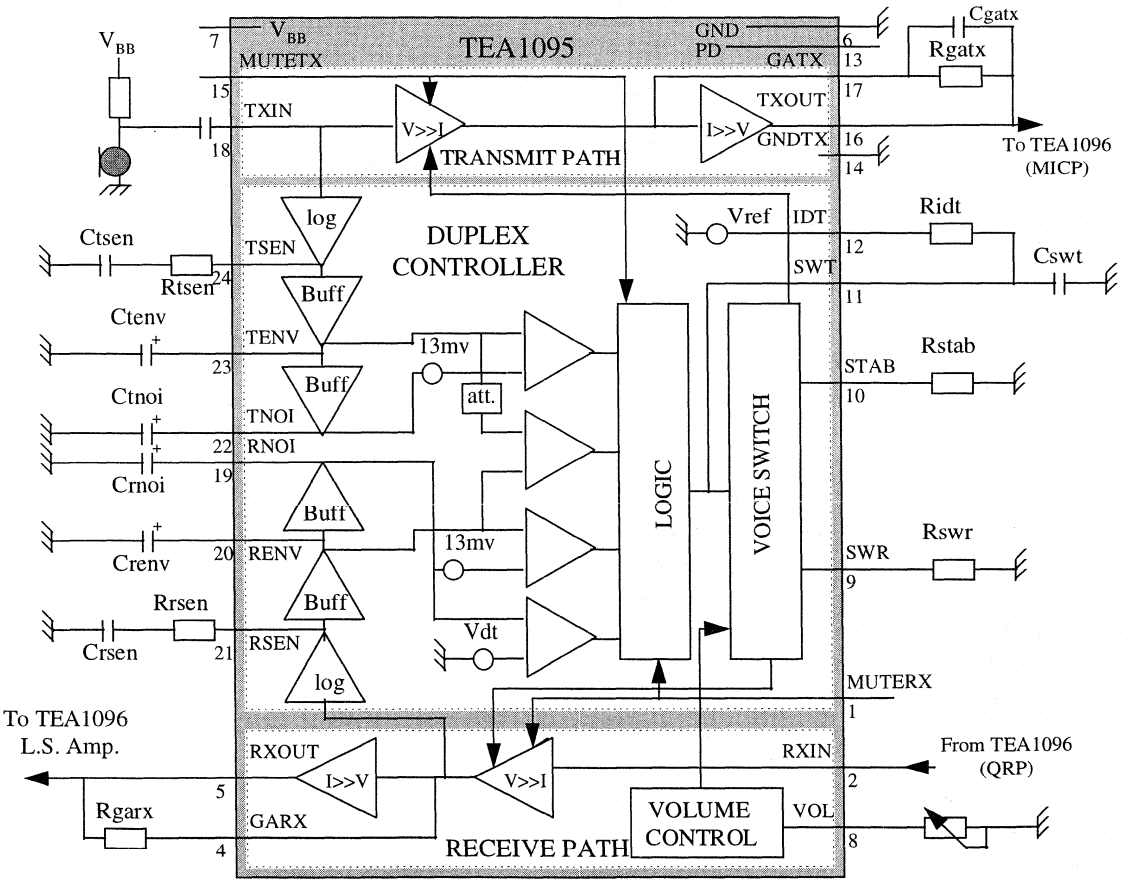


Fig. 2.1 Block diagram of TEA1095

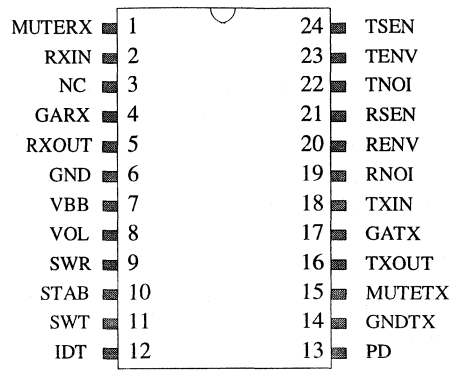


Fig. 2.2 Pinning of TEA1095

PIN	NAME	DESCRIPTION
1	MUTERX	Receive channel mute input
2	RXIN	Receive channel input
3	NC	Not connected
4	GARX	Receive gain adjustment
5	RXOUT	Receive channel output
6	GND	Ground reference
7	VBB	Positive supply input
8	VOL	Receive channel volume adjustment
9	SWR	Switching range adjustment
10	STAB	Reference current adjustment
11	SWT	Switching timing adjustment
12	IDT	Idle-mode timing adjustment
13	PD	Power-down input
14	GNDTX	Ground reference for microphone amplifier
15	MUTETX	Transmit channel mute input
16	TXOUT	Transmit channel output
17	GATX	Microphone gain adjustment
18	TXIN	Microphone amplifier input
19	RNOI	Receive noise envelope timing adjustment
20	RENV	Receive signal envelope timing adjustment
21	RSEN	Receive signal envelope sensitivity adjustment
22	TNOI	Transmit noise envelope timing adjustment
23	TENV	Transmit signal envelope timing adjustment
24	TSEN	Transmit signal envelope sensitivity adjustment

In fig.2.1 it can be seen that the IC consists out of four parts: the supply, the microphone amplifier, the receive path and the duplex controller. These blocks will be shortly described below including the function of the external components. The detailed description will follow in chapter 3.

Supply :

The circuit is supplied between pins VBB and GND. The TEA1095 can be switched into a low power consumption mode with the pin PD.

Microphone amplifier :

The handsfree microphone signal is amplified from pin TXIN to pin TXOUT. The signal reference is GNDTX, a "clean ground" which has to be connected to GND. The input TXIN has to be coupled to the microphone by means of a capacitor. The gain of the amplifier can be set with Rgatx. This amplifier can be muted by making pin MUTETX high.

Receive path :

The receive signal is amplified from pin RXIN to pin RXOUT. The input RXIN has to be coupled by means of a capacitor. The gain of the amplifier can be set with Rgarx, and the volume of the receive signal can be adjusted by means of the potentiometer connected between input VOL and GND. This channel can be muted by making pin MUTERX high.

Duplex controller :

From both the transmit and receive signal, signal and noise envelopes are made. The transmit signal envelope is on pin TENV and the receive one on pin RENV. The transmit noise envelope is on pin TNOI and the receive one on pin RNOI. The timing of the envelopes can be set by the capacitors Ctenv, Ctnoi, Crenv and Crnoi. The sensitivity of the envelope detectors can be set by means of the RC combinations Rtsen with Ctsen for the transmit envelope and Rrsen with Crsen for the receive one. The resistors set the sensitivity and the capacitors block the DC-component, creating also high-pass filters.

The logic determines to which mode (Tx, Rx or Ix-mode) the set has to switch over. The timing for switching to the Tx or the Rx -mode is determined with the capacitor Cswt. The timing for switching to the Ix-mode is set by the combination Cswt and Ridt. The switching range is determined by the resistor Rswr. Resistor Rstab has a fixed value.

3. DESCRIPTION OF THE TEA1095

This chapter describes in detail the four blocks of the duplex controller circuit TEA1095: the supply (3.1), the microphone amplifier (3.2), the receive path (3.3) and the duplex controller (3.4). For each block the principle of operation is described and its adjustments and performances are discussed.

All values given in this chapter are typical and at room temperature unless otherwise stated. For more details of the TEA1095 specification, see TEA1095 device specification.

3.1 Supply block

Principle of operation

As opposite to TEA1093 which includes an integrated supply which stabilizes a supply voltage out of the line current and as the TEA1094, the TEA1095 has no integrated supply. This makes the TEA1095 most suitable for applications where the handsfree controller is supplied from an external voltage source.

In fig. 3.1.1, different supply arrangements with TEA1095 are shown.

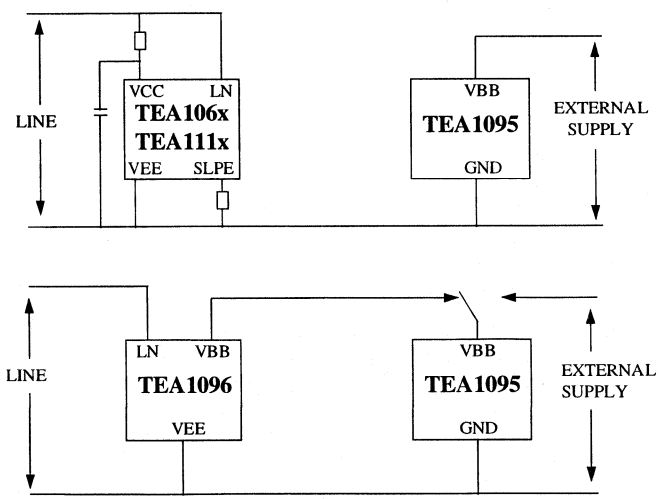


Fig. 3.1.1 Supply arrangement examples with TEA1095

As can be seen, the line current flows through the TEA106x or the TEA1096, while the TEA1095 is supplied from an external voltage source. Nevertheless, as can be seen in the bottom example, TEA1096 is able to provide this supply, leading to a line-powered very integrated solution. The common reference for all signals is GND on TEA1095 and VEE on TEA106x or TEA1096 side.

In case of a line-powered application using TEA106x or TEA111x, the TEA1095 as well as an external loudspeaker amplifier can be supplied via a large coil (or TEA1081) connected between line and VBB. At VBB,

a capacitor has to be connected to serve as reservoir. The TEA1095 and the loudspeaker amplifier have to be referenced at SLPE in order not to influence the transmission characteristics.
In fig.3.1.1 no galvanic insulation is drawn. When such is needed, the insulation can be done in the supply part or in the signal interfacing. In the supply part, the galvanic insulation can be done in the main-adaptor. In the signal interfacing between the TEA1095 and the TEA106x, the galvanic insulation can be done either with transformers or with opto-couplers.
The power consumption of the TEA1095 can be dramatically reduced when its functionalities are not required by making pin PD high.

Adjustments and performances

The voltage which can be applied between VBB and GND may vary between 2.9 V and 12 V. The 12 V is an absolute maximun rating. When a supply is used which may generate, during transients, a higher voltage, an appropriate protection device must be applied between VBB and GND in order to control this voltage.
The current consumption of the TEA1095 is typically 2.7 mA at VBB = 5 V. At higher voltages, the current consumption slightly increases.
In power-down mode, the current consumption is typically reduced to 140 µA at VBB = 5 V.

3.2 Microphone amplifier block

In the first paragraph of this chapter, the principle of operation of the microphone amplifier is described as well as its adjustments and performance. In the second paragraph, the mute transmit function is described.

3.2.1 Microphone amplifier

Principle of operation
In fig. 3.2.1 the block diagram of the microphone amplifier of the TEA1095 is depicted together with the interconnection with the TEA1096.

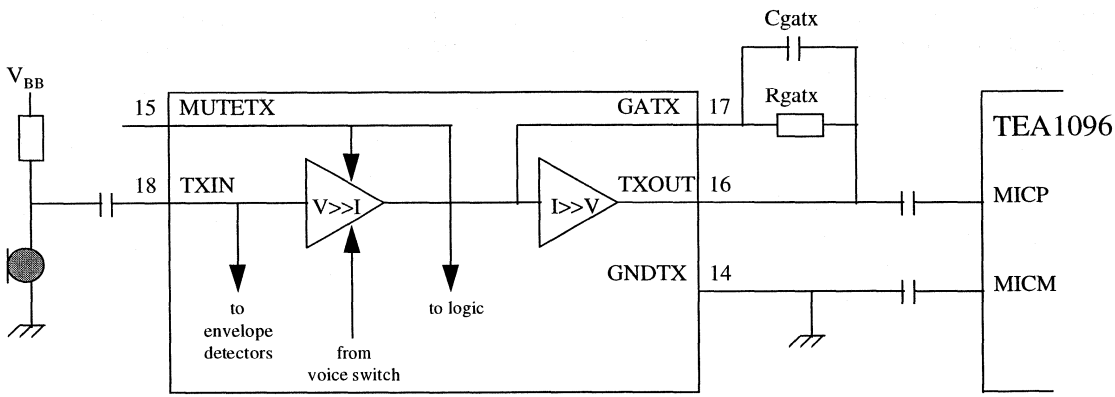


Fig. 3.2.1 Block diagram of the microphone path

As can be seen in fig.3.2.1, the microphone amplifier is referenced to pin GNDTX instead of being referenced to GND. This is in order to prevent interference from other blocks of the TEA1095 or of the application, GNDTX is called a clean ground. The input and output signals of the microphone channel have to be referenced to GNDTX. Pin GNDTX itself has to be referenced to GND.

The input of the microphone amplifier is pin TXIN. It is an assymmetrical input well suited for electret microphones. Induced signals in the short wire between the microphone and pin TXIN are assumed to be negligible. This in contrary with the handset microphone which is connected via the handset cord. The TEA106x/TEA111x families as well as the TEA1096 have symmetrical microphone inputs.

The output of the microphone amplifier is pin TXOUT. When interconnecting the TEA1095 and the TEA1096, pin TXOUT is preferably connected to the TEA1096 input MICP, in that case, pin MICM of the TEA1096 is connected to pin GNDTX.

As can be seen in fig.3.2.1, the microphone amplifier is built up out of two parts: a preamplifier and an end-amplifier. The gain of the preamplifier is determined by the duplex controller block, see & 3.4. The gain of the end-amplifier is determined by the external feedback resistor Rgatx.

The overall gain (Atx) of the microphone amplifier from input TXIN to output TXOUT in TX-mode is given as:

Atx = 20 * log (0.72 * Rgatx / Rstab).

With Rstab being the resistor at pin STAB of 3.65 kΩ.

Adjustments and performances

A handsfree microphone, referenced to GNDTX, can be connected to the input TXIN via a DC blocking capacitor Ctxi. Together with the input impedance of pin TXIN of 20 kΩ, this capacitor form a first order high-pass filter which can be used to adjust the transmit curve.

The handsfree electret microphone can be supplied from VBB via a resistor. However, during normal operation, VBB may contain a small riple, and due to poor power supply rejection of electret microphones it is advised to add an RC smoothing filter in the feeding part, as shown in fig.3.2.2.

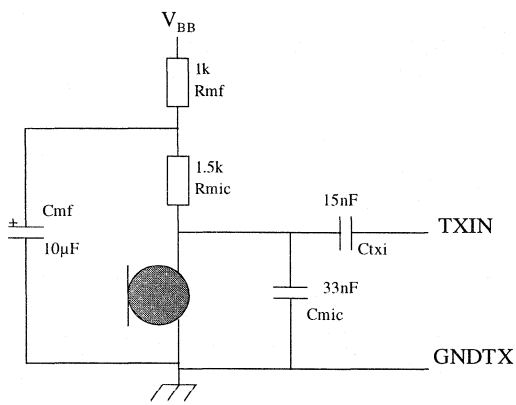


Fig. 3.2.2 Supply arrangement for electret microphone

As shown in fig.3.2.2, the RC smoothing filter is referenced to GNDTX in order to have one good reference for the whole microphone signal path. On the printed circuit board lay-out GNDTX can be connected with a separate wire to pin VEE of the TEA1096 in order to reduce ground interference as much as possible.

The sensitivity of the electret microphone is set via resistor Rmic. By putting a capacitor Cmic in parallel with the microphone, a first order low-pass filter is formed for the microphone signal in order to adjust the transmit curve.

Via the resistor Rgatx, the gain of the microphone amplifier can be adjusted from -15 to +25 dB to suit application specific requirements. With the resistor Rgatx = 30.1 kΩ, the gain equals typically 15.5 dB.

Capacitor Cgatx is applied in parallel with resistor Rgatx to ensure stability of the microphone amplifier, it also provides a first order low-pass filter for the adjustment of the transmit curve.

The input of the microphone amplifier can handle signals up to 18 mVrms with 2% total harmonic distortion. However, the microphone input signal is also used by the duplex controller, see &3.4. At 10 mVpeak at the input, the positive part of the signal on pin TSEN starts clipping which might influence the switching behavior. It is therefore advisable to keep the microphone input signal below this level.

The output drive capability at pin TXOUT is 20 µArms.

The output noise at TXOUT of the TEA1095 is -100 dBmp (psophometrically weighted) at a gain of 15 dB. With a sending gain of the TEA1096 set at 35 dB (total handsfree transmit gain of 50 dB), the noise level on the line will be : -65 dBmp.

In TX-mode, the noise level will be at its maximum. In Ix-mode and Rx-mode, the noise at TXOUT will be lower because the contribution of the preamplifier is reduced. However, the bottom level of the sending noise at TXOUT is limited by the end-amplifier and is about -110 dBmp.

The bottom level of the sending noise on the line is determined either by the speech circuit (TEA1096 or TEA106x/TEA111x) or by the noise at TXOUT increased by the transmit gain of the speech circuit, whichever is largest. When in Ix-mode, the noise on the line is due to TXOUT noise level, it can be reduced by changing the distribution of the gains between TEA1095 and speech circuit : increasing the transmit gain of the TEA1095 and decreasing with the same value the gain on the speech circuit side by modification of the attenuation placed between TXOUT and MICP of the speech circuit.

3.2.2 Transmit mute

During handsfree operation, the microphone can be muted by making pin MUTETX high, so conversation cannot be heard by the other party. When the microphone amplifier is muted, automatically the TEA1095 switches over to the RX-mode, see also &3.4.

When a logic high is applied to MUTETX, meaning the voltage on MUTETX is higher than 1.5 V, the microphone preamplifier is muted. The end-amplifier can still be used by applying a current signal on GATX. The obtained gain reduction is 80 dB. The current which has to be sourced into pin MUTETX when high is typically 2.5 µA.

When MUTETX is logic low, meaning the voltage on MUTETX is lower than 0.3 V or pin MUTETX is left open, the microphone amplifier is not muted.

The maximum allowable voltage on pin MUTETX is VBB+0.4 V, the minimum allowable is GND-0.4 V.

3.3 Receive path block

The block diagram of the complete receive path block is depicted in fig.3.3.1

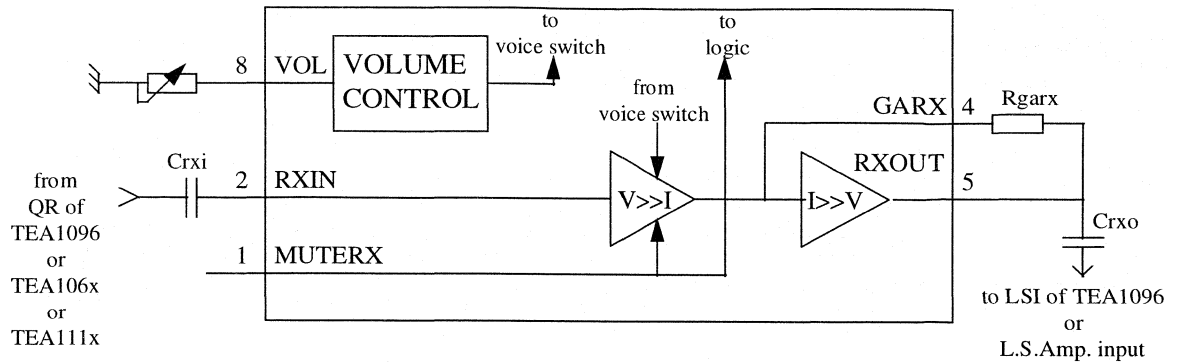


Fig.3.3.1 Principle of the receive path

As can be seen in fig.3.3.1, the receive channel is built up out of two parts: the receive path itself and the volume control. In the first paragraph of this chapter, the principle of operation of the receive path is described as well as its adjustments and performances. In the second paragraph, the same items are described for the volume control. In the third paragraph, the receive mute function is described.

3.3.1 Receive path

Principle of operation

As can be seen in fig.3.3.1, the input of the receive channel, pin RXIN is assymetrical and the signal has to be referenced to GND. The input RXIN can be connected, via a decoupling capacitor, to the earphone output QRP of the speech circuit (TEA1096 or TEA106x/TEA111x).

The output of the receive channel is pin RXOUT. When interconnecting the TEA1095 and the TEA1096, pin RXOUT is connected via a decoupling capacitor to input pin LSI of the TEA1096.

As can be seen in fig.3.3.1, the receive path itself is built up out of two parts: a preamplifier and an end-amplifier. The gain of the preamplifier is determined by the duplex controller block. The gain of the end-amplifier is determined by the external feedback resistor Rgarx.

The overall gain (Arx) of the receive path from input RXIN to output RXOUT is given as:

$$Arx = 20 * \log(0.46 * Rgarx / Rstab).$$

With Rstab being the resistor at STAB of 3.65 kΩ.

Adjustments and performances

The input signal for the receive channel has to be coupled in via the capacitor Crxi to block DC. Together with the input impedance of 20 kΩ at RXIN, a first order high-pass filter is introduced which can be used to adjust the receive curve and/or to reduce any low frequency unwanted signal coming from the line.

The input RXIN can handle signal up to 390 mVrms with a total harmonic distortion of 2%.

The input RXIN is biased at around 0V with respect to GND. By applying a signal to the input, it can become negative. The protection on this pin is made different from other pins which makes it possible to have RXIN as low as -1.2 V without damaging the circuit.

The output RXOUTcan be connected to the LSI input of TEA1096 or the input of any loudspeaker amplifier via a decoupling capacitor Crxo. The output is biased at 1.4 V referenced to GND. Together with the input impedance of the loudspeaker amplifier, Crxo forms a first order high-pass filter. With the resistor Rgarx, the gain of the receive path can be adjusted from -20 to +20 dB. The gain equals typically 6.3 dB with resistor Rgarx=16.2 kΩ. A capacitor Cgarx can be connected in parallel with Rgarx to provide a low pass filter which can be used to adjust the loudspeaker amplifier curve.

The output drive capability at pin RXOUT is 100μArms.

The noise level at the output RXOUT is -91 dBmp at a gain of 6 dB and with the input RXIN shorted with 200 Ω to GND.

3.3.2 Volume control

Principle of operation

Via the volume control block, the volume of the receive signal can be adjusted by the external potentiometer connected to pin VOL. By changing the potentiometer resistance, the gain of the preamplifier varies through the duplex controller. Volume control doesn't affect the transmit gain in Tx-mode.

Adjustments and performances

Out of pin VOL a current Ivol, set by Rstab, see &3.4, is flowing which is proportional to the absolute temperature (PTAT). At room temperature this current is around 10 μA. Together with the resistance of the potentiometer, the current Ivol creates a PTAT voltage on pin VOL. This PTAT voltage is processed by the volume control block, as a result, a temperature independent volume reduction of the output receive signal of 3 dB is obtained at approximately every increase of 950 Ω of the potentiometer resistance.

This means that a linear potentiometer can be used to control the volume logarithmically, thus in dB. With the advised value of 10 kΩ, the maximum gain reduction of the volume control is more than 30 dB. However, this maximum gain reduction is limited by the switching range, see &3.4. When the resistance of the potentiometer is zero, the receive gain is maximum in Rx-mode.

When digital volume control is desired, the switches can be either MOSFETs or analog switches with very low saturation voltage. Due to saturation voltage, it is advised not to use bipolar transistors as switches.

When a voltage is applied to pin VOL to control the volume, preferably this voltage has to be a PTAT voltage source. If not, the obtained gain varation is no longer temperature compensated.

3.3.3 Receive mute

During handsfree operation, the receive channel can be muted by making pin MUTERX high. As a result the receive signal is reduced by 80 dB, also the TEA1095 is internally forced into Tx-mode.

When a logic high is applied to MUTERX, meaning a voltage higher than 1.5 V, the receive preamplifier is muted. The end amplifier can still be used by applying a current signal on GARX. The obtained gain reduction is 80 dB when the volume control is set at maximum volume. The current which has to be sourced into pin MUTERX when high is typically 2.5 μA.

When MUTERX is logic low, meaning the voltage is lower than 0.3 V or pin MUTERX is left open, the receive path is muted.

The maximum allowable voltage on pin MUTERX is VBB+0.4 V, the minimum allowable is GND-0.4 V.

3.4 Duplex controller block

In this chapter, the principle of operation of the duplex controller will be described as well as its adjustments and performances. This will be done with the help of fig.3.4.1.

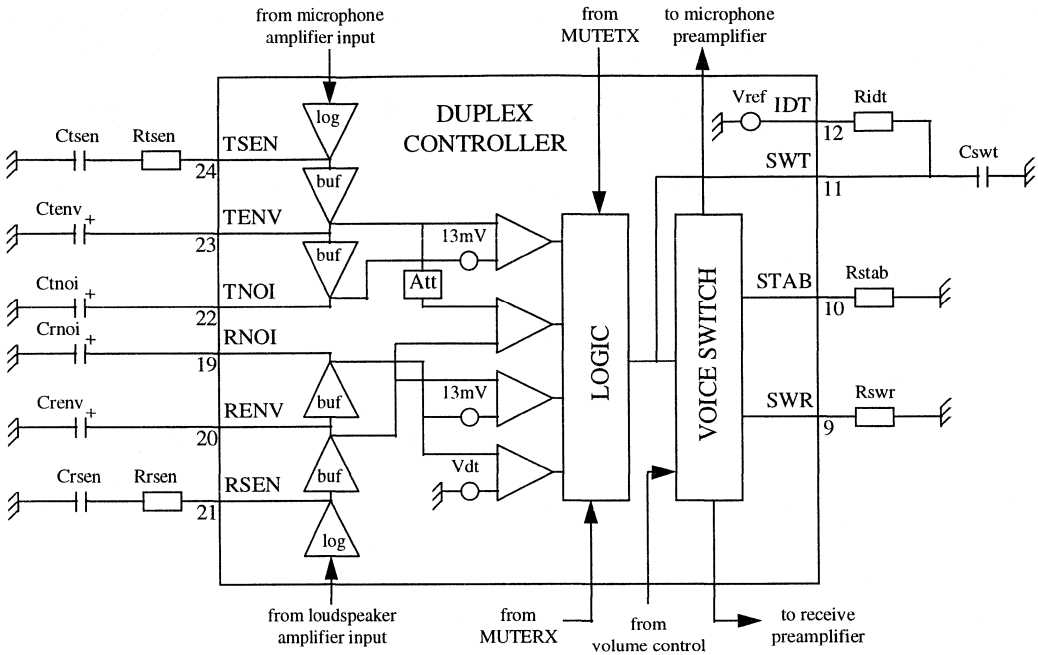


Fig. 3.4.1 Principle of the duplex controller

As can be seen in fig.3.4.1, the duplex controller is built up out of signal and noise envelope detector, decision logic and a voice switch.

The signal and noise envelope detectors determine the signal envelope and the noise envelope of both the transmit and receive signal. These envelopes are used by the decision logic to determine to which mode the TEA1095 has to switch over (Tx, Rx or Ix-mode). The logic charges and discharges the capacitor Cswt and the resulting voltage on pin SWT controls the voice switch. The voice switch switches over the TEA1095 between the three modes while keeping the loopgain constant.

In paragraphs 3.4.1 to 3.4.3, the principle of operation of the three parts is given. In paragraph 3.4.4, the adjustments and performances of the complete duplex controller are given.

3.4.1 Signal and noise envelope detectors

The signal and noise monitors of the transmit and receive channels are globally the same.

Therefore, the principle of the detectors will be explained with the help of one of them: the signal and noise detector of the transmit channel.

The microphone signal on pin TXIN is sent to the first stage of the detector, see fig.3.4.1. The first stage amplifies the microphone signal from pin TXIN to pin TSEN with an internal gain of 40 dB. Via the RC combination RtsenCtsen, the signal on TSEN is converted into a current. This conversion determines the sensitivity of the envelope detector. The current is logarithmically compressed and internally converted to a voltage which represents the compressed microphone signal. At room temperature, an increase of the microphone signal with a factor of 2 will increase the signal envelope with 18 mV if the current through TSEN stays between 0.8 and 160 μArms. Outside this region the compression is less accurate.

The compressed microphone signal is buffered by the second stage to pin TENV. As the buffer can source 120μA and sink 1μA, the signal on TENV follows the positive peaks of the compressed signal, this signal is called the signal envelope. The time constants of the signal envelope are therefore determined by the combination of the internal current sources and the capacitor Ctenv.

The voltage on TENV is buffered by the third stage to pin TNOI. As this buffer can source 1 μA and sink 120 μA, the signal on TNOI follows the negative peaks of the signal on TENV. This is called the noise envelope because it represents the background noise. The time constants of the noise envelope are determined by the combination of the internal current sources and the capacitor Ctnoi. Both capacitors Ctnoi and Crnoi are provided with a start-up circuit. During start-up the capacitors are charged with approximately 40 μA up to 1.9 V. The starter will restart when the voltage on the capacitors drops below 0.9 V.

As can be seen in fig.3.4.1, the principle of operation of the signal and noise envelope detectors of the receive channel is equal to the one of the transmit channel. However, the gain of the first stage (input to pin RSEN) is 0 dB instead of 40 db for the transmit channel, this is in order to compensate the level on TXIN which is not yet amplified.

The behavior of the envelopes is illustrated in fig.3.4.2 where the signal and noise envelope of one channel are depicted together with the input signal.

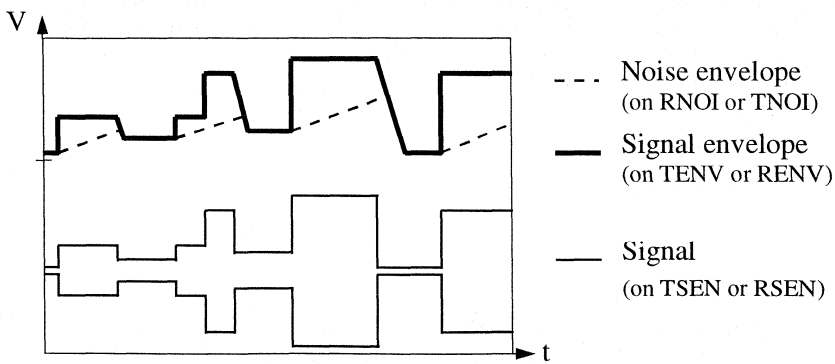


Fig. 3.4.2 Typical behavior of the signal and noise detectors

In fig.3.4.2 it is shown that when the input signal raises quickly, the envelope signal follows immediately and the noise envelope slowly follows the envelope signal. When the input signal decreases, the envelope signal follows

immediatly but nevertheless less quickly than when it raises, the noise envelope follows immediatly the decrease of the envelope signal and never crosses it.

3.4.2 Decision logic

The signal and noise envelopes of the transmit and receive signal are used by the decision logic to determine in which mode the TEA1095 has to be.

The output of the logic is a current source which charges or discharges the capacitor Cswt at pin SWT. If the logic determines Tx-mode, the capacitor Cswt is discharged with 10 µA. When Rx-mode is determined, Cswt is charged with 10 µA. When Ix-mode is determined, the current source is zero and the voltage on SWT becomes equal to the voltage on pin IDT via the current provided through the resistor Ridt. The time constants of the duplex controller are therefore determined by the combination of the internal current sources, the capacitor Cswt and the resistor Ridt.

As can be seen in fig.3.4.1, the envelopes are not used directly by the decision logic.

First, to have a clear choice between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference of 13mV. This so called speech/noise threshold is implemented in both the receive and the transmit channel. At the end of paragraph 3.4.4 a way to increase this threshold is discussed.

Second, the signal on TXIN contains both the signal of the local talker as well as the signal coming from the loudspeaker (acoustic coupling). In Rx-mode, the contribution of the loudspeaker overrules the contribution of the local talker. As a result, the signal envelope on TENV is mainly formed by the loudspeaker signal, to correct this, an attenuator is placed between TENV and the TENV/RENV comparator. The attenuation equals the attenuation applied to the microphone amplifier gain. Thus when the TEA1095 is in Rx-mode, the attenuation equals the switching range.

Third, when a dial tone is present on the line, without measures this would be recognized as noise after some delay because its level is constant. As a result, the TEA1095 would go to Ix-mode and the user of the set would hear the dial tone fade away. Therefore, a dial tone detector is incorporated which doesn't consider input signals as noise when they have a level higher than the dial tone level. The dial tone level, represented by Vdt in fig.3.4.1, is adjustable by Rsen.

When these three corrections are made, the signal and noise envelopes are used by the comparators and the logic. As already explained, the output of the logic is a current source. The relation between the current source and the output of the comparators is given in the table of fig.3.4.3. If for instance, TENV>RENV (transmit signal larger than receive signal) and TENV>TNOI (transmit signal more than 4.3 dB larger than noise level), then the output current will be -10 µA.

Comparator TENV/TNOI	1	x	x	0	x
Comparator TENV/RENV	1	0	0	1	0
Comparator RENV/RNOI	x	1	x	x	0
Comparator RNOI/Vdt	x	x	1	x	0
Output current	-10µA	+10µA	+10µA	0µA	0µA

Fig.3.4.3 Truth table of the detection logic

When pin MUTETX is made high, see paragraph 3.2.2, the output current is forced to be +10 µA, which forces the TEA1095 into Rx-mode and mutes the microphone amplifier. When pin MUTERX is made high, see

paragraph 3.3.3, the output current is forced to be -10 µA, which forces the TEA1095 into Tx-mode and mutes the receive path. When both MUTETX and MUTERX are made high, both channels are muted.

The voltage on pin SWT is internally limited to IDT-0.4 V and IDT+0.4 V.

3.4.3 Voice switch

With the voltage on pin SWT, the voice switch regulates the gain of the microphone preamplifier and the receive channel preamplifier in such a way that the sum of the transmit and receive gain is kept constant. This is done to keep the loop gain of the handsfree telephone set constant, see also the introduction &1. The switch-over behavior of the voice switch will be described with the help of fig.3.4.4.

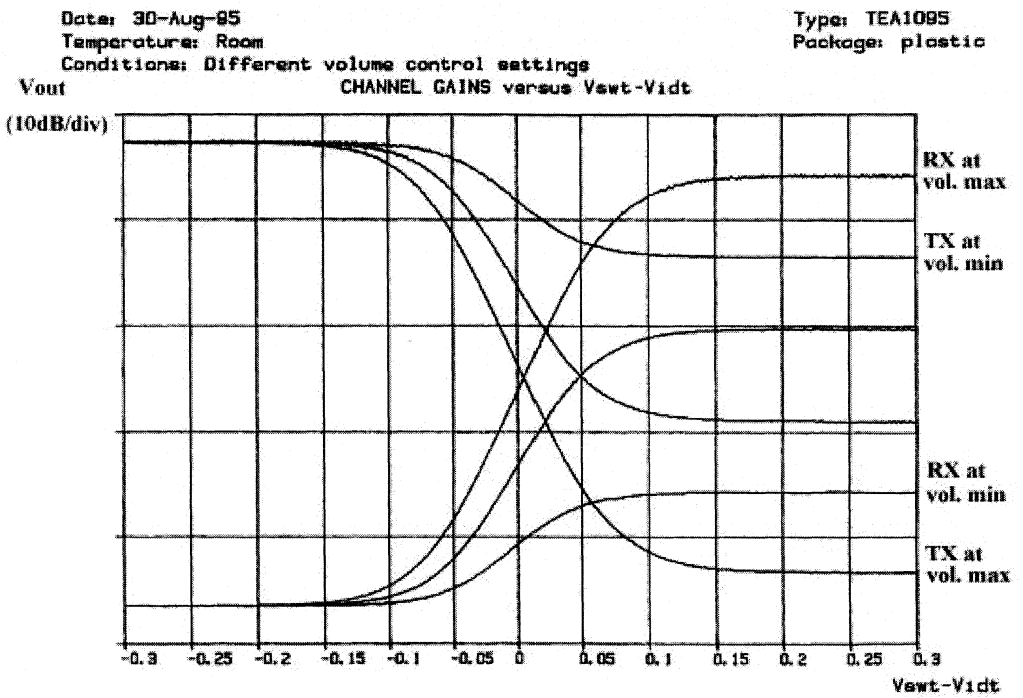


Fig. 3.4.4 Behavior of the voice switch

When the voltage on SWT is more than 180 mV below the voltage on IDT, the TEA1095 is fully switch to Tx-mode (gain of the transmit path at maximum and gain of the receive path at minimum). When the voltage on SWT is more than 180 mV above the voltage on IDT, the TEA1095 is fully switch to Rx-mode (gain of the receive path at maximum and gain of the transmit path at minimum). The TEA1095 is considered to be in Ix-mode when the voltage on SWT equals the voltage on IDT. When the capacitor Cswt is charged or discharged, the voltage on SWT varies and as a result the voice switch will smoothly switch over between the modes keeping the sum of the transmit and receive gains constant.

The difference between the maximum and the minimum gain of the receive or transmit preamplifiers is called the switching range. This range is determined by the ratio of Rswr and Rstab, see paragraph 3.4.4. Both Rswr and Rstab set internally used reference currents which are proportional to absolute temperature (PTAT).

As already stated in &3.3 the volume control acts upon the receive preamplifier via the control of the voice switch. As a result, the loop gain of the handsfree set is kept constant when the volume of the receive path is adjusted. However, the voice switch is designed such that the volume control has no influence in Tx-mode. In the extreme case, when the volume of the receive channel is reduced with the value of the switching range, the TEA1095 virtually does not switch over. In order to avoid inversion of the gain in Rx-mode, the volume control range of the TEA1095 cannot be larger than the switching range.

3.4.4 Adjustments and performances

The adjustment of the duplex controller has to be performed according to the following recipe:

1. Determine the switching range
2. Determine dial tone detector level
3. Determine sensitivity
4. Determine timings

Ad 1. Determine switching range

The switching range Asw is determined by the ratio of the two resistors Rswr and Rstab according to:

$$Asw\ (dB) = 20 * \log (Rswr / Rstab)$$

The resistor Rstab has to be taken 3.65 kΩ. The value of the resistor Rswr can vary between 3.65 kΩ and 1.5 MΩ resulting in a switching range between 0 dB and 52 dB. With Rswr of 365 kΩ, the switching range is typically set to 40 dB.

The switching range is calculated out of the loop gain (Aloop). In a handsfree application, the loop gain has to be smaller than one (<0 dB) and can be calculated as follows:

$$Aloop = Atx1095 + Atx1096 + Ast + Arx1096 + Arx1095 + Als1096 + Aac - Asw.$$

with Atx1095 = sending gain of the TEA1095 (TXIN to TXOUT)

Atx1096 = sending gain of the TEA1096 (MIC to LN)

Ast = electrical sidetone

Arx1096 = receive gain of the TEA1096 (LN to QR)

Arx1095 = receive path gain of the TEA1095 (RXIN to RXOUT)

Als1096 = loudspeaker amplifier gain of the TEA1096 (LSI to QLS)

Aac = electro-acoustic coupling from loudspeaker to microphone (QLS to TXIN)

Asw = switching range

In this calculation, the worst case has to be taken for Ast and Aac. Furthermore, for safety, it is advised to choose Asw large enough to compensate spreads (margin from 10 to 15 dB).

The electrical sidetone is the difference (in dB) between the wanted receive signal on the TEA1096 and the unwanted part of the transmit signal received while having an equal signal level on pin LN for both the transmit and the receive signal. Ast is dependent of frequency and connecting conditions of the set (line lenght, line impedance).

The acoustic coupling is dependent on the environment of the telephone set, for the determination of Aac, the worst condition has to be searched.

If a certain minimum volume control range is required, the switching range must not be chosen smaller.

In appendix A, a method for measuring the required switching range, based on the above calculation, is given.

It is also possible to determine the switching range by experiments:

As for the calculation, it is necessary to identify what are the worst conditions for sidetone and acoustic coupling. In these worst conditions, Rswr can be adjusted in such a way that the handsfree telephone set is at the limit of howling. Then the determined value of Rswr must be increased in order to have a margin of 10 dB to 15 dB.

Handsfree behavior will be more comfortable for the user if the switching range is not too large. So, **it is advised to take care of the acoustic coupling between the loudspeaker and the microphone** which might come from the cabinet of the terminal itself.

Ad 2. Determine dial tone detector level

The dial tone detector level is determined by the value of Rrsen according to:

$$V_{dialtone} = 4.2\ \mu A * R_{rsen}$$

With Rrsen of 10 kΩ, the dial tone detector level will be 42 mVrms. This means, a continuous signal on the input RXIN larger than 42 mVrms will be recognized as a dial tone.

Ad 3. Determine sensitivity

The sensitivity is set by Rrsen and Rtsen. The resistor Rrsen is already determined by the dial tone detector level. It must however be checked if the choosen value for Rrsen is a practical one for the dynamic range of the logarithmic compressor. The optimized range for the compression is when the current flowing through pin RSEN is between 0.8 to 160 μArms. This means that at nominal receiving signal the current through RSEN is preferably around 11 μArms. This gives a maximum dynamic range of plus and minus 23 dB.

The same counts for pin TSEN.

The resistor Rtsen has to be chosen in such a way that both channels have the same priority for the duplex controller. This can be obtained by choosing Rtsen according to:

$$20 * \log(R_{tsen}) = 20 * \log(R_{rsen}) - A_{tx1095} - A_{tx1096} - A_{st} - A_{rx1096} + A_{tsen} + 1/2\ A_{loop}$$

with A_{tsen} = internal gain from TXIN to TSEN = 40 dB.

In this relation, the maximum loop gain and the worst case sidetone are used. If it is prefered to give the transmit channel priority above the receive channel, the value of Rtsen has to be chosen smaller. For the opposite, the value of Rtsen has to be chosen larger. With respect to the calculated setting, Rtsen and Rrsen can be varied with plus and minus 1/2 * Aloop (in dB).

In appendix A, a method for determining the required Rtsen, based on the above calculation, is given.

The capacitors Ctsen and Crsen form first order high-pass filters respectively with Rtsen and Rrsen to reduce influence of low frequencies on the switching behavior. It is suggested to choose the capacitors Ctsen and Crsen such that the cut-off frequencies of the filters are similar.

When the calculated sensitivity setting is implemented, subjective tests with real telephone lines will be necessary to come to the optimal sensitivity setting.

Once Rrsen is determined, it would also be possible to determine Rtsen only by experiments. In this case, subjective tests with different line conditions (attenuation, impedance, length) have to be carried-out until the optimal sensitivity setting is found.

Ad 4. Determine timings

The timings which can be set are : signal envelope timing and noise envelope timing for both channels, switch-over timing and idling timing.

The signal envelope timing is set by the capacitors Ctenv and Crenv. Because of the logarithmic compression between TSEN and TENV respectively RSEN and RENV, the timing can be expressed in dB/ms. At room temperature, the following relation counts :

$$\text{Timing} \cong I / (3 * C) \quad \text{(in dB/ms)}$$

With I = charge or discharge current from pin TENV, RENV, TNOI, RNOI

C = timing capacitor Ctenv, Crenv, Ctnoi, Crnoi

With the advisable signal envelope timing capacitors Ctenv and Crenv of 470 nF, the maximum attack-timing of the signal envelopes will be around 85 dB/ms (I=120 µA). This is enough to track normal speech. The release timing will be 0.7 dB/ms (I=1 µA). This is enough to smoothen the signal envelope and to eliminate the influence of room echoes on the switching behavior.

With the advisable noise envelope timing capacitors Ctnoi and Crnoi of 4.7 µF, the attack timing of the noise envelopes will be 0.07 dB/ms (I=1 µA). This is small enough to track background noise and not to be influenced by speech bursts. The maximum release timing will be 8.5 dB/ms (I=120 µA). This is enough to track the signal envelope during release because the signal envelope release timing is 0.7 dB/ms which is a factor smaller. It is advised to choose the signal envelope timing and the noise envelope timing of both channels equal for optimum operation of the duplex controller.

The switch-over timing is determined by the value of the switch-over capacitor Cswt. The idling timing is determined by the combination of Cswt and the idling resistor Ridt.

The output current of pin SWT is Iswt, a voltage difference over Cswt can be obtained according to :

$$\delta Vswt/t = Iswt / Cswt \ (mV/ms).$$

With the advised value of 220 nF for Cswt, the obtained voltage difference is 45 mV/ms. The switch-over time is dependent on the voltage difference which has to be generated on pin SWT. Suppose the set is in full Tx-mode, then the voltage on SWT will be V(IDT)-400 mV, see fig.3.4.4. To reach Rx-mode a voltage difference of 580 mV must be generated to end up a voltage of V(IDT)+180 mV. So in this case the switch-over time will be 13 ms. When the set is in Ix-mode, the voltage on SWT equals the voltage on IDT, in that case switching to Tx-mode or to Rx-mode requires a voltage generation of only 180 mV and they will be reached in 4ms.

The idling timing is determined by an RC time constant. It is supposed that Ix-mode is reached when a time (tidt) is elapsed:

$$tidt = 4 * Ridt * Cswt$$

With the advised value for Ridt of 2.2 MΩ, an idling time of around 2 seconds is obtained. To have a clearly determined idling timing, it is advised not to use a capacitor with a high leakage current.

When the calculated timing settings are implemented, subjective tests with real telephone lines will be necessary to be sure that the optimal timings have been set.

Miscellaneous

When a handsfree telephone set is used at one end of the line and a conventional set at the other end,the user of the conventional set may think that the line is cut when the handsfree set stays in receive mode while no signal on the line is present. This is avoided when the handsfree set switches over to idle mode. This mode is incorporated in the TEA1095 and is placed exactly at mid attenuation between transmit and receive mode. When it is desired to have an idle mode which is closer to transmit than receive mode, the circuit of fig.3.4.5 can be applied.

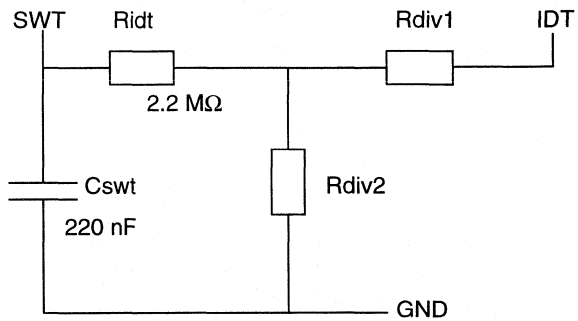


Fig.3.4.5 Circuit for shifting the idle mode

With the circuit of fig.3.4.5, in idle mode, the voltage on SWT will not go to the voltage on IDT but to the voltage on IDT minus the voltage drop over Rdiv1. The voltage drop over Rdiv1 determines the shift of the idle mode (in dB). This shift can be read from fig.3.4.4 , when the voltage drop over Rdiv1 is taken as the X-axis value. The voltage on IDT is approximately 1.2 V, so with for instance Rdiv1 = 33 kΩ and Rdiv2 = 1 MΩ, the shift will be about 10 dB. It is advised not to choose Rdiv2 lower than 1Mohms inorder to limit the current drawn from IDT. By connecting Rdiv2 to VBB instead of GND, the idle mode is shifted towards the receive mode.

In noisy environments, like offices, a handsfree set can show an unsteady behavior in idle mode (unwanted switching over from Ix to Tx-mode). In the TEA1095, this unsteady behavior is reduced by the implemented speech/noise threshold of 4.3 dB. However, when a larger threshold is required, this can be achieved by connecting a resistor Rtnoi in series with Ctnoi.

When there is only noise present at the input of the envelope detector, the voltages on pins TENV and TNOI are equal. When suddenly, a signal is present, the level on TENV will increase. Without Rtnoi, the voltage on TNOI will increase only slowly because of the charging current of 1 µA. When a resistor Rtnoi is placed in serie with Ctnoi, under the same conditions, this 1 µA current will cause a voltage jump on TNOI. This jump determines the shift of the speech /noise threshold. As depicted in fig.3.4.1, at room temperature, the 4.3 dB threshold equals 13 mV. A resistor Rtnoi in series with Ctnoi will add an extra voltage to this threshold of 1 µA * Rtnoi. When for instance, a resistor of 10 kΩ is chosen for Rtnoi, the speech/noise is increased to 23 mV which is equal to 7.6 dB at room temperature. The new speech/noise threshold is slightly dependent on temperature and on the spread of the internal current source and therefore less accurate than the internal 4.3 dB. It is advised not to use a resistor larger than 15 kΩ.

4. APPLICATION COOKBOOK

In this chapter, the procedure for making a basic application with a speech and listening-in IC TEA1096 and the handsfree duplex controller TEA1095 will be given. With the help of fig. C1 in appendix, the design flow is given as a number of steps which should be made. As far as possible for every step, the components involved and their influence on every step are given. The preferred values are given between brackets.

The application of fig. C1 is a basic application of the TEA1095 voice switched speakerphone IC with the TEA1096 speech and listening-in circuit.

As can be seen in fig. C1, only a few components have a fixed value. All other values will follow from the cookbook of fig.4.1.

Step	Adjustment
DC setting :	
Adjust the DC setting of the TEA1096 to the local PTT requirements.	
Voltage LN-VEE	
DC slope	Refer to [4] and/or to [12] (N° : ETT94001)
Supply point VCC	
Supply point VBB	
Artificial inductor	
Impedance and sidetone :	
After setting the required set impedance, the sidetone has to be optimized using the two sidetone netwoks in order to minimize the loop gain in all line conditions. AGC can be adjusted at that step.	
Set active impedance	Refer to [4] and/or to [12] (N° : ETT94001)
Sidetone	
AGC	
TEA1096 transmit and receive gains	
Transmit gain	Total transmit and receive gains have to be siplitted between TEA1096 and TEA1095. It is suggested to leave 15dB of transmit gain for the TEA1095 and to adjust the receive gain between LN and QRP at -3 dB. Ctxo and MICP input impedance form a high-pass filter. A capacitor in parallel with the transmit gain resistor (between TEA1096 pins 17 and 11) form a low-pass filter. A resistor bridge can be inserted between TXOUT of TEA1095 and MICP of TEA1096.
Receive gain	A capacitor in parallel with the receive gain resistor (between TEA1096 pins 26 and 25) form a low-pass filter. For more details, refer to [4] and/or to [12] (N° : ETT94001)
TEA1095 microphone amplifier (see & 3.2):	
After the sensitivity and the curve of the microphone are adjusted, the gain can be adjusted to the desired value	
Microphone sensitivity	Rmic sets the sensitivity. Together with Rmf, Rmic provides the polarisation of the electret.
Frequency curve	Cmic with Rmic and the output impedance of the electret form a low-pass filter. Ctxin with the 20 kΩ input impedance at TXIN form a high-pass filter.
Transmit gain and stability	Rgatx sets the microphone amplifier gain : Atx=20*log(0.72*Rgatx/Rstab) Cgatx may be necessary for stability and forms a low-pass filter with Rgatx.

Step	Adjustment
TEA1096 loudspeaker amplifier :	
The gain is fixed at 35.5 dB , a high-pass filter can be made, the dynamic limiter timing can be chosen.	
Frequency curve	Crxo and/or capacitor in series with loudspeaker can form high-pass filters
Dynamic limiter timing	Capacitor at pin DLL.
TEA1095 receive channel (see & 3.3) :	
The gain of the receive pass and the curve can be adjusted. The volume control range can be chosen.	
Receive gain	Rgarx : the total receive gain of the set is equal to receive gain of the TEA1096 (-3 dB ?), the gain of the loudspeaker amplifier (35.5 dB) and the gain set with Rgarx.
Receive curve	Crxi with the input impedance of 20 kΩ at pin RXI form a high-pass filter (a cut-off frequency between 100 and 200 Hz is advised),
Volume control	Cgarx in parallel with Rgarx forms a low-pass filter. A linear potentiometer of 10 kΩ is suggested (3 dB for each 950 Ω).
TEA1095 Duplex controller (see & 3.4) :	
When all gains are adjusted, the switching range can be determined. Then the dial tone detector level followed by the sensitivities can be set. Finally the timings of the envelopes and the switching are adjusted.	
Switching range	Loop gain : Aloop=Atx1095+Atx1096+Ast+Arx1096+Arx1095+Als1096+Aac-Asw < 0dB Choose Asw with safety margin Adjust Rswr : Asw=20log(Rswr/Rstab) with Rstab fixed at 3.65kΩ
Dial tone detector	Rrsen : Vdialtone=4.2 μA*Rsen
Sensitivities	Rtsen for balanced sensitivities between Tx and Rx Ctsen form a high-pass filter with Rtsen Crsen form a high-pass filter with Rrsen
Signal envelopes	Ctenv (0.47 μF), Crenv (0.47 μF) : maximum attack : 120 μ/(3*Cenv) (dB/ms), release : 1 μ/(3*Cenv) (dB/ms)
Noise envelopes	Ctnoi (4.7 μF), Crnoi (4.7 μF) : attack : 1 μ/(3*Ctnoi) (dB/ms), maximum release : 120 μ/(3*Ctnoi) (dB/ms)
Switch-over timing	Cswt (220 nF) : δVswt/t=10μ/Cswt (mV/ms)
Ix-mode timing	Ridt (2.2 MΩ) : time constant=4*Ridt*Cswt

Fig. 4.1 Steps in the design flow of the TEA1095 with TEA1096

5. APPLICATION EXAMPLE

In this chapter, a basic application example of the TEA1095 with the TEA1096 is depicted. Only the essential elements are given, for instance no bridge, no protection, no ringer, no line interruptor are included.

Fig. C2 gives the basic handsfree application of the TEA1095 together with the speech and listening-in circuit TEA1096. This application doesn't include handset telephony (which would have to be added by means of analog switches) but only basic handsfree telephony.

- **DC setting** : nominal DC characteristic and nominal V_{BB} of 3.6 V are chosen.

- **Impedance and sidetone** : the impedance is a complex one (220 Ω, 825 Ω//115 nF). A standard 600 Ω impedance would save six components.

- **TEA1096 transmit and receive gains** : the transmit gain of TEA1096 is set at 30.5dB by means of a resistor bridge (22 kΩ, 7.5 kΩ at microphone input combined with an internal gain of 43 dB set by 32.5 kΩ). The cut-off frequency of the high-pass filter is set at 110 Hz by 2*100 nF in series, the cut-off frequency of the low-pass filter is set at 7.2 kHz by 680 pF//32.5 kΩ.

The receive gain of TEA1096 is set at -3 dB by 82.5 kΩ. The cut-off frequency of the low-pass filter is set at 4.1 kHz by 470 pF//82.5 kΩ.

-**TEA1095 microphone amplifier** : the sensitivity of the electret microphone is set by Rmic=1.5 kΩ. The microphone power supply is filtered by Rmf, Cmf with a cut-off frequency of 16Hz. An electrical low-pass filter is provided with Cmic, in combination with the effect of the cabinet and the self curve of the electret, it adjusts the high frequency part of the transmit curve. A high-pass filter is formed with Ctxin and the 20 kΩ input impedance at TXIN, its cut-off frequency is set at 530 Hz (a higher cut-off frequency may be necessary to better minimize the room echo and/or to better compensate the line attenuation).

The gain of the microphone channel is set at 15.5 dB by Rgatx=30.1 kΩ, a low-pass filter with Cgatx=2.2 nF would provide a cut-off frequency of 2.4 kHz.

- **Loudspeaker amplifier** : nominal loudspeaker amplifier application is made (gain of 35.5 dB).

- **TEA1095 receive channel** : the gain of the receive path of the TEA1095 is set at -7 dB by Rgarx=3.65 kΩ (the total receive gain of the set is : 35.5 - 3 - 7 = 25.5 dB). A high-pass filter with a cut-off frequency of 120 Hz is formed by Crxin=68nF and the input impedance of 20 kΩ at RXIN. A low-pass filter with Cgarx=15 nF would provide a cut-off frequency of 2.9 kHz for the adjustment of the loudspeaker curve.

A 10kΩ linear potentiometer provides a volume control range of about 31dB.

- **Duplex controller** : after optimized acoustic adaptation (**reduction of acoustic coupling between loudspeaker and microphone** and good sidetone adaptation) the switching range is set at 40dB by Rswr=365k, including safety margin.

With Rrsen=10 kΩ, the dial tone detector level is set at 42 mV which means 60 mVrms on line.

With Crsen=100 nF, the cut-off frequency of the high-pass filter is 160 Hz.

Rtsen and Ctsen respectively equal Rrsen and Crsen in order to balance transmit and receive sensitivities.

With Ctenv and Crenv=0.47 µF, the max. attack time of the signal envelopes is set at 85 dB/ms.

With Ctnoi and Crnoi=4.7 µF, the max. attack time of the noise envelopes is set at 0.07 dB/ms.

The switch-over timing is nominally set by Cswt=220 nF and the idling timing by Ridt=2.2 MΩ.

Due to its large flexibility (range of adjustments and architecture), the TEA1095 can be implemented in a lot of environments, offering handsfree function with various speech interfaces and loudspeaker amplifiers, with or without external supply.

6. ELECTROMAGNETIC COMPATIBILITY

As no common international specification exists for RFI immunity, and as different assembly methods may lead to different solutions, only some advices can be provided.

It is advisable to take care of the impedance of the GND, the smallest is always the best. Even if it is required to separate low level microphone signals on GNDTX from high level signals (loudspeaker or others), GND and GNDTX traces must be as wide as possible.

Also, the connection of Rstab, Rswr, Rgatx and Rgarx has to be done with very short traces (specially STAB input which sets all the gains must be very immune).

VOL and TXI inputs may also be sensitive (RF signals entering these pins would be amplified). Rvol can be connected with short traces if possible or VOL input may be lightly decoupled by a capacitor to GND. Care has to be taken with the lay-out of the microphone amplifier, which is also helpfull for the noise, providing a good decoupling to GNDTX. A low-pass RC filter may be added at the input of the amplifier.

It is not allowed to put a capacitor directly between STAB and GND, only an RC network can be implemented if it helps (365 Ω, 4.7 nF).

RXIN input may also be decoupled to GND.

A low impedance capacitor in parallel with the electrolythic one between VBB and GND may help.

7. REFERENCES

[1] TEA1095 Voice Switched Speakerphone IC
Device specification

[2] Philips Semiconductors
SEMICONDUCTORS FOR TELECOM SYSTEMS - IC03 -

[3] TEA1094 Handsfree IC
Device specification

[4] TEA1096 / TEA1096A Line interface and Listening-in ICs
Device specification

[5] TEA1081 Supply circuit with power-down for telephone set peripherals
Device specification

[6] TEA1083 / TEA1083A Call progress monitor for line-powered telephone set
Device specification

[7] TEA1085 / TEA1085A Listening-in circuit for line-powered telephone set
Device specification

[8] TEA1112 / TEA1112A / TEA1113 Low voltage versatile telephone transmission circuits with dialler interface
Device specifications

[9] TEA1062 / TEA1062A Low voltage versatile telephone transmission circuits with dialler interface
Device specification

[10] TEA1064A / TEA1064B Low voltage versatile telephone transmission circuits with dialler interface and level dynamic limiting
Device specification

[11] Application of the TEA1094 handsfree circuit (ETT/AN94004)

[12] Application of the TEA1096 transmission and listening-in circuit (ETT94001)

[13] Measures to meet EMC requirements for TEA1060-family speech transmission circuits (ETT89016)

[14] Application of the speech transmission circuit TEA1062 (ETT89008)

[15] Application of the versatile speech/transmission circuit TEA1064 in full electronic telephone sets (ETT89009)

[16] Philips Semiconductors
Wirebound telecom
APPLICATIONS HANDBOOK

APPENDIX A MEASUREMENT SETUP

This appendix describes how the loop gain and the sensitivity setting can be measured. These measurements provide a base for obtaining of the final values which, however, can only be reached by performing subjective tests.

For determining the loop gain, the worst case for both acoustical coupling and sidetone must be considered. This can be done with the measurement setup of fig. A.1.

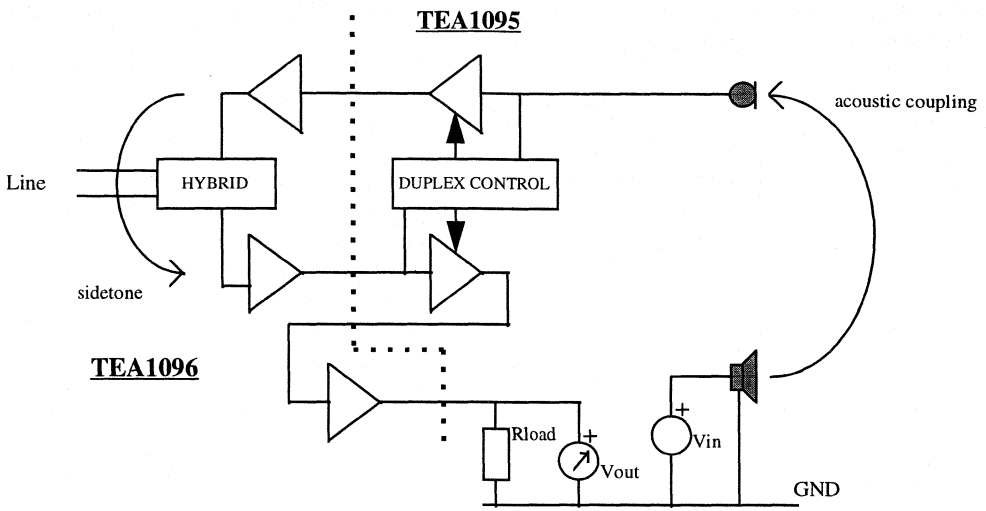


Fig. A. 1 Setup for loop gain measurement

The loudspeaker is disconnected from the set and an electrical signal is applied to it. The acoustical signal coming from the loudspeaker is coupled to the microphone (Aac), transmitted to the line (Atx1095 + Atx1096), returns via sidetone (Ast) and is amplified again to the loudspeaker output of the TEA1096 (Arx1096 + Arx1095 + Als1096). The output is loaded with a loudspeaker equivalent impedance (Rload), it has to be checked that the TEA1096 loudspeaker amplifier is not saturated and that its gain is not reduced by the dynamic limiter. The total gain of this loop is reduced with the switching range (Asw).

The gain from the loudspeaker connection (Vin) to the loudspeaker amplifier output (Vout) is the loop gain (Aloop), given as:

$$20 * \log (Vout / Vin) = Aloop$$

$$Aloop = Aac + Atx1095 + Atx1096 + Ast + Arx1096 + Arx1095 + Als1096 - Asw$$

This measurement has to be carried-out with a Vin level avoiding saturation of the loudspeaker amplifier (start with 100 mVrms) in the frequency range 200 Hz to 5000 Hz (100 to10000 Hz for high quality aparatus).

From the curve obtained, the maximum gain (<0 dB) indicates the gain margin.

Sidetone curve changes with line impedance, so, the Aloop curve will change in the same way. It is advisable to double-check with different line conditions (impedance and length) that the identified worst line condition is really the worst all over the frequency range.

Moving around the set also modifies acoustic coupling, so, it is advised to proceed as for sidetone.

The measurement combining both worst case conditions of sidetone and acoustical coupling gives the worst case loop gain and thus the gain margin.

All transmit and receive gains and curves are supposed to be set, the value of the switching range however, can only be finalized after the measurement. Therefore, during the measurement, the switching range must be set to a preliminary value. An advised preliminary value for measurement is 40 dB.

When the correct switching range is set, the sensitivity settings can be determined.

Rrsen is determined to get the correct tone detector level.

For determining the sensitivity, calculations can be done as described in &3.4.4. It is also possible measuring the correct sensitivity setting with measurement setup of fig. A. 2.

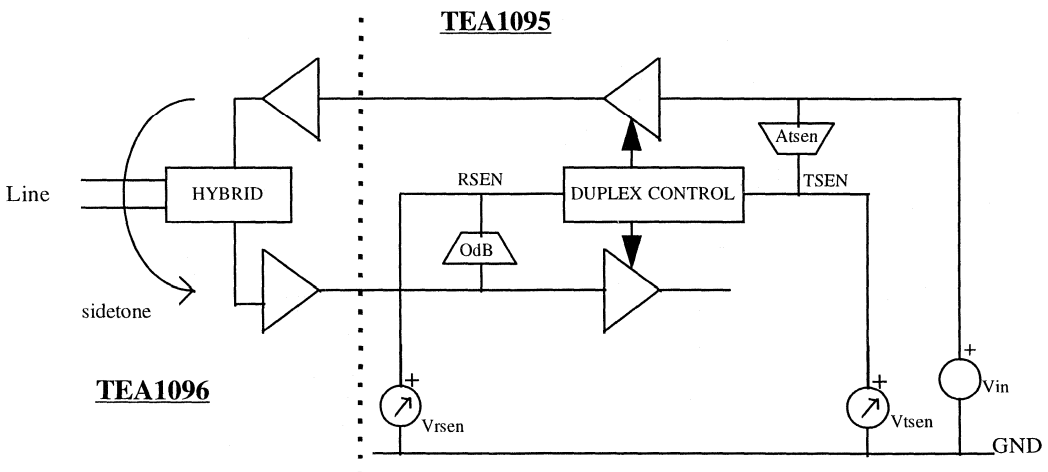


Fig. A. 2 Simplified measurement setup for determining sensitivity

Both the loudspeaker and microphone are disconnected from the set. An input signal (Vin) of 1 mVrms is applied to the microphone input. This signal is amplified to pin TSEN (Atsen), it is also transmitted to the line, returns via sidetone, is amplified by the TEA1096 to the TEA1095 pin RXIN and buffered to pin RSEN. The ratio of the signal on pin TSEN (Vtsen) and RSEN (Vrsen) is given as :

$$20 * \log (Vtsen/Vrsen) = Atsen - Atx1095 - Atx1096 - Ast - Arx1096$$

This measurement has to be done in nominal line and environment conditions in the frequency range 300 Hz to 3400 Hz. The TEA1095 must be forced in Tx-mode by making pin MUTERX high, the receive channel is muted but Vrsen is not affected.

Out of the measured ratio of Vtsen and Vrsen it follows :

$$20 * \log (Rtsen / Rrsen) = 20 * \log (Vtsen / Vrsen) + Aloop / 2 \qquad (\text{see } \&3.4.4, Ad.3)$$

Both the ratio of Vtsen and Vrsen and Aloop are frequency dependent, so the optimal value of Rtsen would be frequency dependent. However, this can be simplified by using the lowest value of 20*log(Vtsen/Vrsen) and the highest value of Aloop to obtain the correct Rtsen.

The value of Rtsen found is a starting point for obtaining the final value which can only be reached by subjective tests with real telephone conditions.

APPENDIX B LIST OF ABBREVIATIONS AND DEFINITIONS

Aac	Electro-acoustic coupling (electrically measured)
AGC	Automatic line loss compensation of the TEA1096
Aloop	Loop gain of a handsfree telephone set
Als1096	TEA1096 loudspeaker amplifier gain
Arx1095	Gain of the receive path of TEA1095
Arx1096	Receive gain of TEA1096
Ast	Sidetone gain
Asw	Switching range
Atsen	Gain from TXIN to TSEN of 40dB
Atx1095	Gain of the transmit path of TEA1095
Atx1096	Transmit gain of the TEA1096
Cgarx	Capacitor setting receive path amplifier low-pass filter
Cgatx	Capacitor setting microphone amplifier low-pass filter
Cmf	Microphone supply filter capacitor
Cmic	Microphone low-pass filter capacitor
Crenv	Capacitor determining the receive signal envelope
Crnoi	Capacitor determining the receive noise envelope
Crsen	DC blocking capacitor of receive sensitivity setting
Crxi	Receive input capacitor
Crxo	Receive output capacitor
Cswt	Switch-over timing capacitor
Ctenv	Capacitor determining the transmit signal envelope
Ctnoi	Capacitor determining the transmit noise envelope
Ctsen	DC blocking capacitor of transmit sensitivity setting
Ctxin	Microphone amplifier input capacitor
Ctxo	Transmit output capacitor
dBmp	dBm psophometrically weighted (0dBmp=1mW)
δVswt	Voltage difference on SWT
GARX	Receive gain adjustment pin
GATX	Transmit gain adjustment pin
GND	Ground reference pin

GNDTX	Ground reference pin for microphone signals
IDT	Idle-mode timing adjustment pin
Iswt	Output current through pin SWT (from logic)
Ix-mode	Idle mode
LN	Positive line terminal of TEA1096 or TEA106x
LSI	Loudspeaker amplifier input of TEA1096
MICP,MICM	Microphone input of TEA1096
MOSFET	Meta Oxide Field Effect Transistor
MUTERX	Receive channel mute
MUTETX	Transmit channel mute
NC	not connected
PD	Power-down input pin (reduced power consumption)
PTAT	Proportional to absolute temperature
PTT	Public telephone company
QRP	Earphone amplifier output of TEA1096
RENV	Receive signal envelope timing adjustment pin
RFI	Radio frequency interference
Rgarx	Resistor setting receive path amplifier gain
Rgatx	Resistor setting transmit path amplifier gain
Ridt	Resistor setting Ix-mode timing
Rload	Loudspeaker equivalent load resistor
Rmf	Microphone supply filter resistor
Rmic	Resistor setting microphone sensitivity
RNOI	Receive noise envelope timing adjustment pin
Rrsen	Resistor setting sensitivity of the receive envelopes
RSEN	Receive signal envelope sensitivity adjustment pin
Rslpe	Resistor setting slope of the DC characteristic of TEA1096
Rstab	Resistor setting an internally used PTAT current
Rswr	Resistor setting switching range
Rtnoi	Resistor increasing microphone speech/noise threshold
Rtsen	Resistor setting sensitivity of the transmit envelopes
Rvol	Volume control potentiometer
RXIN	Receive path input
RXOUT	Receive path output

Rx-mode	Receive mode
SLPE	DC slope pin of TEA1096 or TEA106x
STAB	Reference current pin
SWR	Switching range adjustment pin
SWT	Switch-over timing adjustment pin
TENV	Transmit signal envelope timing adjustment pin
Tidt	Idle mode timing
TNOI	Transmit noise envelope timing adjustment pin
TSEN	Transmit signal envelope sensitivity adjustment pin
TXIN	Microphone amplifier input
TXOUT	Transmit path output
Tx-mode	Transmit mode
V_{BB}	Positive supply input of TEA1095
Vdt, Vdialtone	Dial tone detector level
VEE	Reference pin on TEA1096
VOL	Volume adjustment pin

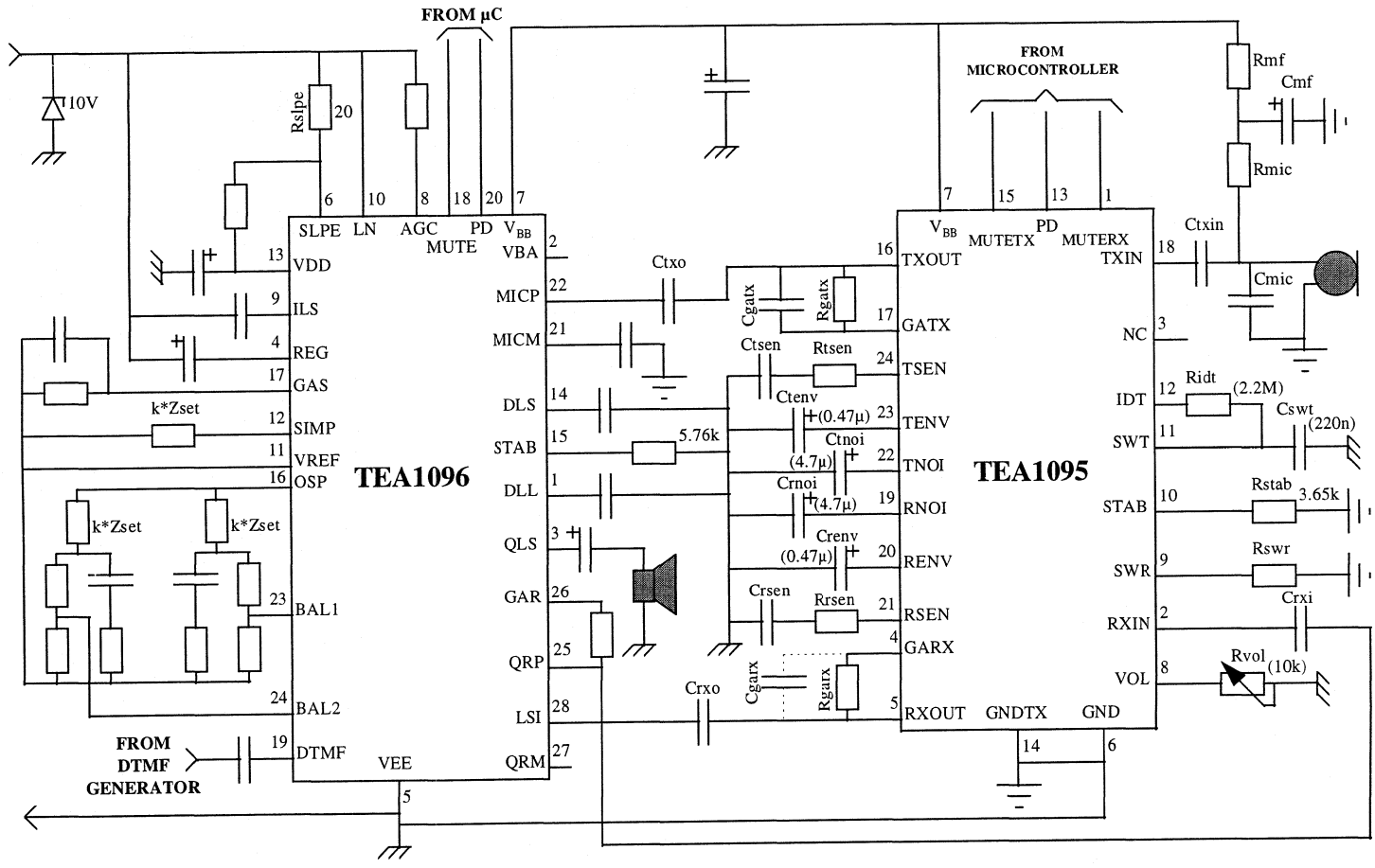


Fig. C1 Basic application of TEA1095 with TEA1096

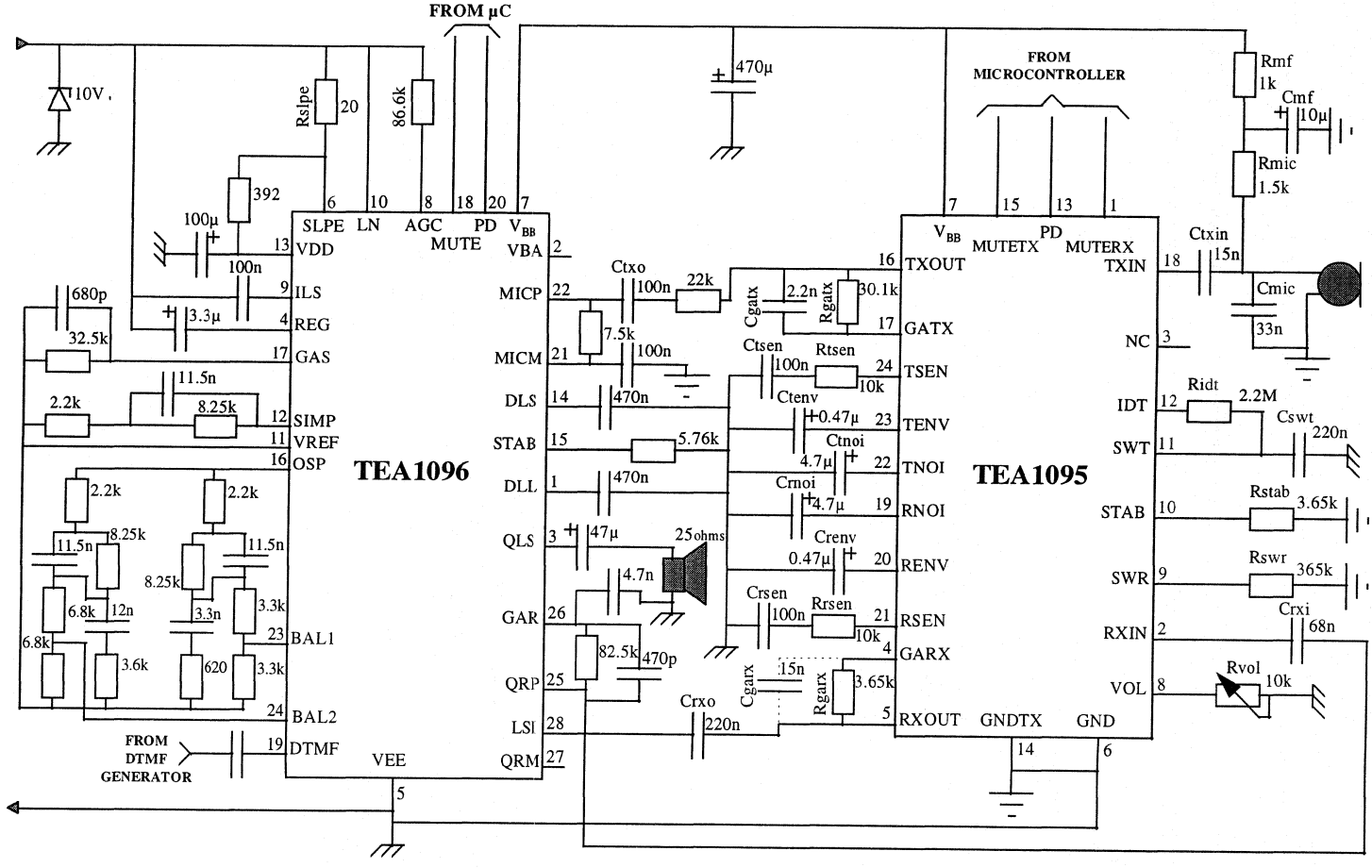


Fig. C2 Basic application of TEA1095 with TEA1096

Low power single/dual frequency synthesizers: UMA1017M/1018M/1019M(AM)/1020M(AM)

AN95102

Author: P. Hugues

UMA1018M and UMA1020M/UMA1020AM low power dual frequency synthesizers

UMA1017M and UMA1019M/UMA1019AM low power single frequency synthesizers

SUMMARY

This application note describes the UMA1018M and UMA1020M/UMA1020AM from Philips Semiconductors. They permit a low-voltage low-power single-chip solution to designing dual PLL frequency synthesizers. They are intended for use in digital or analogue wireless communications equipment. Typical applications include GSM, DECT and DCS1800.

Three low-voltage low-power solutions to single frequency synthesizers are also briefly described. The UMA1017M and UMA1019M/UMA1019AM are derivatives from UMA1018M and UMA1020M, respectively, and are hence closely related.

The overall performance of any PLL frequency synthesizer system is critically determined by the low pass filter used. Described in this report is a basic loop filter design method with worked examples and some measurement results.

1. INTRODUCTION TO UMA1018M DUAL SYNTHESIZER

1.1 General description

The UMA1018M [1] is a low power low voltage single chip solution to a dual frequency synthesizer used in radiocommunications. Designed in a BICMOS process, it operates from 2.7 (3 NiCd cells) to 5.5 V. The UMA1018M contains all the necessary elements with the exception of the VTCXO, VCO and loop filters to build two PLL frequency synthesizers.

It is intended that the principal synthesizer operates in the 50 to 1250 MHz range, and the auxiliary synthesizer will work between 20 and 300 MHz. For each synthesizer, fully programmable main and reference dividers are integrated on chip. The reference input FXTAL can operate from 5 to 40 MHz. Fast programming is possible via the three wire serial bus with clock speeds of up to 10 MHz.

The principal synthesizer phase detector drives a low current charge pump and a high current charge pump simultaneously. Maximum output current is 0.4 mA with the low current charge pump (pin CPP) and 3.2 mA with the other (pin CPPF). The auxiliary phase detector drives only one charge pump. The programmable charge pump currents are fixed by an external resistance R_{ext} at pin I_{SET}. Only passive loop filters are necessary.

To reduce crosstalk between different parts of the synthesizer, separate power supply and ground pins are provided to the analogue and digital sections.

Each synthesizer can be powered down independently to save current via software programming or hardwire pins AON / PON.

An on-chip 7 bit DAC allows adjustment of external functions, such as temperature compensation of the VTCXO, power amplifier control, etc.

1.2 FEATURES

- Dual frequency synthesizers
- Operating voltage range 2.7 to 5.5 V for battery powered operation
- Low current consumption, 10 mA typically at 5.5 V (two PLLs enabled)
- Integrated fully programmable main divider for each synthesizer
  - Principal: 512 to 131,071 up to 1.25 GHz input
  - Auxiliary: 64 to 16,383 up to 300 MHz input
- Independent fully programmable reference divider for each synthesizer
  - Principal: 8 to 2074 up to 2 MHz output
  - Auxiliary: 8 to 2047 up to 1 MHz output
- 3-wire serial bus (Data, Clock, Enable) for fast programming (f_{max} = 10 MHz)
- Independent hardwire and software power down modes for both synthesizers
- Simple passive loop filters
- Charge pump output current under bus control, with reference current I_{SET} set by an external reference resistor R_{ext}
- Programmable out-of-lock detector
- Integrated D-to-A converter
- Small SSOP-20 package

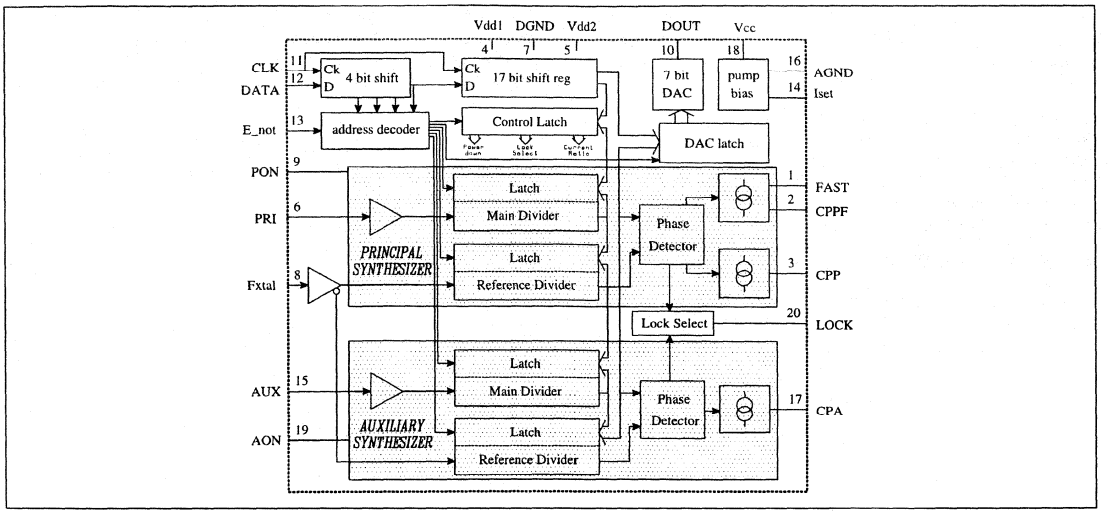


Figure 1–1. UMA1018M Block Diagram

1.3 Typical Application Architecture

UMA1018M integrated circuit is typically used in digital radiotelephone systems like GSM. It is designed to meet the requirements of these systems; low noise (residual and spurious), fast switching and low current consumption (at 5.5 V: 10 mA with both synthesizers ON and 36 µA with both synthesizers OFF).

Figure 1–1 demonstrates a typical application. UMA1018M is integrated on a dual superheterodyne architecture using two local oscillators.

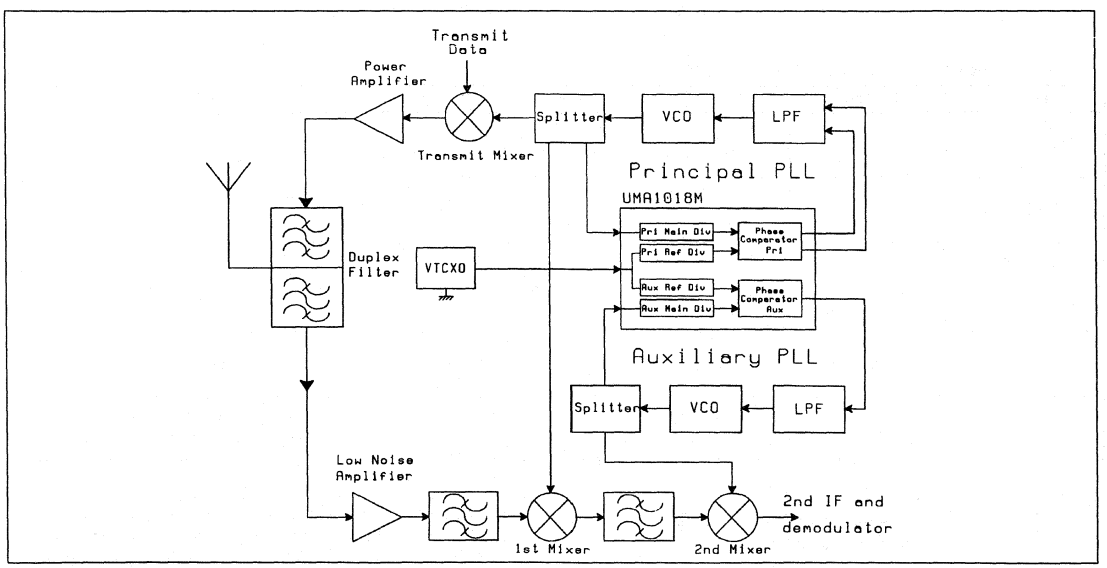


Figure 1–2. UMA1018M: Typical Application Block Diagram

Low power single/dual frequency synthesizers: UMA1017M/1018M/1019M(AM)/1020M(AM)

1.4 UMA1018M Family

To satisfy the need of the emerging digital communication systems, a family of synthesizer controls based around the UMA1018M has been developed.

1.4.1 UMA1020M/UMA1020AM Dual Synthesizers

UMA1020M [2] is used in 2 GHz applications, like PHP, DCS1800 or DECT. Its principal synthesizer operates from 1.7 to 2.4 GHz. It offers the same functions as the UMA1018M dual synthesizer including the 7-bit DAC. The UMA1020AM [3] principal synthesizer works from 1 to 1.7 GHz. It does not include the DAC.

1.4.2 UMA1017M and UMA1019M/UMA1019AM Single Synthesizers

The UMA1017M [4] and UMA1019M/UMA1019AM integrated circuits are derivatives from UMA1018M and UMA1020M, respectively with similar pinning. They contain the principal synthesizer only. UMA1017M operates from 50 to 1250 MHz, UMA1019M [5] from 1.7 to 2.4 GHz and UMA1019AM [6] from 1 to 1.7 GHz. Neither contains the auxiliary synthesizer or the DAC (see Figure 1–3).

In this application note, no extra mention will be made about UMA1020AM and the single synthesizers. All UMA1018M and UMA1020M principal synthesizer descriptions and results are valid for other circuits.

Table, overleaf, summarizes characteristics and typical applications of each synthesizer.

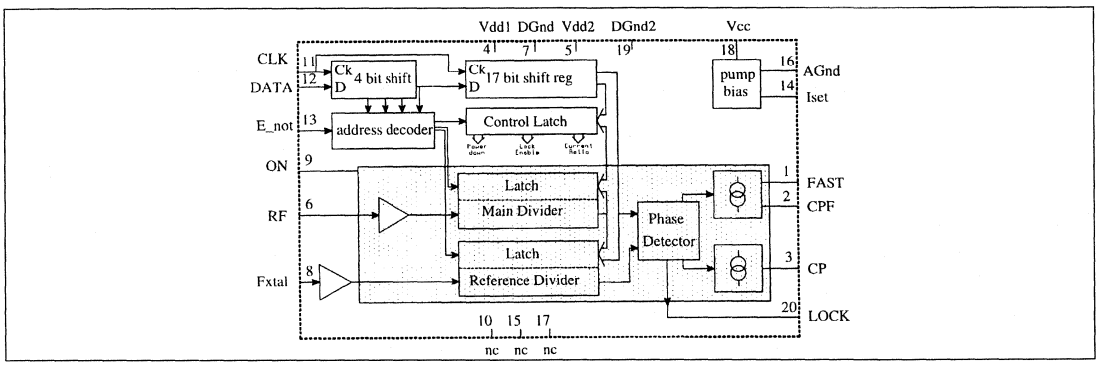


Figure 1–3. UMA1017M and UMA1019M/UMA1019AM Block Diagram

Table 1–1. Frequency Synthesizers Update

Part No.	Supply	Consumption	RF Input Frequency	Main Applications
UMA1017M	2.7 to 5.5 V	7.7 mA (5.5 V) 36 µA (PD)	Single 50 to 1250 MHz	CT2 digital cordless GSM digital cellular General purpose
UMA1018M	2.7 to 5.5 V	10 mA (5.5 V) 36 µA (PD)	Dual 50 to 1250 MHz (main) 20 to 300 MHz (aux)	Cellular systems like GSM Applications with UHF and VHF synthesizers
UMA1019AM	2.7 to 5.5 V	9.4 mA (5.5 V) 36 µA (PD)	Single 1 to 1.7 GHz	General purpose
UMA1019M	2.7 to 5.5 V	9.4 mA (5.5 V) 36 µA (PD)	Single 1.7 to 2.4 GHz	DECT Zero IF Cordless and wireless radios
UMA1020AM	2.7 to 5.5 V	12.1 mA (5.5 V) 36 µA (PD)	Dual 1 to 1.7 GHz (main) 20 to 300 MHz (aux)	General purpose
UMA1020M	2.7 to 5.5 V	12.1 mA (5.5 V) 36 µA (PD)	Dual 1.7 to 2.4 GHz (main) 20 to 300 MHz (aux)	Ideal for DECT superhet Digital cordless and wireless radios

2. FUNCTIONAL DESCRIPTION OF THE UMA1018M AND UMA1020M SYNTHESIZERS

The principle of the Phase Locked Loop (PLL) is illustrated in the PLL application block diagram (Figure 3–1).

A crystal (VTCXO) provides a reference frequency to the PLL. A phase detector drives a charge pump to send correction current pulses to a low pass filter. Current pulses are proportional to the difference in phase between the two phase detector input signals. The filter integrates the pulses giving a voltage which controls a Voltage Controlled Oscillator. VCO frequency and crystal frequency are divided down to a common comparison frequency to control the phase detector. The PLL is locked when the phase difference between input signals is maintained null.

2.1 Phase Detector and Charge Pump

2.1.1 Description

The principal and auxiliary phase detectors in the dual synthesizers are sensitive to both phase and frequency. They react to small phase differences between the main divider and reference divider inputs. The design responds to the full ±2∏ radians range of phase inputs.

The operating principle of the phase detectors is depicted in Figure 2–1. The comparison frequency f_{PC} at the inputs of the phase detector is typically the same as the radio system channel spacing. The phase detection is performed once each period of the comparison frequency.

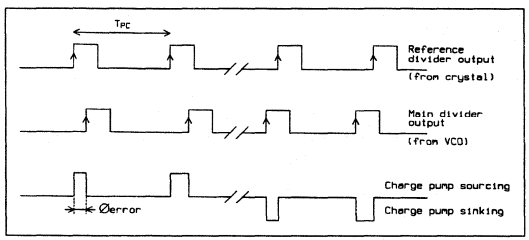


Figure 2–1. Principle of UMA1018M Phase Detectors

The charge pump outputs of the synthesizers are either sourcing, sinking or in high impedance. When the loop is locked, i.e., when the phase error at the input of the phase detector is zero, the charge pump output is in the high impedance state. When the loop is not locked, a phase error between the input signals is seen by the phase detector and the charge pump sends correction current pulses to the loop filter. If the output of the reference divider is leading, then the charge pump sources current pulses to increase the VCO control voltage and frequency. If the output of the reference divider is lagging, then the charge pump sinks current pulses to decrease the VCO control voltage and frequency. The pulse duration is proportional to the phase error. The sinking and sourcing pulses charge or discharge the capacitors in the loop filter, to a voltage required to bring the PLL back into lock.

The principal phase detector drives two charge pumps (pins CPP and CPPF). The charge pump current (the "height" of the positive or negative pulses in Figure 2.1) are switch–selectable by software. I_{CPPF} maximum output current is 3.2 mA, and that for CPP is 0.4 mA. The I_{CPPF}:I_{CPP} current ratio between the two charge pumps varies from 4 to 16. The reference current I_{SET} is set by an external resistance R_{ext} at pin I_{SET}, where a temperature independent voltage of 1.2 volts is generated. R_{ext} should be between 12 kΩ and 60 kΩ to give an I_{SET} between 100 µA and 20 µA. The auxiliary charge pump output current (pin CPA) is always 4 x I_{SET} the charge pump output currents can be programmed as shown below.

Table 2–1. Charge Pumps Current Ratio Relationships

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	I_{CPPF} : I_{CPP}
0	0	4 x I_{SET}	4 x I_{SET}	16 x I_{SET}	4 : 1
0	1	4 x I_{SET}	4 x I_{SET}	32 x I_{SET}	8 : 1
1	0	4 x I_{SET}	2 x I_{SET}	24 x I_{SET}	12 : 1
1	1	4 x I_{SET}	2 x I_{SET}	32 x I_{SET}	16 : 1

There are three ways to connect the charge pump outputs to the principal loop filter:

- Generally, the two charge pump outputs (CPP and CPPF) are connected together to the loop filter. The loop filter design is given in section 3.1.
- In some applications, the PLL is only closed during frequency switching, and opened during time slots where the transmitter (for open loop modulation) or the receiver must be active. In this case, the pin FAST allows opening the loop by disabling the principal fast charge pump. Only this pump should be connected to the loop filter. The principal charge pump (CPP output) is grounded.
- The third way is to have a dual time constant loop. The loop uses both charge pumps during frequency switching. The phase detector drives just the principal charge pump after the required frequency is obtained. The fast charge pump is disabled by the pin FAST. The loop filter design procedure is shown in section 3.3.

The following curves show measurements of sink and source currents of the auxiliary and principal fast charge pumps, as well as leakage currents (high impedance) of the different charge pumps.

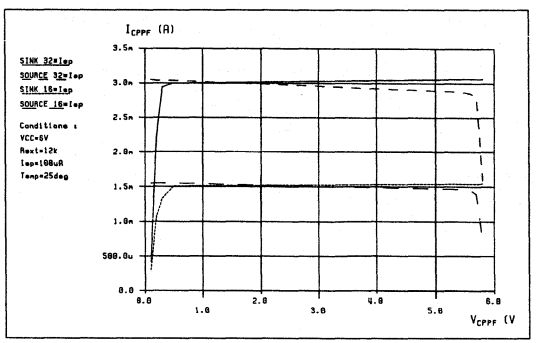


Figure 2–2. Principal Fast Charge Pump (CPPF) Output Current vs Voltage

Low power single/dual frequency synthesizers: UMA1017M/1018M/1019M(AM)/1020M(AM)

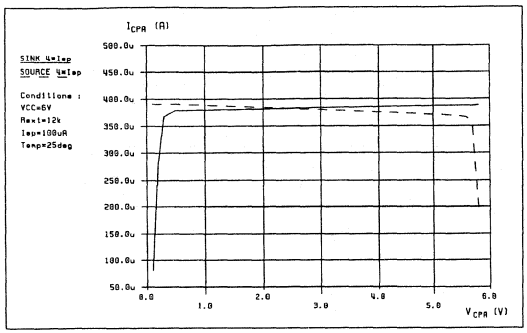


Figure 2–3. Auxiliary Charge Pump (CPA) Output Current vs Voltage

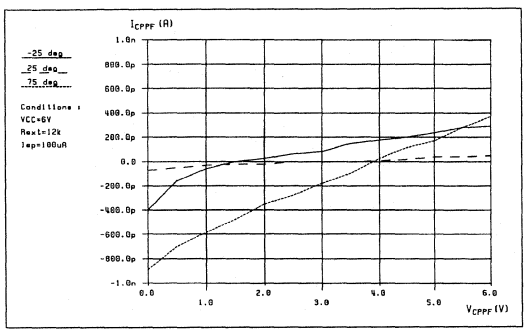


Figure 2–4. Principal Fast Charge Pump Leakage Current vs Voltage and Temperature

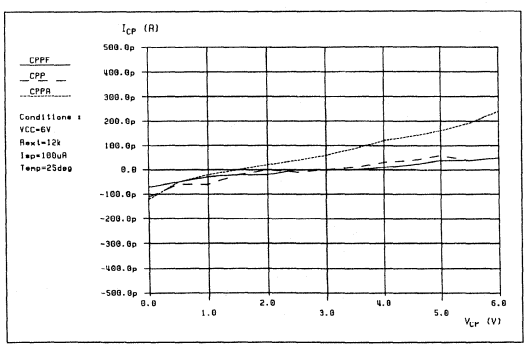


Figure 2–5. Leakage Current of UMA1018M Charge Pumps vs Voltage

2.1.2 Dynamic Characteristics

Two problems occur when the phase detector input signals' edges are very close together, i.e., when the phase error is zero (PLL is locked) or around zero (PLL has nearly settled after switching).

- The first problem is known as the dead–zone. It is due to the finite time the current sources take to switch on. The design of the UMA1018M and UMA1020M takes this into account by introducing a delay in the phase detector reset path. This gives the current sources enough time to respond.
- The second problem is that the charge pump gain is dependent on temperature and VCO control voltage. In this region, the gain varies as a function of the phase error. When the phase error increases outside the defined region, the charge pump gain becomes essentially independent and constant (see curve overleaf). This section is intended to show the linearity of the phase detectors and charge pumps.

Measurement method:

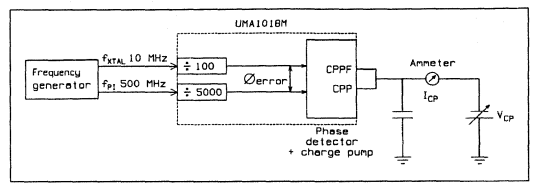
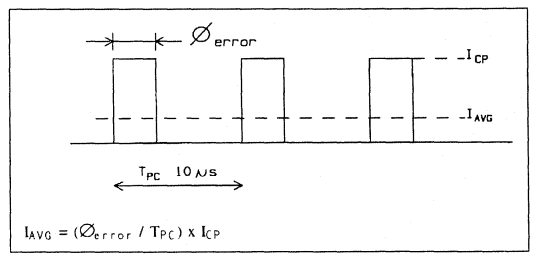
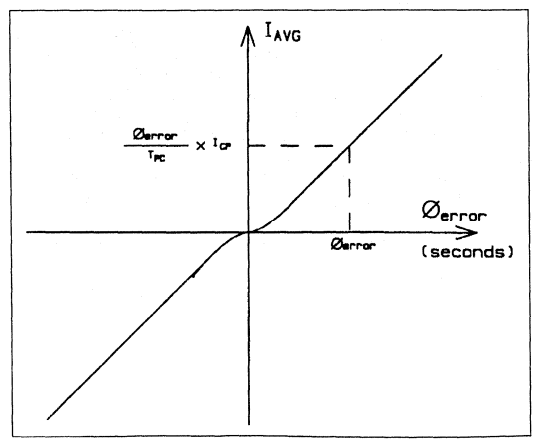


Figure 2–6. UMA1018M Principal Synthesizer Phase Detector Linearity Measurement

A frequency generator supplies the reference frequency f_{XTAL} and the main frequency f_{PI}. These frequencies are divided down to obtain a comparison frequency of 100 kHz. The generator allows controlling the phase of the 500 MHz signal with respect to the 10 MHz reference signal. The I_{AVG} phase detector current is measured as a function of the phase error:





Low power single/dual frequency synthesizers: UMA1017M/1018M/1019M(AM)/1020M(AM)

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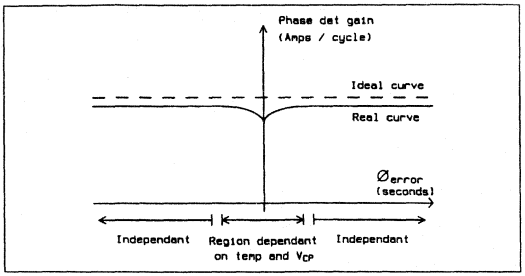
In order to find the real phase detector and charge pump gain for very small phase errors, we transform this curve by the equation:
Phase det gain (Amps/cycle) = $I_{AVG} \times (T_{PC}/\Phi error)$



Phase error values are taken in the region of ±10 ns. This is where the phase detector and the charge pump are less linear and where the loop spends most of its time, i.e., when it is locked or nearly locked. The following curves show measurements for source and sink gains around zero, showing the small departure from ideal. The jagged nature of the curves can partly be explained by very small values of I_{AVG}, and phase error giving granularity problems. In any case real charge pump gain for very small phase errors is mostly maintained within 25% of ideal value.

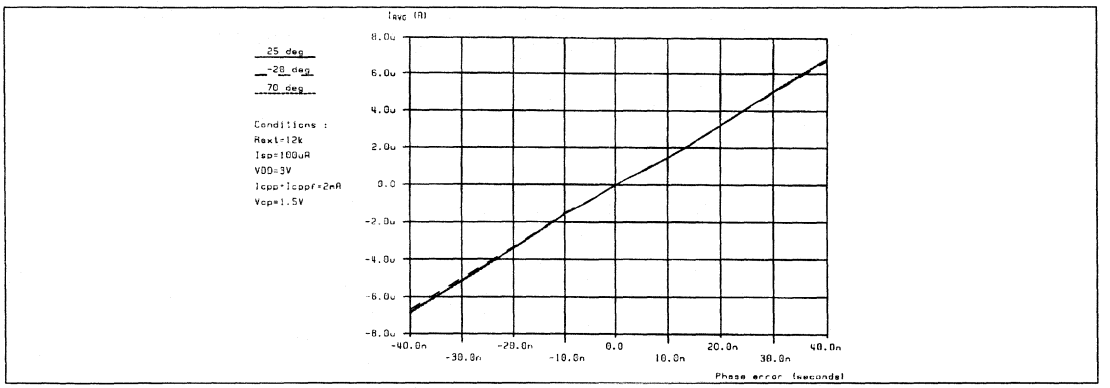


Figure 2–7. Principal Phase Detector and Charge Pump Characteristics vs Temperature

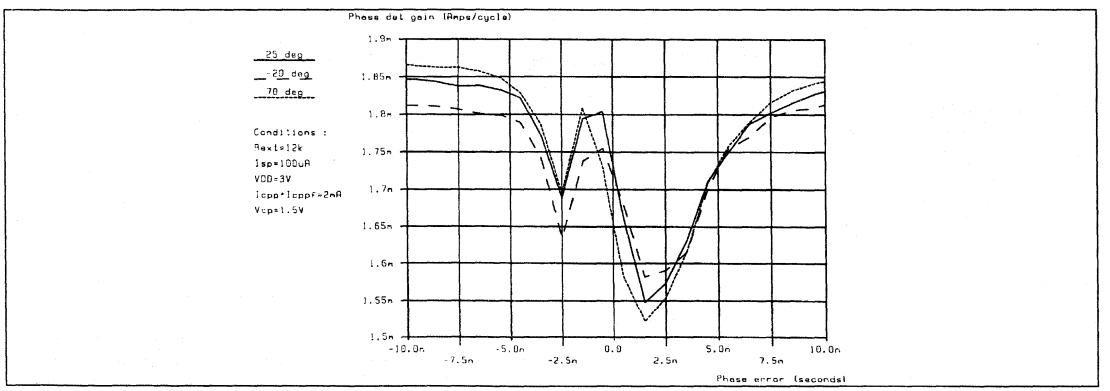


Figure 2–8. Principal Phase Detector and Charge Pump Gain vs Temperature

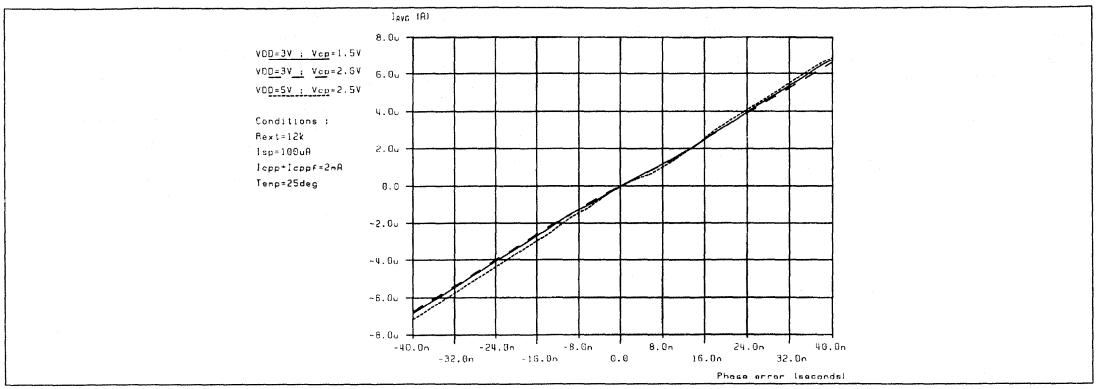


Figure 2–9. Principal Phase Detector and Charge Pump Characteristics vs Temperature

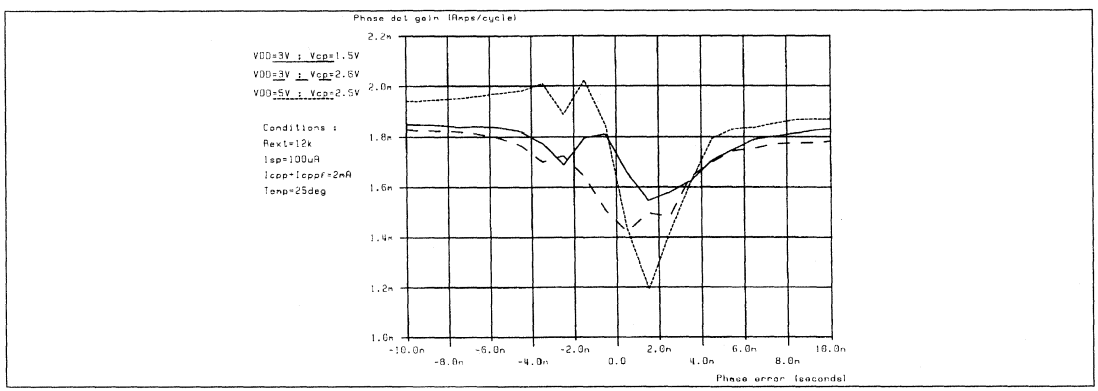


Figure 2–10. Principal Phase Detector and Charge Pump Gain vs V_{DD}

2.2 Programming

A simple 3-wire unidirectional serial bus is used to program the synthesizer. The three lines are DATA, CLK (Clock) and $\overline{E}$ (Enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active low. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive high. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power–down of either or both synthesizers.

After software or hardware power down is terminated, it is not necessary to program the device. Previous programming data is preserved during power down.

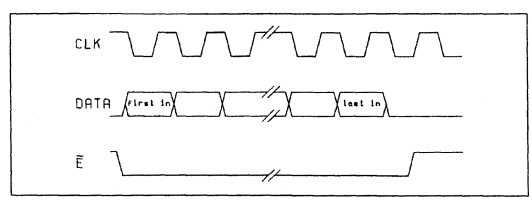


Figure 2–11. Serial Interface Timing Diagram

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are used for the address. The bits are decoded on the rising edge of $\overline{E}$. Two worked examples of programming are shown overleaf.

Special care has to be taken for correct programming when first applying power to the synthesizer. The E signal should be held LOW and only taken HIGH after having programmed an appropriate register on first powering up. If this condition is not achieved, it may result in loading of random data from the serial bus shift register (programming register) into one of the synthesizers data registers including the test register. It should be noted that the test register does not normally need to be programmed. However, if it is programmed, all bits in the data field should be set to 0. In case of random data being loaded into the test register, it is possible to program a frame of zeros, to return to normal operation.

2.2.1 UMA1018M Typical Programming Example

f_{XTAL} input frequency: 13 MHz
Principal synthesizer input frequency: 900 MHz (main divider ratio = PM = 4500)
Principal synthesizer comparison frequency: 200 kHz (main divider ratio = PR = 65)
Auxiliary synthesizer input frequency: 100 MHz (main divider ratio = AM = 1000)
Auxiliary synthesizer comparison frequency: 100 kHz (main divider ratio = AR = 130)
Both synthesizers ON (AON = PON = 1)
Out-of-lock indication from both synthesizer loops (OLP = OLA = 1)
Charge pump currents: I_{CPPF} = 32 x I_{SET}; I_{CPP} = 4 x I_{SET} (CR1 = 0 CR0 = 1)

Table 2–2. UMA1018M Register Data Allocations Expressed in Decimal and Hexidecimal

First In	Register Bit Allocation	Last In
dt16	Data Field dt0	Address
Test register (must be 0 if programmed)		0h
Control reg = 0 0001 101010110 0000b		1h
Principal main = 4500d = 01194h		4h
Principal reference = 65d = 00041h		5h
Auxiliary main = 1000d = 003E8h		6h
Auxiliary reference = 130d = 00082h		7h
DAC setting is 123d = 0007Bh		8h

Table 2–3. UMA1018M Register Data Allocations Expressed in Binary

First In (MSB)							Data Field								(LSB) Last In				Address			
0	0	0	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	1			
0	0	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	0	0		
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1		
0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	1	1	0		
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	1		
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	0	0	0		

2.2.2 UMA1020M Typical Programming Example

f_{XTAL} input frequency: 13.824 MHz
Principal synthesizer input frequency: 1890.432 MHz (main divider ratio = PM = 1094)
Principal synthesizer comparison frequency: 1728 kHz (main divider ratio = PR = 8)
Auxiliary synthesizer input frequency: 300.52 MHz (main divider ratio = AM – 3000)
Auxiliary synthesizer comparison frequency: 100.17 kHz (main divider ratio = AR = 138)
Both synthesizers ON (AOFF = POFF = 0)
Out-of-lock indication from both synthesizer loops (OLP = OLA = 1)
Charge pump currents : I_{CPPF} = 32 x I_{SET} ; I_{CPP} = 4 x I_{SET} (CR 1 = 0 CR0 = 1)

Table 2–4. UMA1020M Register Data Allocations Expressed in Decimal and Hexidecimal

First In	Register Bit Allocation	Last In
dt16	Data Field dt0	Address
Test register (must be 0 if programmed)		0h
Control reg = 0 0001 1010 0000 0000b		1h
Principal main = 1094d = 00446h		4h
Principal reference = 8d = 00008h		5h
Auxiliary main = 3000d = 00BB8h		6h
Auxiliary reference = 138d = 00082h		7h
DAC setting is 123d = 0007Bh		8h

Table 2–5. UMA1020M Register Data Allocations Expressed in Binary

First In (MSB)							Data Field								(LSB) Last In				Address			
0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1			
0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	1	0	0		
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1		
0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	1	1	0		
0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	1	1	1		
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	0	0	0		

2.2.3 UMA1018M and UMA1020M Preset Values

After the supply voltage is switched on, the preset values are normally:

Principal main divider ratio: 4500
Principal reference divider ratio: 65
Auxiliary main divider ratio: 8000
Auxiliary reference divider ratio: 1040
Control register: all 1 except out-of-lock
DAC register: all 0
Test register: all 0

2.2.4 Enable Pulse Width

With $\overline{E}$, a minimum inactive pulse width (T_W in the specification) is necessary before sending a new data burst. Due to internal synchronization, this minimum width depends on the input frequency to the main dividers and the reference divider. In the specification, this is indicated as 4 µs.

In fact, the minimum pulse width (T_W) can be smaller than 4 µs provided the following conditions are all satisfied:

Principal main divider input frequency > $(256/T_W)$
Auxiliary main divider input frequency > $(32/T_W)$
Reference dividers input frequency > $(3/T_W)$

Example: a pulse width of 500 ns can be used if

f_{PI} > 256 / 500 ns f_{PI} > 512MHz
f_{AI} > 32 / 500 ns f_{AI} > 64MHz
f_{XTAL} > 3 / 500 ns f_{XTAL} > 6MHz

2.3 Reference Divider

The input f_{XTAL} drives a preamplifier to provide the clock input for the reference dividers. The auxiliary reference divider is clocked on the opposite edge to the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at

different times. This minimizes the potential for interference between the charge pumps of each loop. Figure 2–12 shows the typical measured input sensitivity of the reference divider.

Some sensitivity to the reference input signal level on overall loop noise performance has been observed. Better performance is obtained for a higher level of f_{XTAL}.

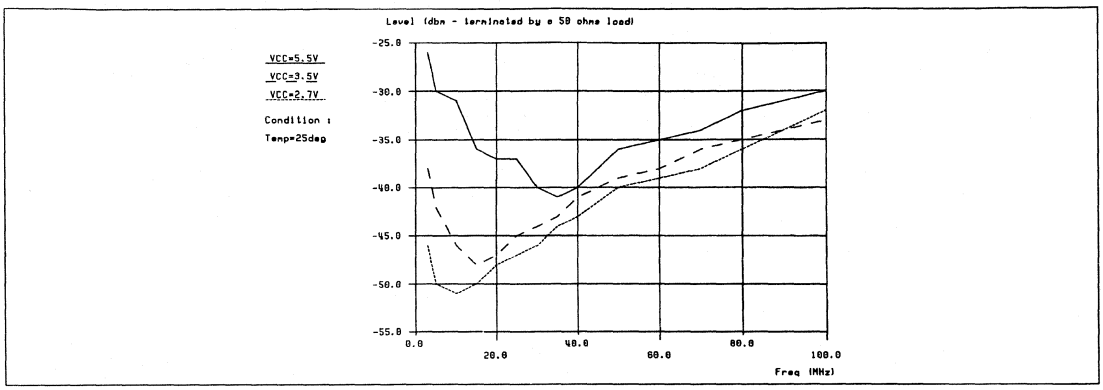


Figure 2–12. Reference Divider Input Sensitivity vs Frequency

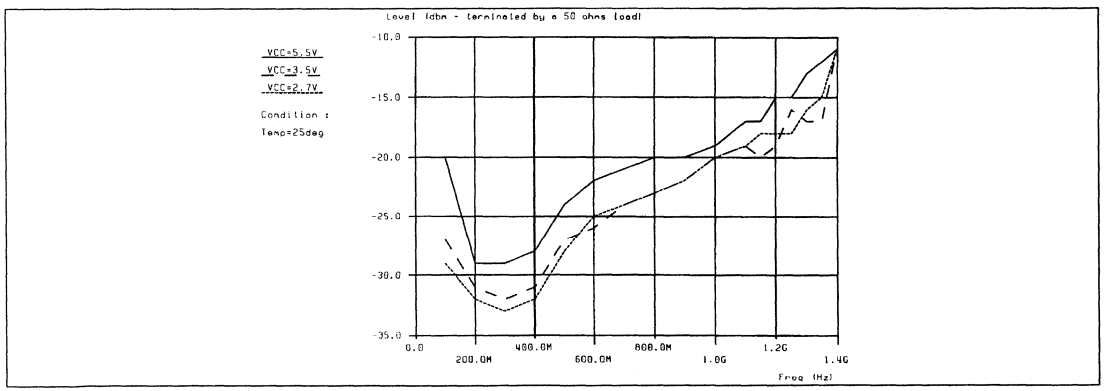


Figure 2–13. UMA1018M Principal Main Divider Input Sensitivity vs Frequency

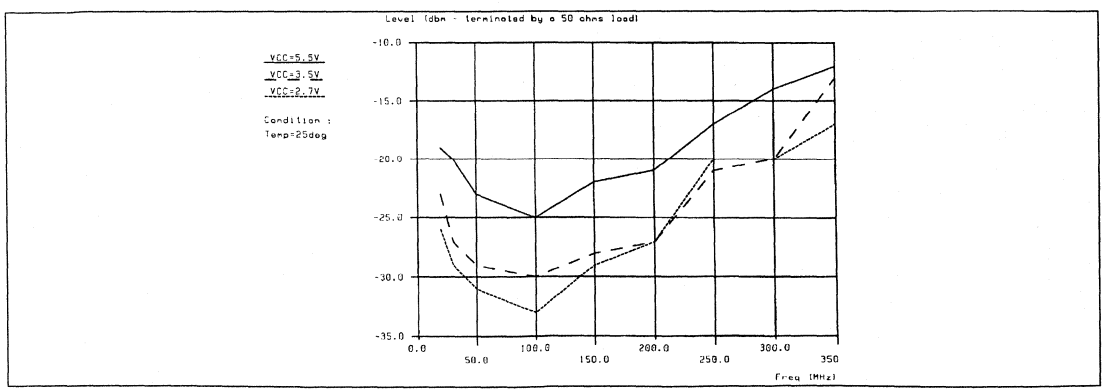


Figure 2–14. Auxiliary Main Divider Input Sensitivity vs Frequency

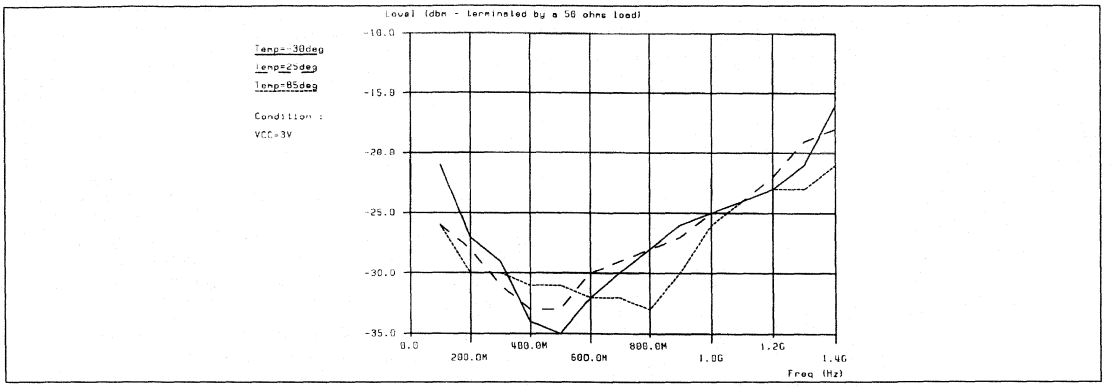


Figure 2–15. UMA1018M Principal Main Divider Input Sensitivity vs Frequency and Temperature

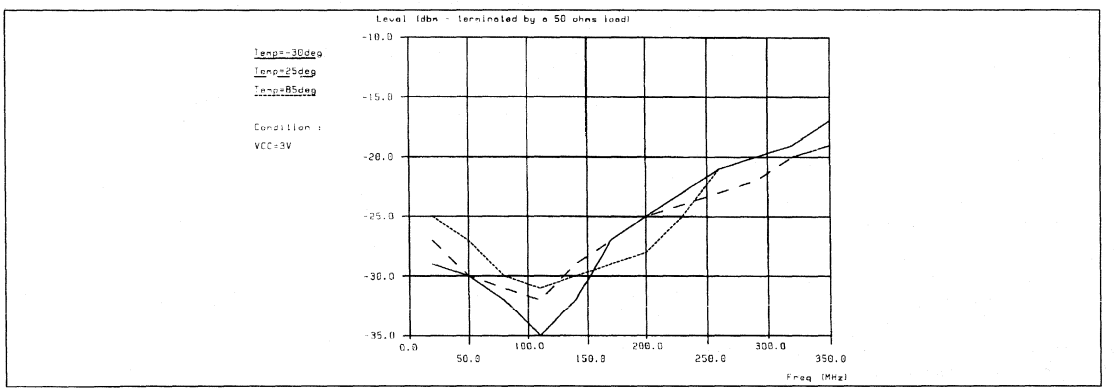


Figure 2–16. Auxiliary Main Divider Input Sensitivity vs Frequency and Temperature

2.4 Main Divider

The RF input drives a preamplifier to provide the clock for the main dividers. The preamplifier has a high input impedance, dominated by pin and pad capacitance. The high frequency sections of the main dividers are implemented using bipolar logic, while the slower sections use lower current CMOS logic. Figures 2–13 to 2–16 show the typical measured input sensitivity of the principal and auxiliary main dividers. Two samples were selected at random, with the device used for frequency versus temperature measurement showing better sensitivity.

2.5 Voltage and Ground Pins

Separate power and ground pins are provided to the analog and digital circuits. To reduce crosstalk between CMOS and bipolar parts, two independent pins supply the digital parts of the integrated circuit (V_{DD1} and V_{DD2}). V_{DD2} pin supplies the principal main divider bipolar section, V_{DD1} pin other digital sections. V_{DD1} and V_{DD2} could be shorted at the pins, however, separate decoupling will be better. The voltages at these pins should be similar.

The ground leads should be externally shorted together otherwise large currents may flow across the die, and damage it.

2.6 In lock Detector

There is a lock detector on-chip for each synthesizer. The lock condition of one, or both loops, can be indicated via an open-drain transistor which drives in-lock detect pin. A pull up resistor must be connected to the output. Whenever a phase difference occurs at the input of a phase detector this produces a pulse that can pass through to the out-of-lock pin (see Figure 2.17).

When integrating the OOL output to convert the pulsed output to a level, a resistor must be added between the OOL pin and the capacitor. This avoids that a current bigger than 400 µA flows through the pin from the capacitor.

The lock output is software selectable as given in Table 2–6 below. Operating principle of out-of-lock is described overleaf.

Table 2–6. Out-Of-Lock Bit Allocations

OLP	OLA	Out-of-Lock Select
0	0	Output disabled
0	1	Auxiliary phase error
1	0	Principal phase error
1	1	Both auxiliary and principal

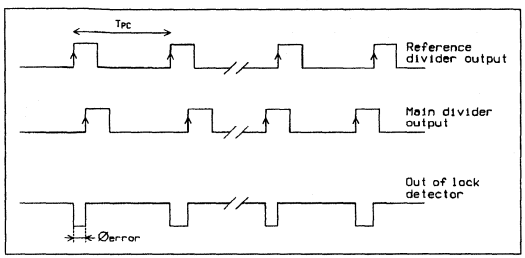


Figure 2–17. Operating Principal of the Out-of-Lock Detector

2.7 Digital-to-Analog Converter

A digital-to-analogue converter is integrated on the UMA1018M and UMA1020M synthesizers.

The DAC output current is scaled by the external resistance R_{ext} at pin I_{SET}, also used by the charge pumps. The nominal full scale current is 2 x I_{SET}. An external user-defined ground referenced resistance connected to the DAC output allows producing a full scale voltage (from 0V to V_{DD1} – 0.4V).

The DAC signal is monotonic across the full range of programmation. A programmed code of 00 corresponds with the minimum DAC leakage current (I_{10min}). It should be less than 5 µA programmed code of 7F corresponds to 2 x I_{SET} x (127 / 128).

The worst monotonic cases occur between 3Fh and 40h, 1Fh and 20h. Here, ΔI measured varies from 0.1 x $\Delta I_{expected}$ to 1.9 x $\Delta I_{expected}$.

Example:

R_{ext} = 12k I_{SET} = 1.2 / 12k = 100 µA
$\Delta I_{expected} = I_{SET}$ x 2 x (3Fh – 40h) / 128 = 1.56 µA
° $\Delta I_{measured}$ can vary between 0.16 µA to 3 µA

The on-board DAC allows adjustment of an external component, such as the central frequency of a VTCXO (Voltage Controlled Temperature Compensated Crystal Oscillator).

3. LOOP FILTER DESIGN

3.1 Basic Loop Filter Design Procedure

This section gives the procedure to ensure a quick and simple loop filter design. The method is based on first order approximations, and provides a working solution without the need for computer simulation. Reading appendices A and B can be useful to clarify some PLL terms and equations of this chapter.

The purpose of a Phase Locked Loop (PLL) in a single loop frequency synthesizer as shown in Figure 3–1 is to transfer the spectral purity and stability of a fixed reference frequency oscillator (TCXO or VTCXO) to that of the Voltage Controlled Oscillator (VCO) output.

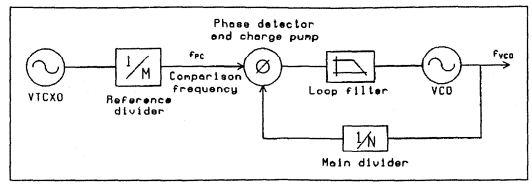


Figure 3–1. Basic Phase Lock Loop Block Diagram

The correct design of the loop filter is of considerable importance to have the optimum performance from the synthesizer. The filter should be designed so as to achieve the required compromise between noise performance and switching time.

Loop filters are usually passive when used with current charge pumps, but can be active if desired. Passive loops have the advantage of reduced noise, fewer parts count and low cost. With UMA1018M or UMA1020M synthesizers, only passive loop filters are necessary. Two common configurations are shown overleaf. The filters in Figure 3–2 are classified in terms of the order of the loop formed.

With the UMA1018M or UMA1020M, the use of the loop filter (a) is often sufficient. For applications requiring further comparison frequency breakthrough rejection, a low pass filter stage (R_3, C_3) can be added. It reduces comparison frequency breakthrough spurs without affecting too much the transient response of the loop when correctly designed.

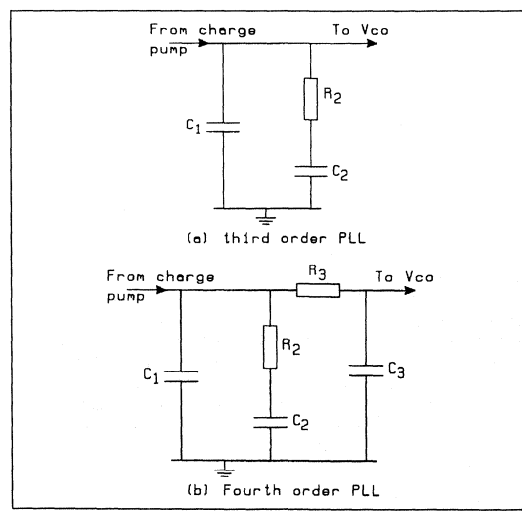


Figure 3–2. Different Types of Passive Loop Filter

Loop parameters are first chosen, they are:

- VCO frequency f_{VCO} (in Hz)
- Phase comparator frequency f_{PC} (in Hz)
- Switching time t_S (in seconds)
- VCO gain K_{VCO} (in Hz/V)

- Phase comparator gain I_{CP} (in amps/cycle)

As the starting point, the equations below are used.

$$W_n = 2 \cdot \Pi \cdot f_n = \left(\frac{K_{VCO} \cdot I_{CP}}{C_2 \cdot N}\right)^{1/2} \quad (1.)$$

$$R_2 = 2 \cdot \rho \left(\frac{N}{(K_{VCO} \cdot I_{CP} \cdot C_2)}\right)^{1/2} \quad (2.)$$

where f_n is the natural frequency (in Hz) and ρ is the damping coefficient.

Calculate the resistor R_{ext} for setting the charge pump output current from

$$R_{ext} = \frac{1.2}{I_{SET}} \quad (3.)$$

I_{CP} is related to I_{SET} according to the relationship given in Table 2–1 and whether the two charge pumps CPP and CPPF are shorted together or not.

Determine the natural frequency f_n

$$f_n = \frac{2.5}{t_S} \quad (4.)$$

It has been found by experience that a good PLL loop filter design takes a switching time (t_S) of less than $2.5/f_n$ to settle to a new frequency. This rule of thumb allows a good compromise between switching time, stability and noise performance when using the UMA1018M and UMA1020M synthesizers. Of course the switching time will also depend on the size of the frequency jump and the definition of when the PLL is settled (i.e., acceptable frequency or phase error with respect to target).

Determine main divider ratio from

$$N = \frac{f_{VCO}}{f_{PC}} \quad (5.)$$

Determine angular velocity W_n (in rad/seconds) from

$$W_n = 2 \cdot \Pi \cdot f_n \quad (6.)$$

Determine C_2 from (1)

$$C_2 = \left(\frac{K_{VCO} \cdot I_{CP}}{W_n^2 \cdot N}\right) \quad (7.)$$

Select damping ratio of approximately 0.9 for a good compromise between switching time and stability.

Determine R_2 from (2)

$$R_2 = 2 \cdot \rho \left(\frac{N}{K_{VCO} \cdot I_{CP} \cdot C_2}\right)^{1/2}$$

Choose C_1 between 1/10 and 1/15 the value of C_2

Determine R_3 from

$$R_3 \geq 2 \cdot R_2 \quad (8.)$$

Determine C3 from

$$C3 < \left(\frac{R_2 \cdot C_2}{20 \cdot R_3}\right) \quad (9.)$$

A program using this cook book method has been written for use on IBM PC (and compatible). It is included with the 3-wire serial bus control software diskette. Values given by the program are approximate and the final values should be optimized. For further optimization, both computer simulation programs, as well as practical experiments, are required.

Capacitors with high leakage currents, such as electrolytic capacitors and capacitors with piezoelectric or delay effects are not preferred because of higher comparison frequency breakthrough and increased switching times. A polyester film capacitor is a good idea for C_2.

3.2 Analysis and Simulation

For analysis, optimization and worst case design of more complex filters, key loops parameters can be entered into a simulation program.

Generally, a stable loop with an acceptable noise performance and a given switching time is needed. Unfortunately, these two requirements are dependent and must be traded off against each other. Stability, being an absolute necessity, gets higher priority. With third order loop filters (see Figure 3–3), the phase margin is the simplest criterion for the stability.

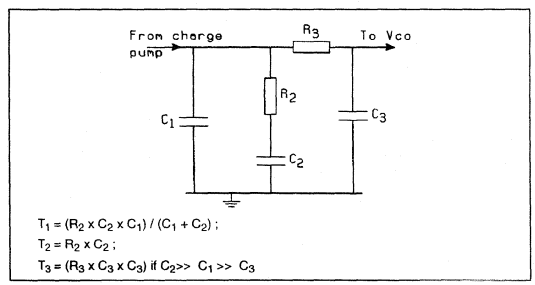


Figure 3–3. Third Order Loop Filter

The phase margin is easily determined from the Bode plot. A Bode plot displays the open loop transfer function magnitude and phase. Figure 3–4 shows Bode plot of a fourth order loop with third order filter (type 3 fourth order system) and a pole in the origin due to the VCO.

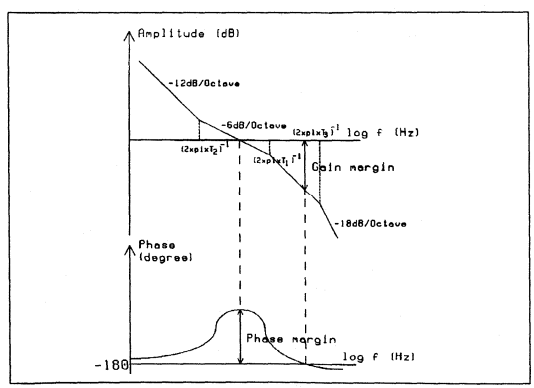


Figure 3–4. Bode Plot 4th Order Open PLL Transfer Function Magnitude and Phase

The phase margin is defined as the difference between 180° and the phase of the open loop transfer function at the frequency where the gain is 1 (gain cross over). The critical point for stability is a phase margin of 0°. The factor by which the system gain would have to be increased for the phase margin to reach the critical value of 0° is called the gain margin.

The time constants in the loop filter are key to controlling the overall loop performance and phase margin. The offset of different time constants can be evaluated from the Bode diagram. The reciprocal of the time constants of the loop filter in Figure 3–3 are the break points in the magnitude plot of Figure 3–4.

When increasing the time constant $T_3 = C_3 \times R_3$, the breakpoint (T_3)–1 will move left and the magnitude curve will start to roll off at a lower frequency. Therefore, the greater the time constant T_3, the better the comparison frequency breakthrough is suppressed. But increasing T_3 will force the point of inflection of the phase margin curve to move to the left as well, this decreasing the phase margin and eventually reducing system stability.

By iteration, inspection of the Bode plot, adjusting the loop filter values and measuring the performance, will yield a compromise between switching time, stability and noise. Simulation programs may give reasonable approximations of PLL behavior, but their accuracy is always limited due to the fact that many practical imperfections and non linearities are not taken into account.

Phase margin between 30° and 70° is required for most applications. The larger the phase margin, the more stable the loop, and the slower the transient response and hence the switching time. A loop with a low phase margin is still stable but may exhibit other problems aside from outright oscillation, low phase margin makes the transient response more oscillatory. A phase margin of 45° is a good compromise between desired stability and the other generally undesired effects.

3.3 Adaptive Loop

Some applications may need to have a dual time constant loop. With two principal charge pumps, UMA1018M and UMA1020M allow this to be implemented. The loop uses both charge pumps for fast frequency switching. Then the phase detector drives just the principal charge pump (CPP) after obtaining the required frequency with a lower bandwidth and hence lower noise. The loop filter used is shown in the Figure 3–5. This filter allows an optimized filter when both charge pumps are ON or when just one charge pump is active.

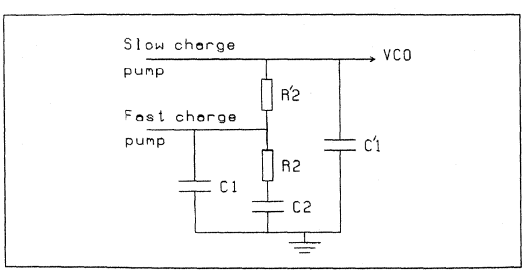


Figure 3–5. Adaptive Loop Filter

The loop filter calculation is given below:

- Use the same design procedure from paragraph 3.2 to calculate the main capacitor C_2, the damping resistor R_2 and the filter capacitor C_1.
- When the fast charge pump CPPF is disabled, loop stability needs to be maintained for the loop which uses only CPP. Recalculate value for the damping resistor with the new value of I_{CP} and ρ = 0.9

$$R'_2 = 2 \cdot \rho \left(\frac{N}{(K_{VCO} \cdot I_{CP} \cdot C_2)} \right)^{1/2} - R_2$$

- Determine C'_1 from

$$C'_1 < \frac{R_2 \cdot C_2}{20 \cdot R'_2}$$

Some precautions must be taken when the principal fast charge pump is switched off. A parasitic capacitor, due to the integrated circuit and the printed circuit board, exists between the FAST and CPPF pins. When the signal is sent to the FAST pin, a coupling through the parasitic capacitance on to the CPPF pin, results in a VCO frequency drift. This problem can he reduced by decreasing the slope of the FAST signal with a RC filter.

3.4 PCB Layout Considerations

With frequency synthesizer layout, good RF design techniques should be employed. To avoid crosstalk between synthesizers (auxiliary and principal), the printed circuit board should have a solid ground plane on the non surface mount side (apart from isolated pads for non-grounded connections to leaded components). On the surface mount side of the board, the ground plane should be designed round each synthesizer, and underneath the Philips integrated circuit so as to provide maximum isolation between two PLLs. A good number of plated-through holes must connect the two layers of the ground plane.

Suitable high frequency capacitors (100 nF) in series with a small value resistor (12Ω) should be used for power supply decoupling. V_{DD1} and V_{DD2} can be shorted at the output of the integrated circuit. However, separate decoupling to Pins 4 and 5 will be better. It is very important to de-couple as close as possible to Pins 4 and 5.

3.5 Worked Example

In this chapter, a design example based on the fourth order PLL for GSM specification is shown. Only the loop filter of the UMA1018M principal synthesizer is calculated.

Experiments show that the use of just one charge pump gives better close in noise (about 3dBc/Hz) than two enabled charge pumps with outputs (CPPF + CPP) connected together. Because slow charge pump is better (about 1 dBc/Hz) than fast charge pump, only the slow charge pump is used in this worked example. The fast charge pump is switched off via pin FAST.

- VCO Frequency f_{VCO} = 902MHz
- Phase comparator frequency f_{CP} = 200kHz
- Switching time t_S = 600µs
- VCO gain K_{VCO} = 11MHz/V
- Phase comparator gain I_{CP} = 0.4mA with CR1 bit set to 0 and CR0 bit set to 0. Pins CPP and CPPF connected together. Fast charge pump is switched off by the pin FAST. Following the basic design procedure from paragraph 3.2 yields:

$I_{CP} = 0.4mA = 4 \times I_{SET} \rightarrow I_{SET} = 100\mu A$
$R_{ext} = 1.2 / I_{SET} = 1.2 / 100\mu A = 12k\Omega$
Natural frequency $f_n = 2.5 / t_S = 2.5 / 60\mu s = 4170Hz$
Main divider ratio $N = f_{VCO} / f_{CP} = 902MHz / 200kHz = 4510$

The main components in the loop filter are:

main capacitor C_2 $= K_{VCO} \times I_{CP} / W_n^2 \times N$
$= 11MHz \times 0.4mA / (2 \times 11 \times 4170)^2 \times 4510$
$= 1.5nF$

damping resistor R_2 $= 2 \times \rho \, (N / K_{VCO} \times I_{CP} \times C_2)^{1/2}$
$= 2 \times 0.9 \, (45101 / 11MHz \times 0.4mA \times 1.5nF)_{112}$
$= 47k\Omega$

filter capacitor $C_2 / 15 \leq C_1 \leq C_2 / 10$ $C_1 = 100pF$

$R_3 \geq 2 \times R_2$ $R_3 = 100k\Omega$

$C_3 < (R_2 \times C_2 / 20 \times R_3)$ $C_3 = 22pF$

A software simulation program has been used to verify the stability of this loop filter. The phase margin is maximum and equal to 52° at the gain cross-over point. The requirement for basic loop stability is fulfilled (see Figure 3–6).

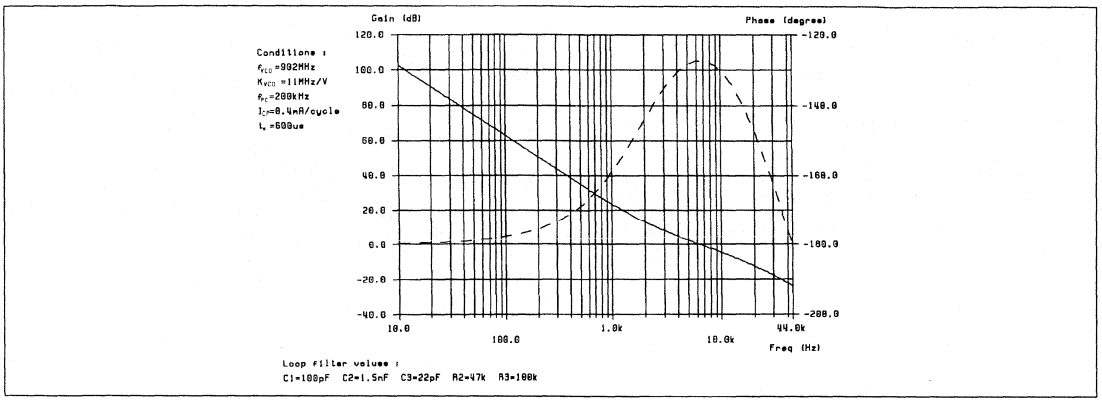


Figure 3–6. Simulated Bode Plot of 4th-Order Open Loop Transfer Function of UMA1018M Principal Synthesizer, Magnitude and Phase vs Frequency

The design procedure is similar with the auxiliary synthesizer and with the UMA1020M for the DCS1800 application. Results are summarized in Table 3–1 and 3–2.

Table 3–1. Design Parameters and Simulation for UMA1018M Dual Synthesizer

Parameter		Principal synthesizer	Auxiliary synthesizer
Loop components (refer to figure 3.3) VCO		C_1 = 100p C_2 = 1.5n C_3 = 22p R_2 = 47k R_3 = 100k	C_1 = 470p C_2 = 10n C_3 = 100p R_2 = 18k R_3 = 39k
VCO gain K_{VCO} VCO frequency f_{VCO}		11MHz/V 902MHz	2.5MHz/V 100MHz
Comparison frequency f_{PC}		200kHz	100kHz
Charge pump	Current gain I_{CP}	0.4mA/cycle	0.4mA/cycle
	R_{ext}	12k	
	Bits CR0, CR1	CR0 = 0, CR1 = 0	
Reference frequency VTCXO		13MHz	
Unity gain phase margin (simulated)		52.6 deg	58.9 deg
Gain margin at 180 deg phase margin (simulated)		24dB	27dB
Unity gain loop bandwidth (simulated)		6.3k	2.8k
Natural frequency (simulated)		4.1k	1.6k
Switching time for a 25MHz step ; freq error < 1kHz (simulated)		540µs	

Table 3–2. Design Parameters and Simulation for UMA1020M Dual Synthesizer

Parameter		Principal synthesizer	Auxiliary synthesizer
Loop components (refer to figure 3.3) VCO		C_1 = 820p C_2 = 13n C_3 = 180p R_2 = 5.6k R_3 = 15k	C_1 = 470p C_2 = 10n C_3 = 100p R_2 = 18k R_3 = 39k
VCO gain K_{VCO} VCO frequency f_{VCO}		20MHz/V 1890MHz	2.5MHz/V 100MHz
Comparison frequency f_{PC}		200kHz	100kHz
Charge pump	Current gain I_{CP}	3.6mA	0.4mA
	R_{ext}	12k	
	Bits CR0, CR1	CR0 = 1, CR1 = 0	
Reference frequency VTCXO		13MHz	
Unity gain phase margin (simulated)		53.2 deg	58.9 deg
Gain margin at 180 deg phase margin (simulated)		25dB	27dB
Unity gain loop bandwidth (simulated)		6.45k	2.8k
Natural frequency (simulated)		3.8k	1.6k
Switching time for a 25MHz step ; freq error < 1kHz (simulated)		550µs	

4. MEASUREMENTS AND TYPICAL RESULTS

This section describes the performance of the UMA1018M and UMA1020M demoboards with the loop filters indicated in Table 3–1 and 3–2.

The relevant performance criteria for a synthesizer are usually:

- Close in phase noise
- Comparison frequency breakthrough
- Switching time
- Integrated phase jitter

Close in noise was measured using a direct reading from the spectrum analyzer and referred to 1Hz bandwidth. This is normally done at a given offset from the carrier while still inside the loop bandwidth.

Integrated phase jitter was measured on a Rohde and Schwartz Modulation Analyzer in a 10Hz to 200kHz audio bandwidth.

Tables 4–1 to 4–3 summarize the measurement results. Figures 4–1 to 4–8 show some of the actual measurements. During the measurements both synthesizers were enabled and locked.

Table 4–1. Demoboard Measurement Results on UMA1018M Principal Synthesizer

VCO supply voltage : 5 volts Both synthesizers enabled UMA1018M supply voltage : 5 volts Temperature=25°C		Principal synthesizer
VCO frequency range		890MHz - 915MHz
Comparison frequency breakthrough	at 200kHz	- 81dBc
	at 400kHz	- 82dBc
	at 600kHz	< -82dBc
Switching time for frequency jump around centre frequency to within 1kHz of the target frequency	200kHz (1 channel)	450µs
	10MHz	500µs
	25MHz (max jump)	580µs
Close in noise (at 1kHz distance from carrier)		-78dBc/Hz
Integrated phase jitter		18 mrad rms

Table 4–2. Demoboard Measurement Results on UMA1020M Principal Synthesizer

VCO supply voltage : 3 volts Both synthesizers enabled UMA1020M supply voltage : 3 volts Temperature=25°C		Principal synthesizer
VCO frequency range		1878MHz - 1903MHz
Comparison frequency breakthrough	at 200kHz	- 77dBc
	at 400kHz	- 81dBc
	at 600kHz	< -82dBc
Switching time for frequency jump around centre frequency to within 2kHz of the target frequency	200kHz (1 channel)	370µs
	10MHz	430µs
	25MHz (max jump)	540µs
Close in noise (at 1kHz distance from carrier)		-70dBc/Hz
Integrated phase jitter (Obtained by integration of close in noise)		53 mrad rms

Table 4–3. Demoboard Measurement Results on Auxiliary Synthesizer

VCO supply voltage : 5 volts Both synthesizers enabled UMA1018M supply voltage : 5 volts Temperature=25°C		Auxiliary synthesizer
VCO frequency		97MHz - 104MHz
Comparison frequency breakthrough	at 100kHz	- 77dBc
	at 200kHz	- 80dBc
	at 400kHz	< -82dBc
Close in noise (at 2kHz from carrier)		-83dBc/Hz
Integrated phase jitter		6 mrad rms

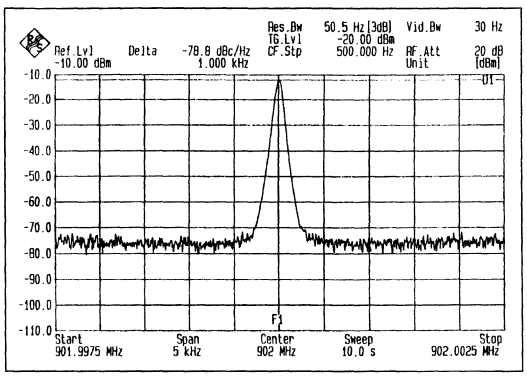


Figure 4–1. UMA1018M Principal Synthesizer Output Spectrum – Close in Noise

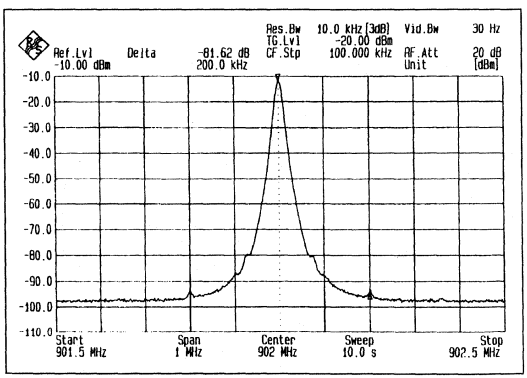


Figure 4–2. UMA1018M Principal Synthesizer – Comparison Frequency Breakthrough

Low power single/dual frequency synthesizers: UMA1017M/1018M/1019M(AM)/1020M(AM)

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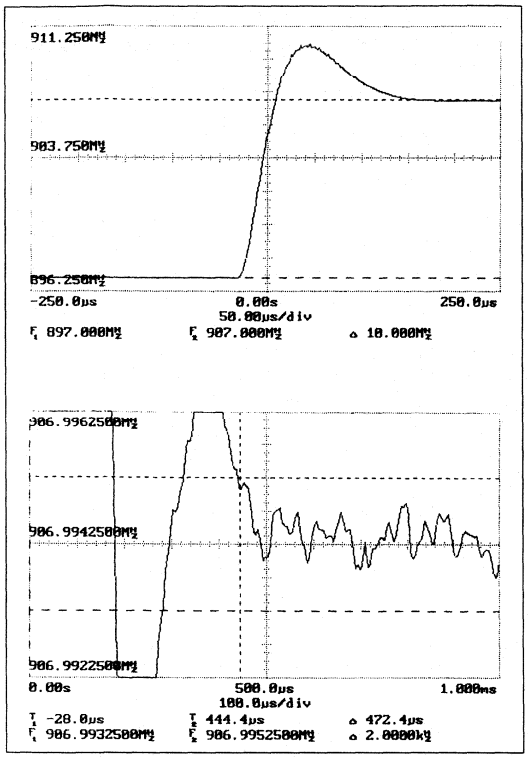


Figure 4–3. UMA1018M Principal Synthesizer – Settling Time for a 10MHz Step

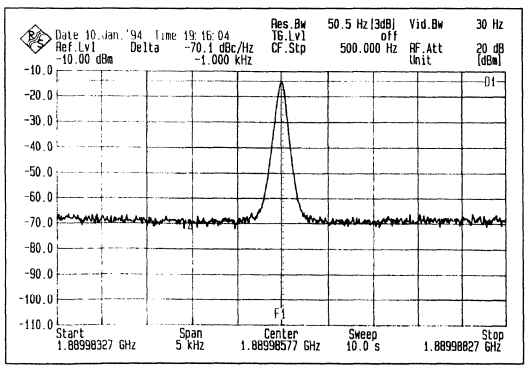


Figure 4–4. UMA1020M Principal Synthesizer Output Spectrum – Close in Noise

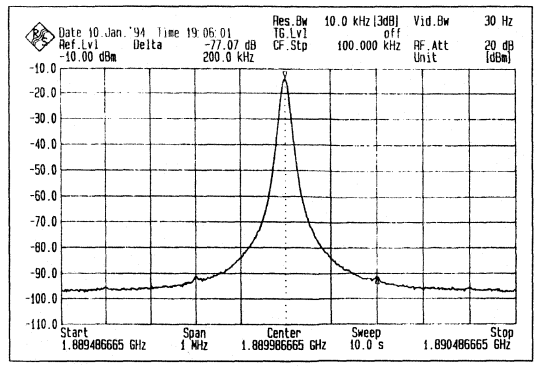


Figure 4–5. UMA1020M Principal Synthesizer – Comparison Frequency Breakthrough

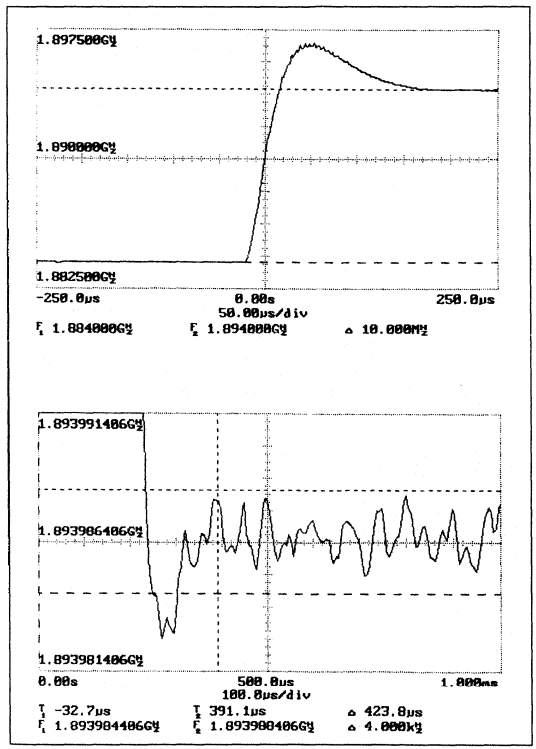


Figure 4–6. UMA1020M Principal Synthesizer – Settling Time for a 10MHz Step

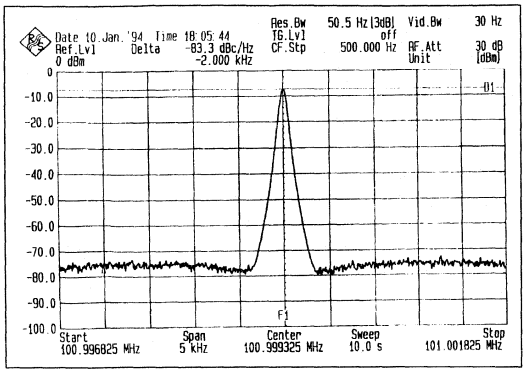


Figure 4–7. UMA1020M Auxiliary Synthesizer Output Spectrum – Close in Noise

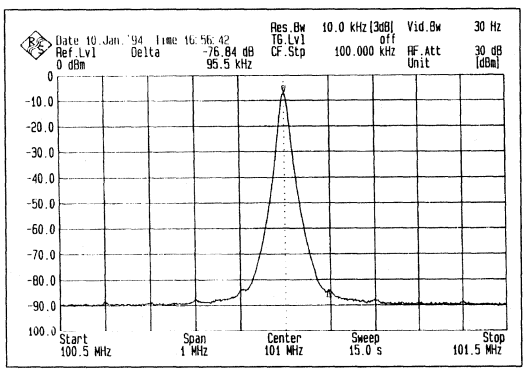


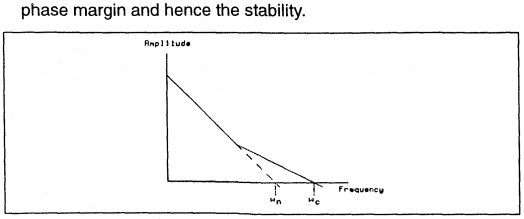
Figure 4–8. UMA1018M Auxiliary Synthesizer – Comparison Frequency Breakthrough

5. APPENDICES

5.1 Appendix A: PLL Terms

The following is a brief glossary of frequently encountered terms in PLL literature.

- **Natural frequency w_n**: the natural frequency of the loop. This is the frequency at which the loop would theoretically oscillate if the damping factor were zero.
- **Open loop cross-over frequency w_C**: this is the frequency at which the open loop gain is unity. It is useful in determining the phase margin and hence the stability.



- **Damping coefficient**: ρ can be used as a measure of the stability in second order systems. It is seldom used as a direct measure of stability in higher order designs.
- **Order of loop**: the order of the loop is the highest power of s (s=jw) in the denominator of the open loop transfer function. The example below shows a second order loop.

  $G(s) \times H(s) = (K_{VCO} \times I_{CP}) \times (s \times T_2 + 1) / (N \times C \times s^2)$
- **Type of loop**: the type of control system formed is defined by the number of perfect integrators in the loop. In the example, above, the loop is a type two system.
- **Phase margin Φm**: The phase margin, in degrees, is expressed as $\Phi m = \Phi(w_C) + 180$ where $\Phi(w_C)$ is the open loop phase shift at the frequency w_C
- **SSB phase noise or close in noise**: It is the noise level within the loop bandwidth relative to carrier at a given frequency offset. It is referred to a 1Hz bandwidth. It is expressed in dBc/Hz.
- **Integrated phase jitter or residual FM**: this is another measure of the noise performance of a signal source. This measure of integrated noise is usually specified over a particular audio bandwidth, e.g., 10 Hz to 200 kHz. It is expressed in degrees rms. An ideal synthesizer would have zero integrated phase jitter.
- **Spurious**: this defines the spectral purity of the oscillator. Common sources of spurious are the comparison frequency and harmonies. Comparison frequency breakthrough is generated by leakage in the loop filter components or the charge pump.
- **Settling time or switching time**: this indicates the time for a given frequency jump to be within a specified distance (frequency or phase) from target value.

5.2 Appendix B: Basic PLL Transfer Function

Figure 5–1 shows the block diagram of a basic control loop.

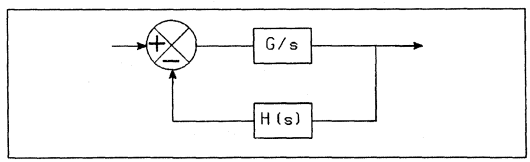


Figure 5–1. Block Diagram of a Loop

In open loop, the transfer function is

$$H(s) \cdot G(s) \quad \text{(a)}$$

In closed loop, the transfer function is

$$\frac{G(s)}{1 + G(s) \cdot H(s)} \quad \text{(b)}$$

If we apply these transfer functions to the Phase Locked Loop in Figure 5–2 with equations expressed in Laplace notation

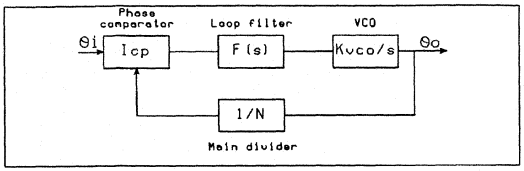


Figure 5–2. Block Diagram of a Phase Locked Loop

$$G(s) = \frac{I_{CP} \cdot K_{VCO} \cdot F(s)}{s} \quad (c)$$

$$H(s) = \frac{1}{N} \quad (d)$$

The PLL open loop transfer function is

$$\frac{I^{CP} \cdot K_{VCO} \cdot F(s)}{s \cdot N} \quad (e)$$

The PLL closed loop transfer function is

$$\frac{\Phi o(s)}{\Phi(s)} \frac{K_{VCO} \cdot I_{CP} \cdot F(s)/s}{1 + (K_{VCO} \cdot I_{CP} \cdot F(s)/s \cdot N)}$$

$$= \frac{N \cdot K_{VCO} \cdot I_{CP} \cdot F(s)}{(s \cdot N) + (K_{VCO} \cdot I_{CP} \cdot F(s)} \quad (f)$$

Basic performance of PLL is determined by R_2 and C_2 (see Figure 3–2) in the loop filter.

Note: when introducing more components in the loop filter, the expression for the transfer function becomes a lot more complicated. Anyway, this design can serve as a starting point for even more complicated filters.

The transfer function of this simple loop filter is

$$F(s) = R_2 + \left(\frac{1}{s \cdot C_2}\right) = \left(\frac{(s \cdot R_2 \cdot C_2) + 1}{(s \cdot C_2)}\right) \quad (g)$$

Then, the closed loop transfer function is

$$\frac{\Phi o(s)}{\Phi i(s)} = \frac{N \cdot K_{VCO} \cdot I_{CP} \cdot F(s)}{s \cdot N + K_{VCO} \cdot I_{CP} \cdot F(s)} =$$

$$\frac{N \cdot K_{VCO} \cdot I_{CP}(s \cdot R_2 \cdot C_2 + 1)/s \cdot C_2}{s \cdot N + K_{VCO} \cdot I_{CP}(s \cdot R_2 \cdot C_2 + 1)/s \cdot C_2} =$$

$$\frac{N(s \cdot R_2 \cdot C_2 + 1)}{\frac{s^2 (C_2 \cdot N)}{(K_{VCO} \cdot I_{CP})} + (s \cdot R_2 \cdot C_2 + 1} \quad (h)$$

If we compare the denominator of (h) with

$$\frac{s^2}{w_n^2} + \frac{2 \cdot \rho \cdot s}{W_n} + 1$$

we find the equations shown below:

$$w_n = \left(\frac{K_{VCO} \cdot I_{CP}}{C_2 \cdot N}\right)^{1/2} \quad (i) \rightarrow (1)$$

$$\rho = \frac{w_n (R_2 \cdot C_2)}{2} \quad (j)$$

$$R_2 = 2 \cdot \rho \left(\frac{N}{K_{VCO} \cdot I_{CP} \cdot C_2}\right)^{1/2} \quad (k) \rightarrow (2)$$

5.3 APPENDIX C: DEMONSTRATION BOARD DOCUMENTATION

Table 5–1 Parts List for UMA1018M/UMA1020M Demonstration Board (GSM/DCS1800)

Reference	Value / Type	Size	Reference	Value / Type	Size
R1	560kΩ	0805 SMD	C1	33pF	0805 SMD
R2	560kΩ	0805 SMD	C2	33pF	0805 SMD
R3	560kΩ	0805 SMD	C3	33pF	0805 SMD
R4	12kΩ	0805 SMD	C4	56pF	0805 SMD
R5	56Ω	0805 SMD	C5	56pF	0805 SMD
R6	18Ω	0805 SMD	C6	560pF	0805 SMD
R7	18Ω	0805 SMD	C7	100pF	1206 SMD
R8	12Ω	0805 SMD	C8	47µ / 25V	Alu 5x11
R9	12Ω	0805 SMD	C9	470pF	0805 SMD
R10	18kΩ	0805 SMD	C10	10nF	0805 SMD
R11	39kΩ	0805 SMD	C11	100pF	0805 SMD
R12	12Ω	0805 SMD	C12	100nF	1206 SMD
R13	100kΩ	0805 SMD	C13	–	
R14	3k9	0805 SMD	C14	100pF (820pF)	0805 SMD
R15	100kΩ	0805 SMD	C15	–	0805 SMD
R16	–		C16	1.5nF (12n//1n)	0805 SMD
R17	–(12)	0805 SMD	C17	22pF (180pF)	0805 SMD
R18	0	0805 SMD	C18	100nF	1206 SMD
R19	47kΩ (5k6)	0805 SMD	C19	100nF	1206 SMD
R20	100kΩ (15kΩ)	0805 SMD	C20	56pF	0805 SMD
R21	12kΩ	0805 SMD	C21	56pF	0805 SMD
R22	12kΩ	0805 SMD	C22	100nF (–)	1206 SMD
R23	56Ω	0805 SMD	C23	47µ / 25V	Alu 5x11
R24	18Ω	0805 SMD	C24	1nF	0805 SMD
R25	18Ω	0805 SMD	C25	10nF	0805 SMD
R26	18Ω	0805 SMD	C26	22nF	0805 SMD
R27	12 (–)	0805 SMD	C27	100nF	1206 SMD
R28	100kΩ	0805 SMD	C28	100nF	1206 SMD
R29	22kΩ	0805 SMD	C29	100nF	1206 SMD
R30	1k8	0805 SMD	C30	1µ / 63V	Alu 5x11
R31	1k2	0805 SMD	C31	–(100nF)	1206 SMD
R32	–	0805 SMD	D1	LED	
R33	12	0805 SMD	L1	4.77nF	1008CT
R34	–(12)	0805 SMD	78L05		T092
VCO1	MQC505-902	MURATA	LM317LZ		T092
VCO2	(URAE8x542A)	ALPS	FXTLIN	PN-Minicoax-Bus SMB	
VCO3	Aux. VCO		RF_PRI	PN-Minicoax-Bus SMA	
VTCX01	13MHz	B8 Philips	RF_AUX	PN-Minicoax-Bus SMB	
VCTX02	13MHz	B9 Philips			

NOTE: All values in between brackets ( ) are related to 1800MHz application.

J1 Controls power down auxiliary synthesizer
J2 Activates the FAST charge pump
J3 Controls power down principal synthesizer
J4 Enables DAC output
J5 Selects VTCXO or external reference frequency
J6 Selects 3V, 5V or external variable voltage
J7 Disconnects the auxiliary VCO
X1 3-Wire bus control
X2, X4 Supply
X3 Modulation

Table 5–2 Parts List for Interface Card and Auxiliary VCO

Reference	Value / Type	Size	Reference	Value / Type	Size
Components for the Auxiliary VCO 100 MHz					
Rf1	27Ω	0805 SMD	Cf1	1pF	0805 SMD
Rf2	150Ω	0805 SMD	Cf2	27pF	0805 SMD
Rf3	1kΩ	0805 SMD	Cf3	68pF	0805 SMD
Rf4	820Ω	0805 SMD	Cf4	–	0805 SMD
Rf5	1kΩ	0805 SMD	Cf5	22pF	0805 SMD
Rf6	1kΩ	0805 SMD	Cf6	33nF//22pF	0805 SMD
Rf7	10kΩ	0805 SMD	Cf7	3p3	0805 SMD
Rf8	100Ω	0805 SMD	Cf8	3p9	0805 SMD
Rf9	270Ω	0805 SMD	Cf9	10pF	0805 SMD
Rf10	82Ω	0805 SMD	Cf10	15pF	0805 SMD
Lf1	120nF	0805 SMD	Cf11	1pF	0805 SMD
Lf2	180nF	0805 SMD	Cf12	8n2	0805 SMD
CVf1	BBY31	SOT-23	Tf1	BFT92	SOT-23
			Tf2	BFR92	SOT-23
Components for PC Interface Card					
R1	10kΩ	0805 SMD	C1	100nF	1206 SMD
R2	10kΩ	0805 SMD	IC1	74HC04	
R3	10kΩ	0805 SMD	J1	Sub D 25 pins	
R4	330Ω	0805 SMD	X1	6 pins	
R5	330Ω	0805 SMD			
R6	330Ω	0805 SMD			

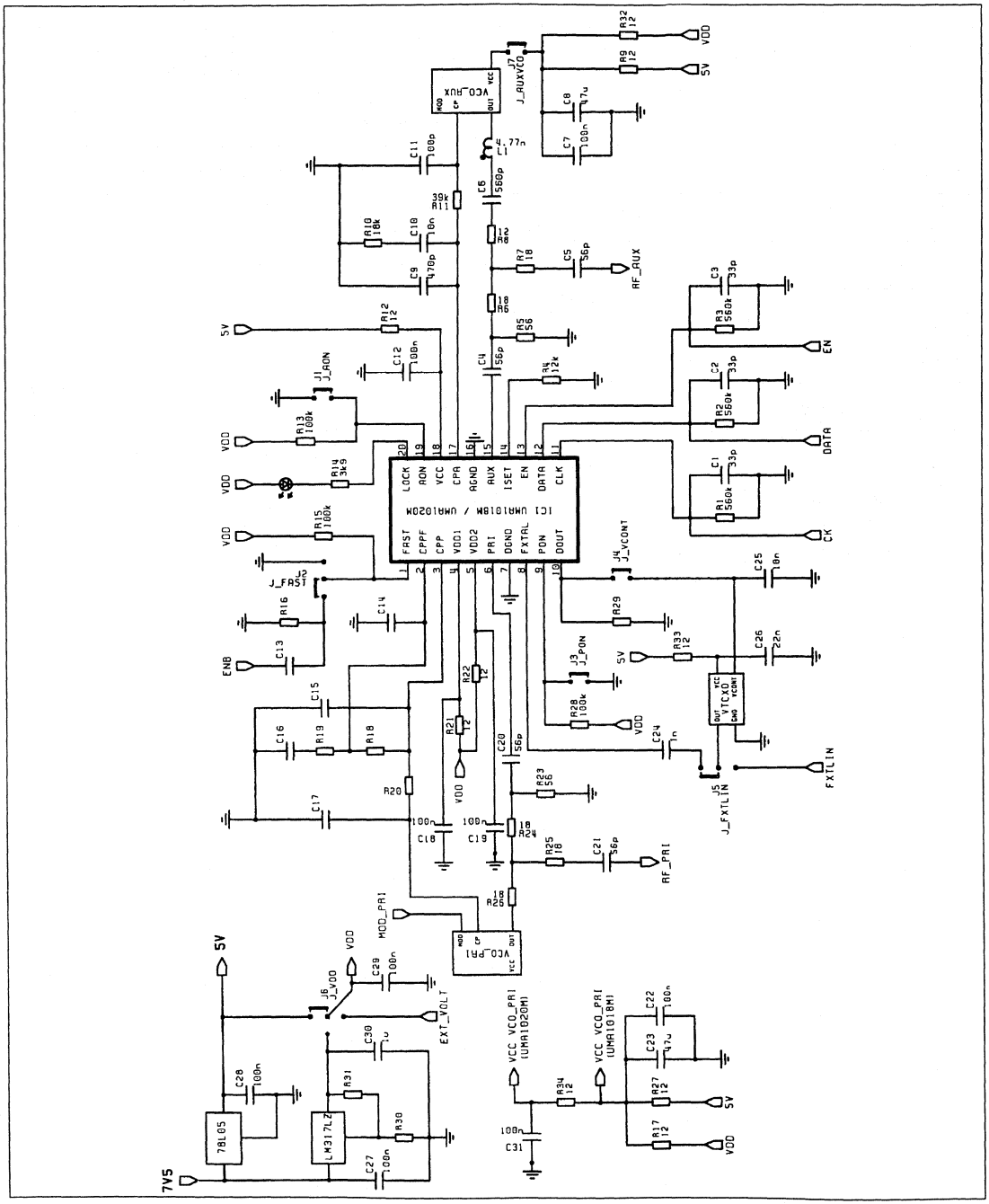


Figure 5–3. Demonstration Board Circuit Diagram

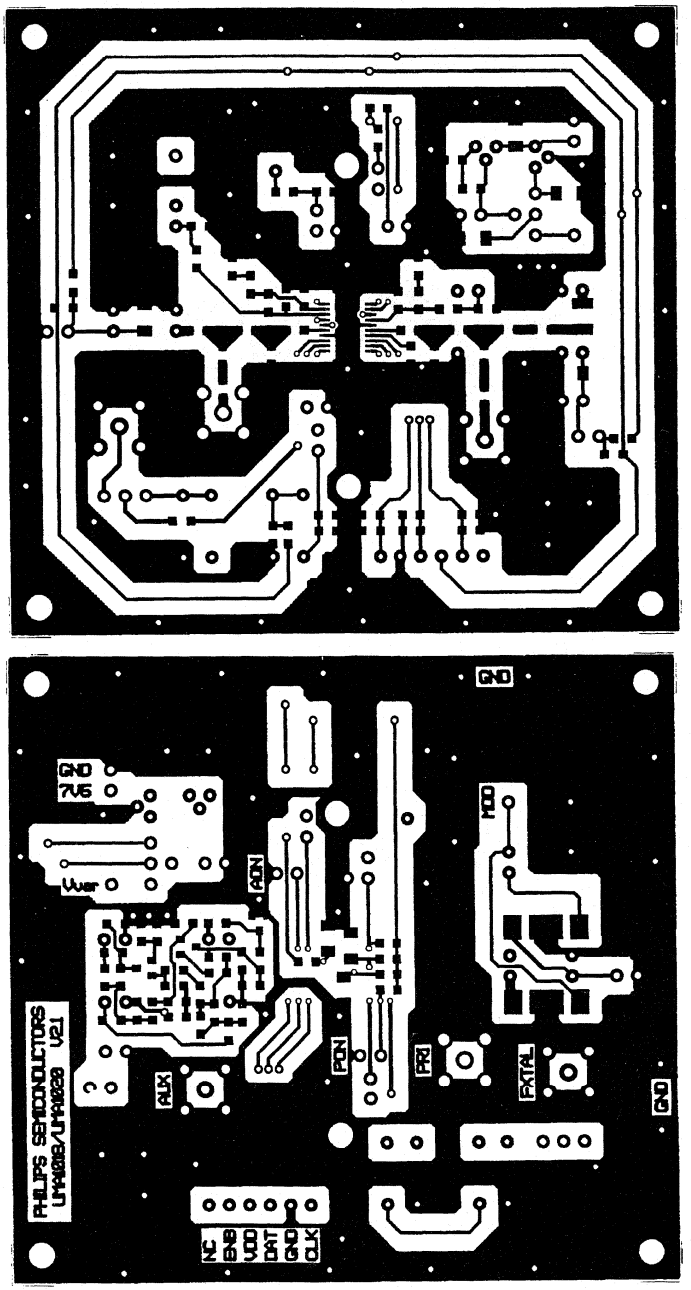


Figure 5–4. Demonstration Board PCB Layout

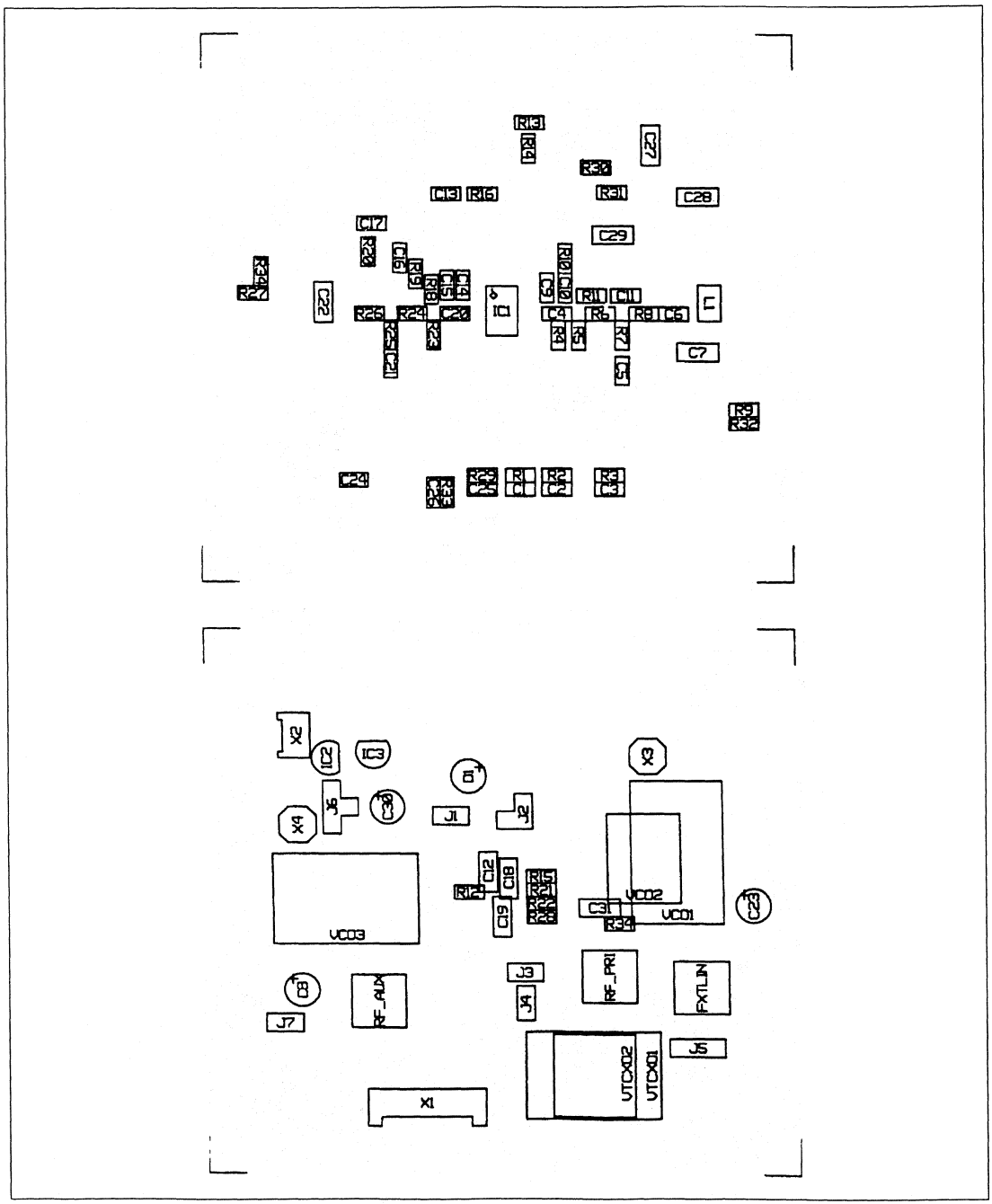


Figure 5–5. Demonstration Board Placement of Components

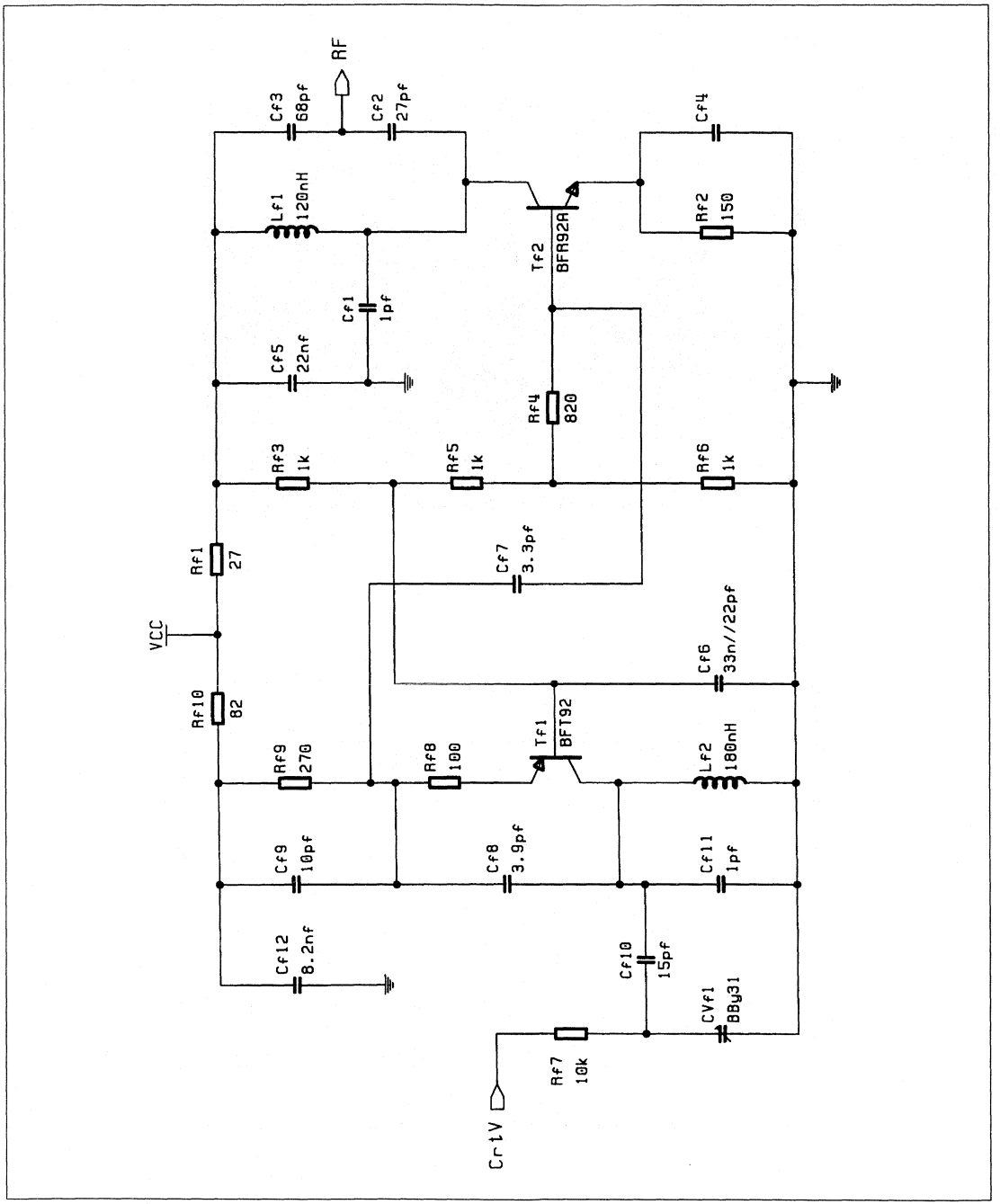
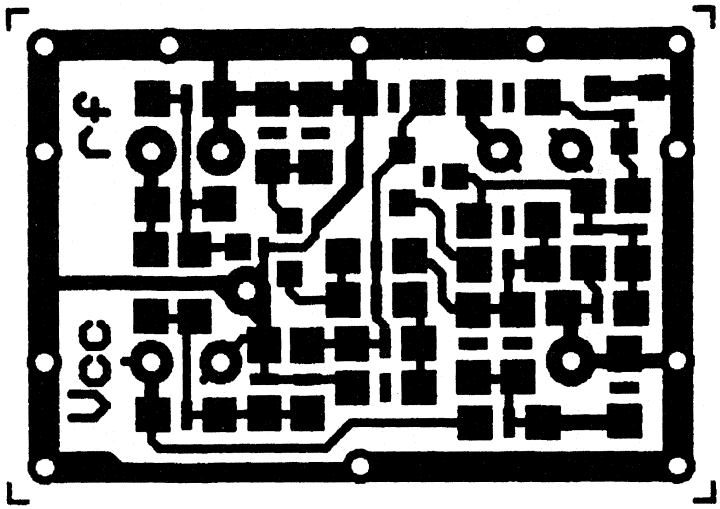


Figure 5–6. Auxiliary 100MHz VCO Circuit Diagram



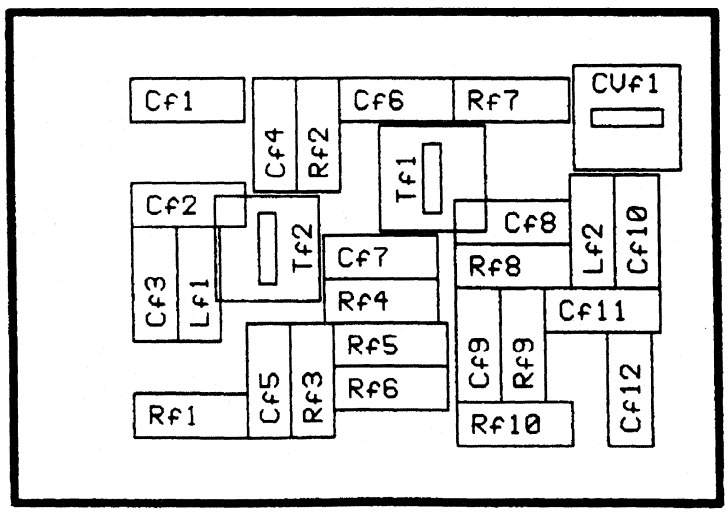


Figure 5–7. Auxiliary 100MHz VCO PCB Layout and Placement of Components

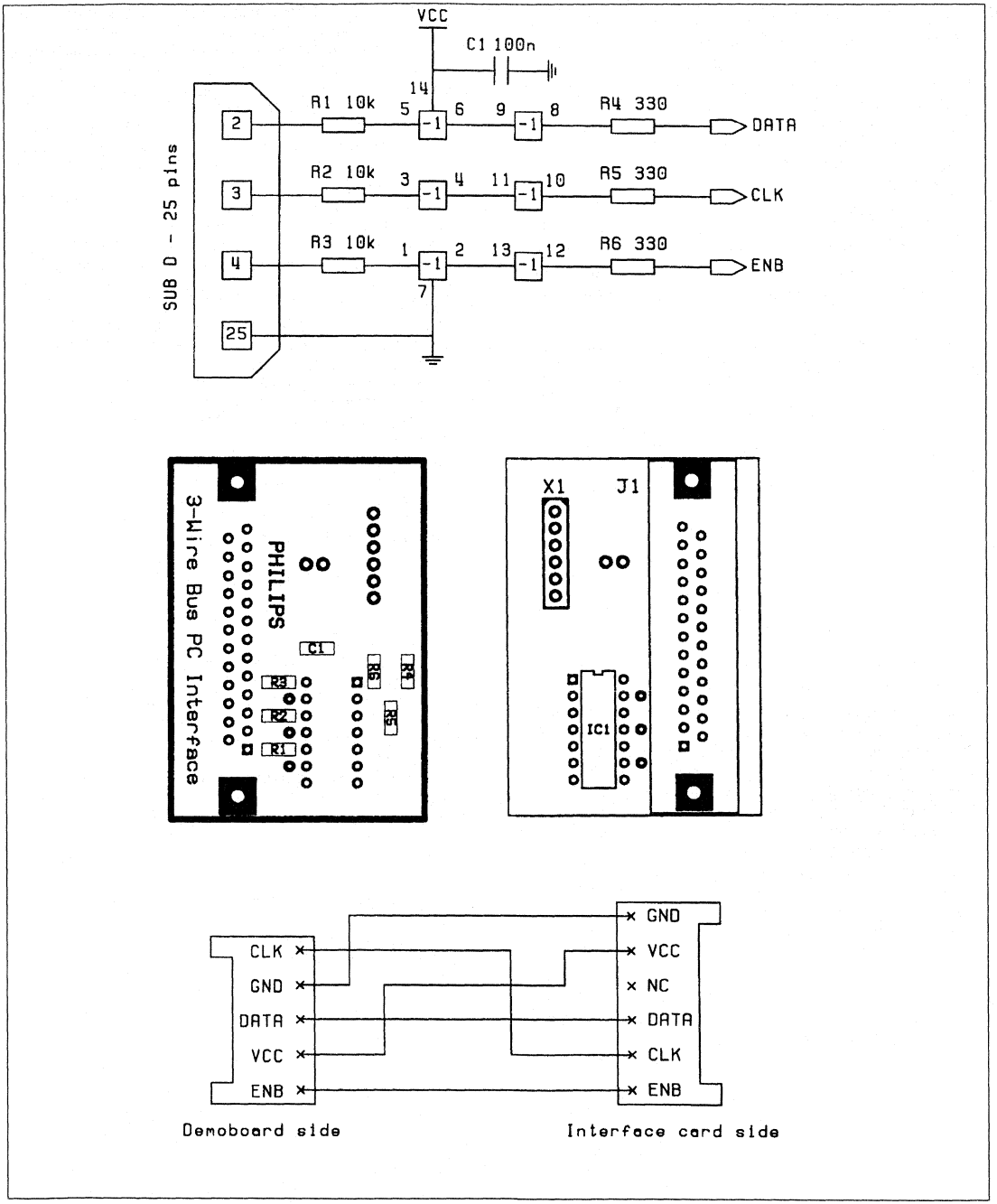


Figure 5–8. Interface Card PCB Layout and Cable Connection

6. FREQUENTLY ASKED QUESTIONS

Q. How can the noise be improved?

A. Five things can be done to improve the noise:

1. Increase the f_{XTAL} level (within specification limits).
2. Use a higher crystal frequency. Doubling the reference frequency improves the close in noise by 3dBc/Hz.
3. Use only one charge pump (CPP or CPPF). The dynamic gain is more constant with supply voltage, frequency and temperature.
4. Use a narrower loop filter. But this increases the switching time.
5. Ensure that supply is well decoupled.

Number 4 does not improve the close in noise, just the phase noise. Other points can improve the close in noise and so, the total phase noise of the PLL.

Q. What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?

A. The phase detector gain is equal to the charge pump output current I_{CP} divided by 2π since the phase detector covers 2π range. However, when using the design formulas, the phase detector gain can be replaced directly by I_{CP} because the 2π factor will be cancelled out by the 2π also in the VCO gain.

Q. What kind of main capacitor should be used in the loop filter?

A. Higher leakage current raises comparison frequency breakthrough and the 'memory effect' of higher dielectric capacitor degrades the settling time, Z5U, X7R series and electrolytic capacitors are not used. A polyester film capacitor is generally used with main capacitor of the loop filter.

Q. How to use the synthesizer with $V_{DD} < 4.5$ V whereas DATA, CLK and $\overline{E}$ are at 5 V logic?

A. Because of protection against electrostatic discharges, the input voltage for these logic pins can not be greater than $V_{DD} + 0.3$ V. An interface between the microcontroller and the synthesizer is then needed to reduce voltage at serial bus pins. A voltage divider using two resistors is a simple and cheap solution to implement. The design of this interface involves performance compromise between the current consumption and the programming speed, which depend on the resistor values in the voltage divider and the parasitic capacitance from the demonstration board. A Technical Marketing Report (TMT94008) describes some measurement results. For different values of $V_{DD} < 4.5$ V, the current consumption and the programming speed are given.

Q. Open loop modulation?

A. Two methods of open loop modulation are briefly described. A complete report "UMA1020M Modulation Capability for DECT" (TMT250894) is available.

Method 1: only the principal fast charge pump is used, and it is enabled/disabled using the pin FAST. The principal charge pump (pin CPP) is grounded. An internal circuit synchronizes the FAST signal with the fast charge pump correction current pulses. This avoids opening the loop when the fast charge pump is still active, which would cause a frequency drift. After the loop is opened, the UMA1020M (or UMA1018M) principal synthesizer can then be powered down to reduce consumption. Some precautions must be taken when the principal fast charge pump is switched off.

Method 2: the loop is opened by powering down (PON pin) the principal synthesizer directly. The signal sent to the PON is externally synchronized with the charge pumps to avoid powering down the synthesizer while they are still active.

Two problems can occur when a synthesizer is powered down:

The first is known as "load pulling". When the synthesizer is switched off, its RF input impedance may change and then an unintended jump in frequency is possible if the VCO is susceptible to load changes. This problem is negligible with the UMA10XX synthesizers, a frequency drift of less than 2kHz has been observed with the UMA1020M in a typical DECT application.

The second problem is called "pushing". The frequency of the VCO moves with changes in its supply voltage. When the principal synthesizer is powered down, it may temporally affect the supply voltage. Two separate voltage supplies (one for the synthesizer, the other for the VCO) will eliminate frequency shift due to "pushing". Alternatively, if using only one voltage supply, proper supply decoupling will attenuate.

7. REFERENCES

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1. INTRODUCTION

The TEA1118/A offer all the transmit, receive and line interface functions required in cordless telephone sets or in answering machines. They perform the interface between the line and the RF interface of a cordless telephone set or between the line and the codecs of a digital answering machine.

Furthermore, the TEA1118A includes a DTMF amplifier for dialling. The selection between the transmit amplifier and the DTMF amplifier is made with a MUTE or a TMUTE function. The MUTE function switches-off both the transmit and the receive amplifiers while the TMUTE switches-off only the transmit amplifier, both switch-on the DTMF amplifier.

The TEA1118 is mainly dedicated to applications where DTMF is not necessary (eg: answering machine application) or where DTMF is provided by some other part (eg: DECT application). The TEA1118A is mainly dedicated to CTO base stations.

The report is divided into two parts: the first part, up to chapter 3, gives a detailed description of the different circuit blocks of the TEA1118/A including operating principles, settings of DC and transmission characteristics and performances of the different functions; the second part describes the consecutive steps to design and adjust applications using the TEA1118/A and introduces the demoboard.

Note: the values of parameters given in this application note are as accurate as possible, but please, refer to the last product specification for final ones.

2. BLOCK DIAGRAMS AND PINNINGS

Fig. 1 shows the block diagram of the TEA1118, fig. 2 shows the block diagram of the TEA1118A, the pinnings are shown in fig. 3 and 4.

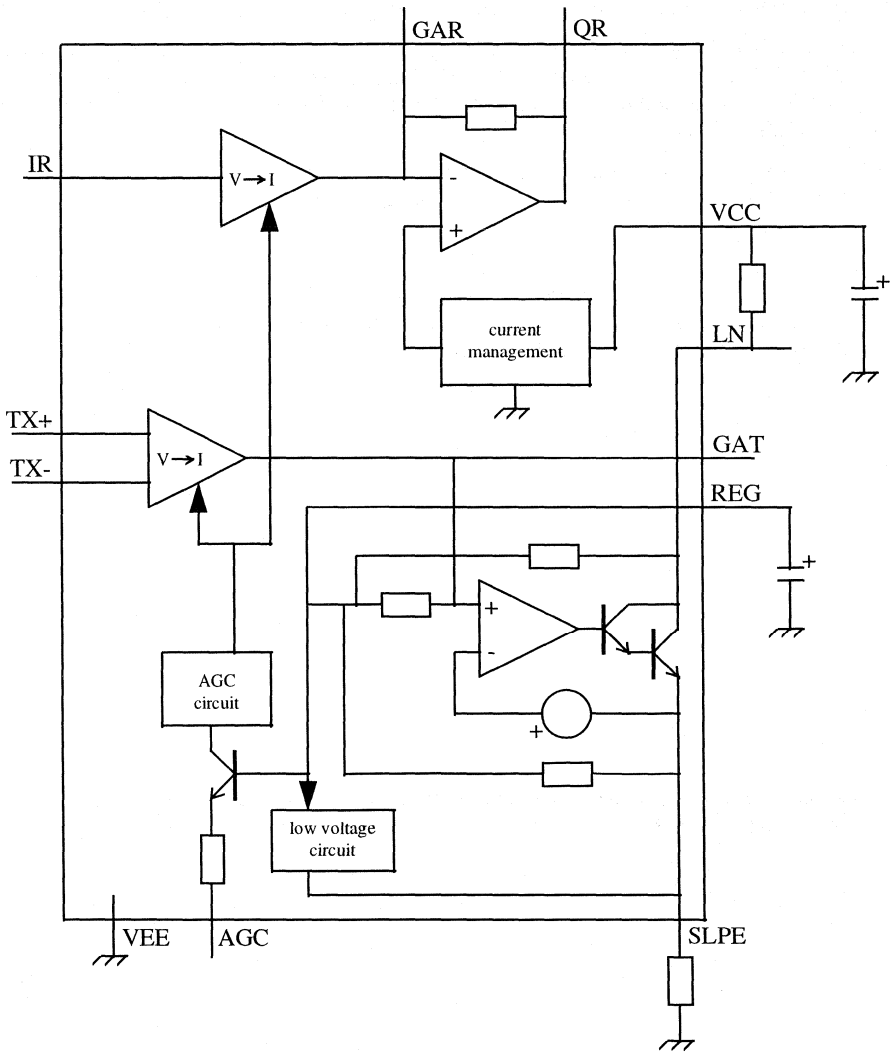


Fig. 1 TEA1118 block diagram

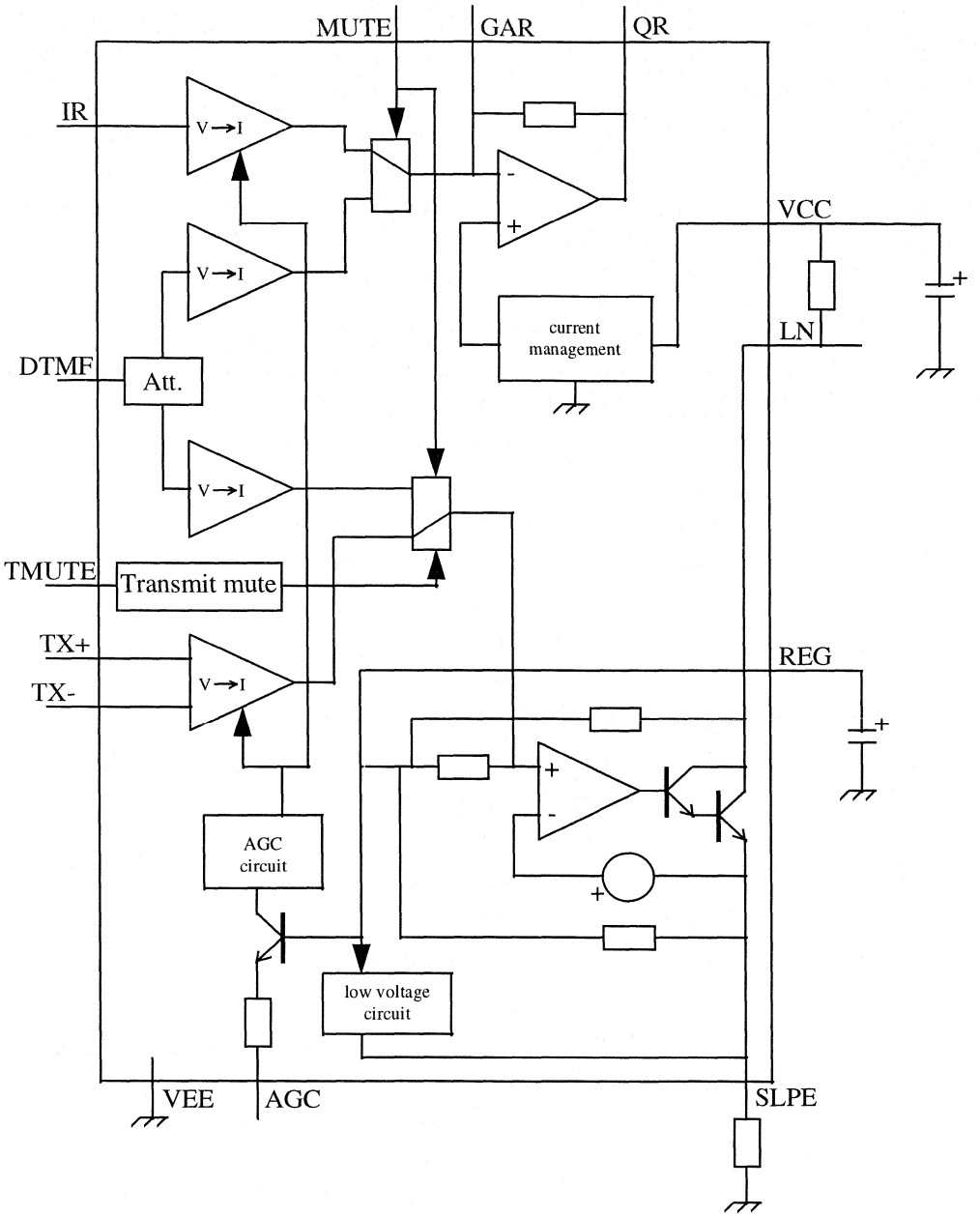


Fig. 2 TEA1118A block diagram

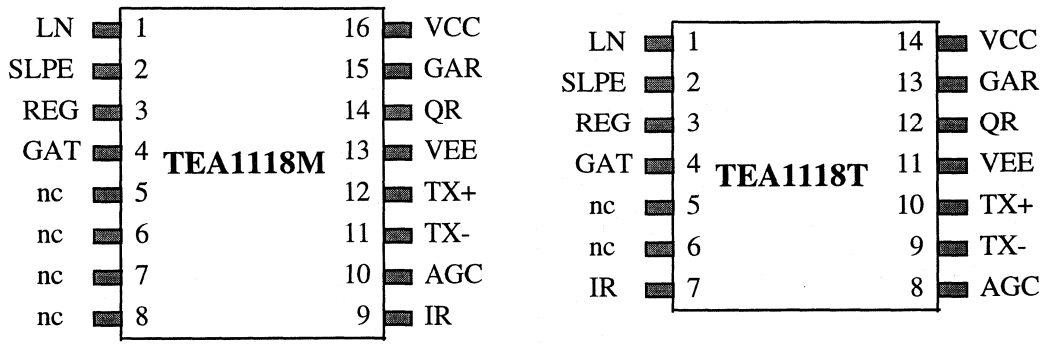


Fig. 3 TEA1118 pinnings

TEA1118M PIN	TEA1118T PIN	NAME	DESCRIPTION
1	1	LN	Positive line terminal
2	2	SLPE	Slope adjustment
3	3	REG	Line voltage regulator decoupling
4	4	GAT	Transmit gain reduction adjustment
5	5	nc	Not connected
6	6	nc	Not connected
7		nc	Not connected
8		nc	Not connected
9	7	IR	Receive amplifier input
10	8	AGC	Automatic gain control
11	9	TX-	Inverting transmit input
12	10	TX+	Non inverting transmit input
13	11	VEE	Negative line terminal
14	12	QR	Receive amplifier output
15	13	GAR	Receive gain reduction adjustment
16	14	VCC	Supply voltage for speech and peripherals

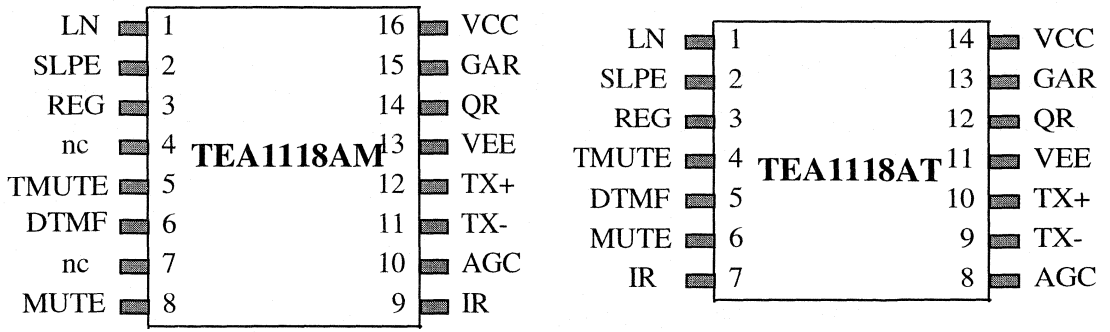


Fig. 4 TEA1118A pinnings

TEA1118AM PIN	TEA1118AT PIN	NAME	DESCRIPTION
1	1	LN	Positive line terminal
2	2	SLPE	Slope adjustment
3	3	REG	Line voltage regulator decoupling
4		nc	Not connected
5	4	TMUTE	Transmit mute input
6	5	DTMF	Dual-tone multifrequency input
7		nc	Not connected
8	6	MUTE	Mute input
9	7	IR	Receive amplifier input
10	8	AGC	Automatic gain control
11	9	TX-	Inverting transmit input
12	10	TX+	Non inverting transmit input
13	11	VEE	Negative line terminal
14	12	QR	Receive amplifier output
15	13	GAR	Receive gain reduction adjustment
16	14	VCC	Supply voltage for speech and peripherals

3. DESCRIPTION OF THE TEA1118/A

All the curves shown in this section result from measurement of typical samples. All the component names refer to the basic application of the ICs shown in fig. 5.

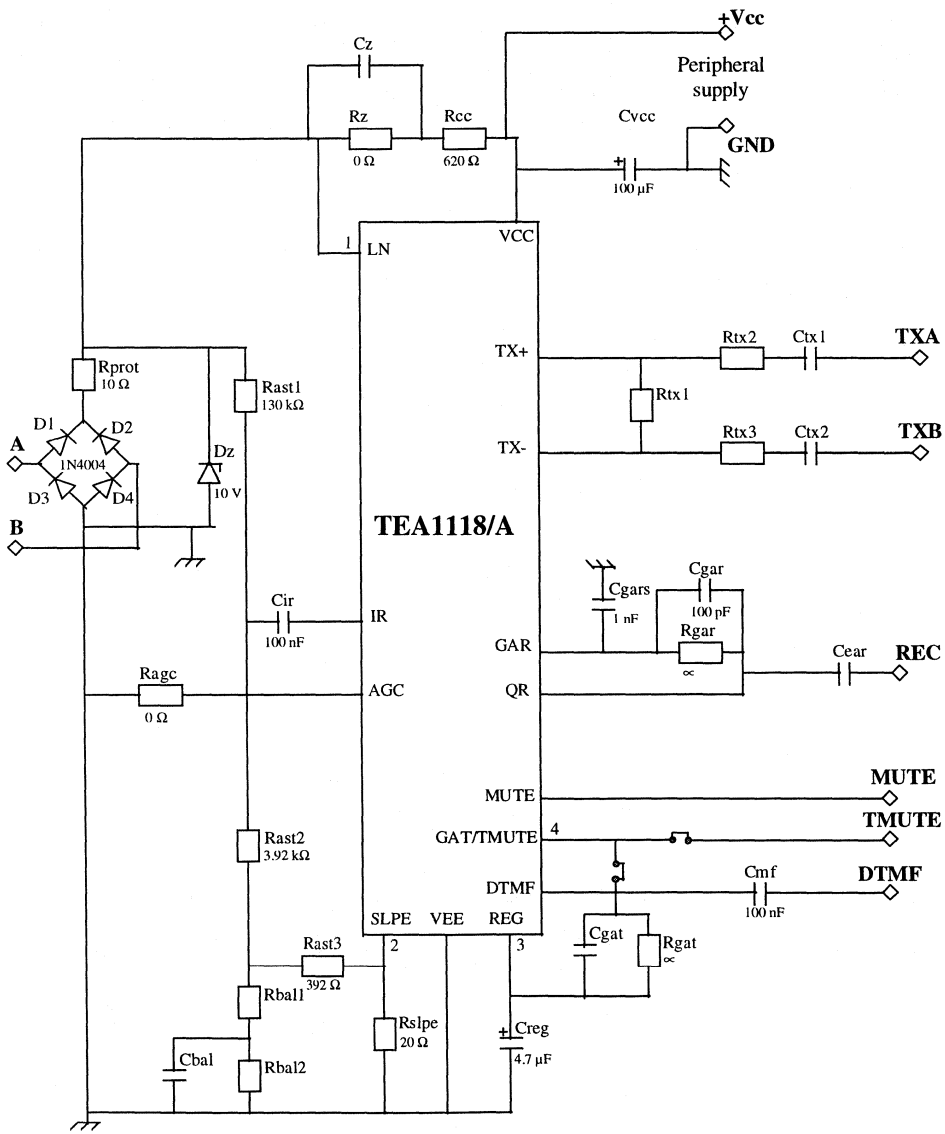


Fig. 5 Basic application for measurements

3.1 DC characteristics and supply block

Without influence on the DC characteristics (except a slight difference at very low line current), the TEA1118/A can be used in two different supply configurations: they can provide supply to peripheral circuits like any IC from the TEA111x family of line interfaces or they can be externally supplied if an external power supply is available.

3.1.1 DC characteristics

Principle of operation

The ICs generate a stabilized voltage (called Vref) between pins LN and SLPE. This reference voltage, typically 3.35 V, is temperature compensated. The voltage at pin REG is used by the internal regulator to generate the stabilized Vref voltage and is decoupled by a capacitor Creg connected to VEE.

For effective operation of the apparatus, the TEA1118/A must have a low resistance to the DC current and a high impedance to speech signals. The Creg capacitor, converted into an equivalent inductance (see "set impedance" section), realizes this impedance conversion from its DC value (Rslpe) to its AC value (Rcc +Rz//Cz in the audio frequency range). The DC voltage at pin SLPE is proportional to the line current.

This general configuration is shown in fig. 6.

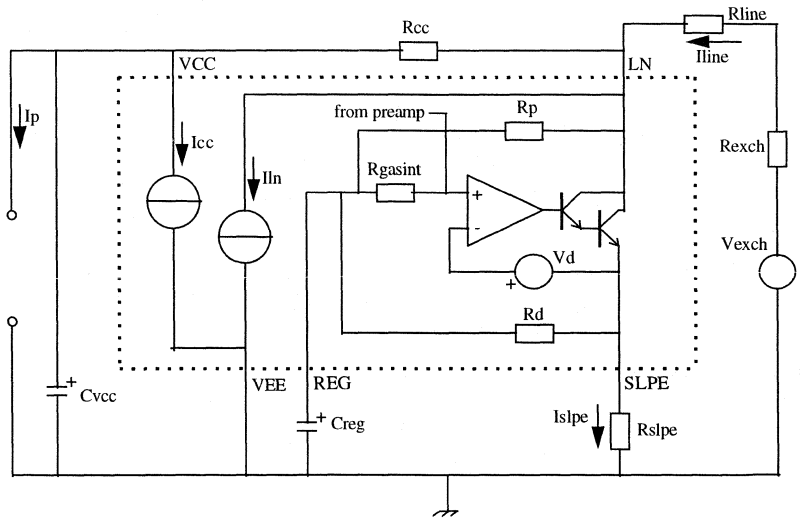


Fig. 6 DC characteristics configuration

The ICs regulate the line voltage between pins LN and SLPE. the voltage on pin LN can be calculated as:

Vln = Vref + Rslpe × Islpe

Islpe = Iline - Icc - Ip - Iln

Iline = line current

Icc = current consumption of the IC

Ip = supply current for peripherals

Iln = Current consumption between LN and VEE

The DC line current Iline flowing into the apparatus is determined by the exchange supply voltage Vexch, the feeding bridge resistance Rexch, the DC resistance of the telephone line Rline and the voltage across the apparatus including diode bridge.

Below a threshold line current Ith (typically equal to 7.5 mA) the internal reference voltage (generating Vref) is automatically adjusted to a lower value (down to an absolute minimum voltage of 1.6 V). In this range, the shape of the curve giving Vref versus line current is slightly different if VCC is used to supply peripheral circuits or if the TEA1118/A are supplied from external supply. This means that more sets can operate in parallel or that for very low voltage feeding bridge the line current has a higher value. For line currents below this threshold current, the TEA1118/A has reduced sending and receiving performances. This is called the low voltage area.

The internal circuitry of the TEA1118/A is supplied from pin VCC. In line powered application, this voltage is derived from the line voltage by means of a resistor (Rcc) and must be decoupled by a capacitor (Cvcc). Fig. 7 shows the IC current consumption (Icc) as a function of the VCC supply voltage.

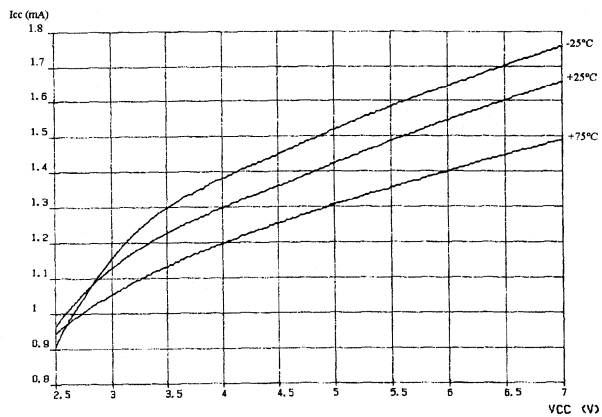


Fig. 7 Icc versus VCC

Fig. 8 shows the main voltages as a function of the line current.

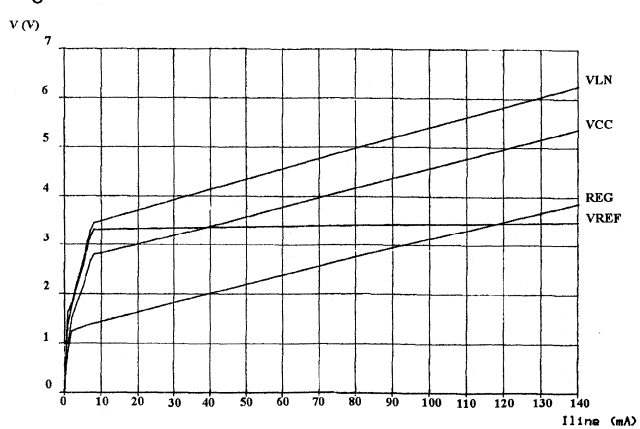


Fig. 8 Main voltages versus line current

Fig. 9 shows the behavior in the low voltage area in line powered condition while fig. 10 shows this behavior when the ICs are externally powered.

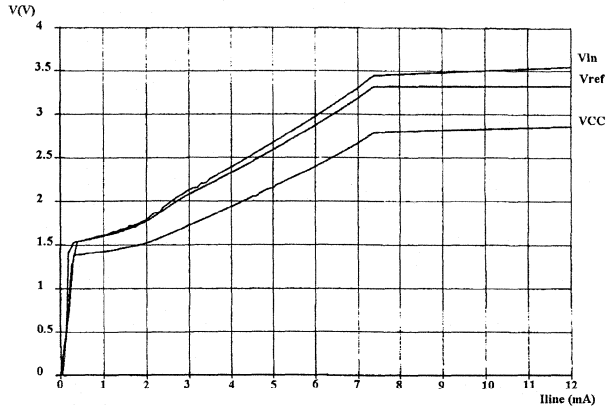


Fig. 9 Low voltage behavior in line powered conditions

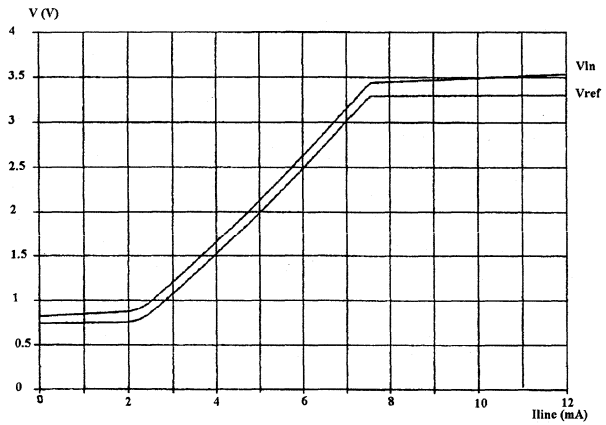


Fig. 10 Low voltage behavior with external 3.3 V power supply

Adjustments and performances

The reference voltage, Vref, can be adjusted by means of an external resistor Rva. It can be increased by connecting the Rva resistor between pins REG and SLPE (see fig; 11), or decreased by connecting the Rva resistor between pins REG and LN. In case of line powered application, it is not recommended to use the voltage reduction because it reduces the peripheral supply capability. To ensure correct operation, it is not advised to adjust Vref at a value lower than 3 V or higher than 7 V (the maximum operating voltage of 12 V must be guaranteed by the application). These adjustments will slightly affect a few parameters: there will be a small change in the temperature coefficient of Vref and a slight increase in the spread of this voltage reference due to matching between internal and external resistors. Furthermore, the Rva resistor connected between REG and LN will slightly affect the apparatus impedance(see section "set impedance").

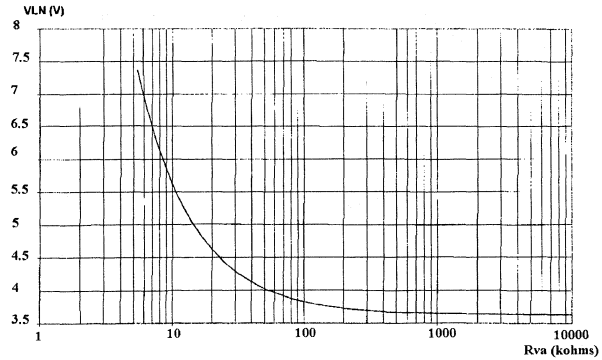


Fig. 11 Influence of an Rva resistor between REG and SLPE on Vln at 15mA

The DC slope of the voltage on pin LN is influenced by the Rslpe resistor as shown in fig. 12. The preferred value for Rslpe is 20 Ω, changing this value will affect more than the DC characteristics, it also influences the gains, the AGC characteristics, the maximum output swing on the line and the low voltage threshold Ith.

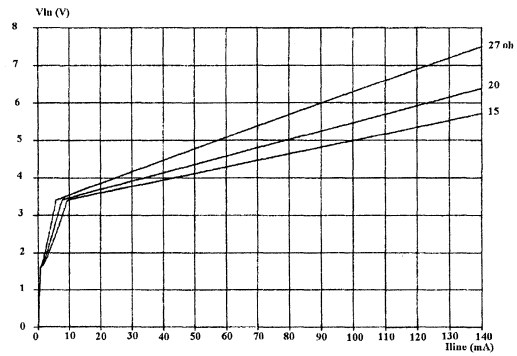


Fig. 12 Influence of Rslpe on the DC characteristics

3.1.2 Supply for peripherals

This sub-chapter concerns line powered applications which may not be usual for these ICs.

Principle of operation

The supply voltage at pin VCC is normally used to supply the internal circuitry of the TEA1118/A. However, a small current can be drawn to supply peripheral circuits having VEE as ground reference. The VCC supply voltage depends on the current consumed by the IC and the peripheral circuits as shown by the following formula:

$$VCC = VCC0 - Rccint \times (Iqr + Ip)$$

$$VCC0 = VLN - Rcc \times Icc$$

Iqr = internal current necessary to supply the receive output amplifier when there is AC signal

Rccint = Rcc // internal equivalent impedance between VCC and VEE

Rccint is the output impedance of the voltage supply point. As can be seen from fig. 7, the internal supply current Icc depends on the voltage on the pin VCC, it means that the impedance of the internal circuitry connected between VCC and VEE is not infinite. While supplying a peripheral circuit on VCC, the Ip supply current flowing through the Rcc resistor decreases the value of the voltage on the pin VCC and then reduces the Icc consumption. So, the impedance to use in combination with Ip and Iqr is not Rcc but Rccint which include in parallel the impedance of the internal circuitry connected between VCC and VEE. For a line current equal to 15 mA and Rcc equal to 620 Ω, this Rccint impedance is 550 Ω.

As VCC is limited to a minimum value to ensure correct operation, Ip will be limited to a maximum value.

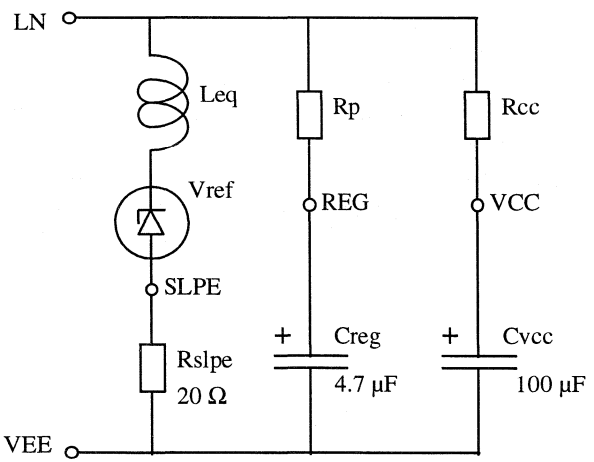
Adjustments and performances

As the impedance connected between LN and VCC also determines the set impedance, the easiest way to increase the current capability of the supply point VCC is to increase the reference voltage Vref by connecting a resistor Rva between pins REG and SLPE (see 3.1.1).

3.2 Set impedance

Principle of operation

The ICs behave like an equivalent inductance that presents a low impedance to DC (Rslpe) and a high impedance (Rp) to speech signals. Rp is an integrated resistance in the order of 15.5 kΩ +/-15%. It is in parallel with the external RC realized by Rcc and Cvcc. Thus, in the audio frequency range, the apparatus impedance (called set impedance) is mainly determined by the Rcc resistor. Fig. 13 shows an equivalent schematic for the set impedance.



Leq = Creg x Rslpe x Rp
Rp = internal resistor

Fig. 13 Equivalent set impedance

Adjustments and performances

When decreasing the reference voltage Vref, a resistor is connected between LN and REG in parallel of Rp (see fig. 13) so, slightly modifying the impedance.

If complex set impedance is required, the Rcc resistor resistor is replaced by a complex network (see fig. 5 :Rcc + Rz // Cz). The DC resistance which influences the value of VCC becomes Rcc + Rz.

3.3 Transmit amplifier

Principle of operation

In fig. 14, the block diagram of the transmit amplifier of the TEA1118/A is depicted.

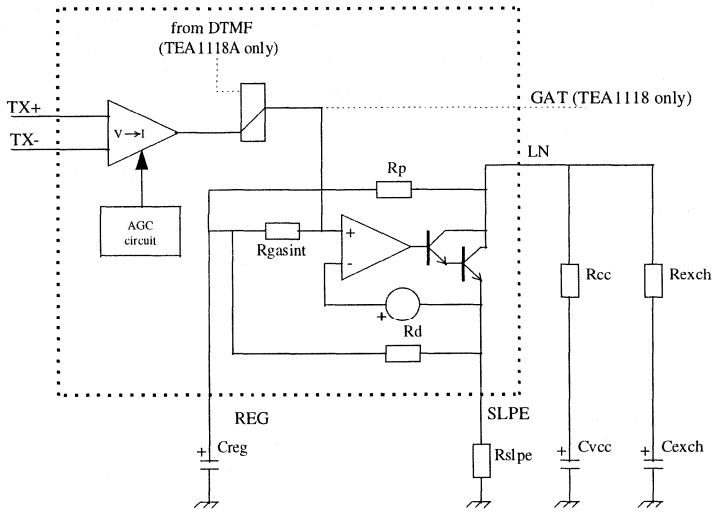


Fig. 14 Transmit channel

The transmit amplifier has symmetrical high input impedances (typically 64 kΩ -2 times 32 kΩ- between pins TX+ and TX- with maximum tolerances of +/- 15%). The input of this transmit amplifier is able to handle AC signals up 900 mVrms with less than 2% total harmonic distortion.

As can be seen from fig. 14, the transmit amplifier itself is built up out of two parts: a preamplifier which realizes a voltage to current conversion, and an end-amplifier which realizes the current to voltage conversion. The overall gain (Gvtx) of the transmit amplifier from inputs TX+/TX- to output LN is given by the following equation:

$$Gvtx = 20 \times \log Avtx$$

$$Avtx = 0.016 \times (Rgasint / Rrefint) \times (Ri//Zline / Rslpe) \times \alpha$$

with:

Ri = the AC apparatus impedance, Rcc//Rp (typically 620 Ω // 15.5 kΩ)

Rgasint = internal resistor realizing the current to voltage conversion (typically 27.6 kΩ with a spread of +/-15%)

Rrefint = internal resistor determining the current of an internal current stabilizer (typically 3.4 kΩ with a spread of +/- 15% correlated to the spread of Rgasint)

Zline = load impedance of the line during the measurement

α = gain control factor varying from 1 at Iline = 15 mA to 0.5 at Iline = 75 mA when AGC function is applied (see chapter 3.6 for details)

Using these typical values in the equation and assuming Zline = 600 Ω, we find a gain equal to:

$$Gvtx = 20 \times \log Avtx = 11\ dB \quad \text{at } Iline = 15\ mA$$

The different gain controls (AGC; MUTE and TMUTE for TEA1118A only) act on the transmit preamplifier stage, modifying its transconductance.

Adjustments and performances

On the **TEA1118 only**, the transmit gain can be decreased by connecting a resistor Rgat between pins GAT and REG. It can be adjusted from 11 dB to 5 dB to suit application specific requirements, however, this gain adjustment slightly increases the gain spread and affects the temperature coefficient due to matching between internal and external resistors. Fig. 15 shows the typicall curve of the transmit gain versus the external resistor Rgat. The gain dependancy to this external Rgat resistor is given by the following equation:

$$Gvtx = 20 \times \log [\ 0.016 \times (Rgasint//Rgat\ /\ Rrefint) \times (Ri//Zline\ /\ Rslpe) \times \alpha\ ]$$

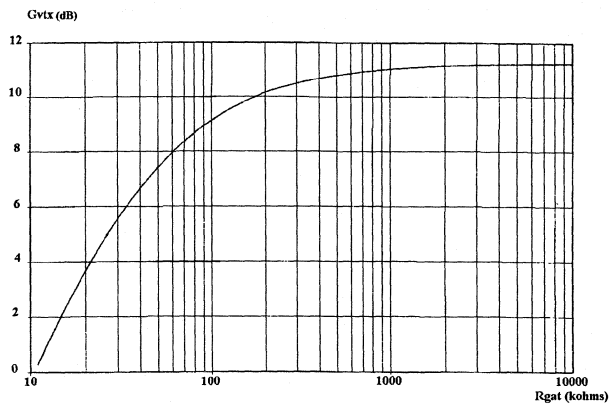


Fig. 15 Transmit gain versus Rgat connected between GAT and REG

A capacitor Cgat can be connected between pins GAT and REG of the TEA1118 to provide a first order low-pass filter which cut-off frequency is determined by the product Cgat × (Rgasint//Rgat). Fig 16 shows the typical frequency response of the transmit amplifier (without filter) of the TEA1118/A.

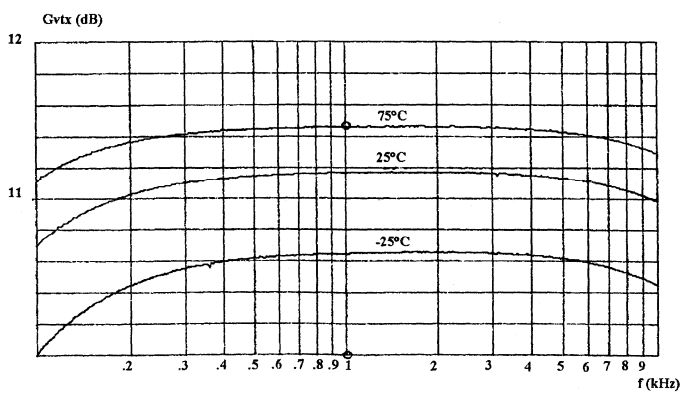


Fig. 16 Transmit gain versus frequency: influence of temperature

Fig 17 shows the distortion of the signal on the line as a function of the transmit signal at nominal DC settings and for a line current of 15 mA for TEA1118/A, while fig. 18 shows this distortion versus the input transmit signal when the transmit gain is reduced to 5 dB on the TEA1118.

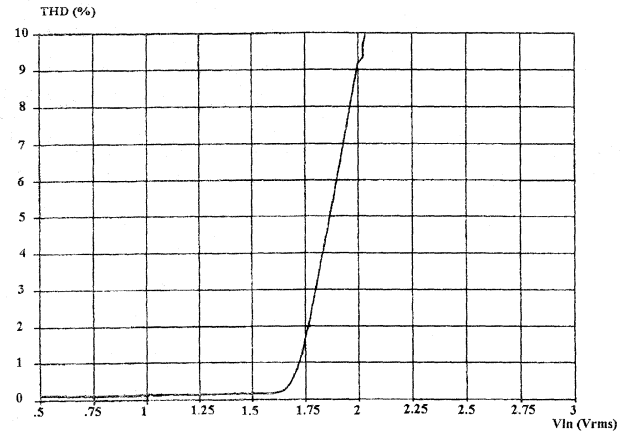


Fig. 17 Distortion on line versus transmit signal at nominal gain on TEA1118/A

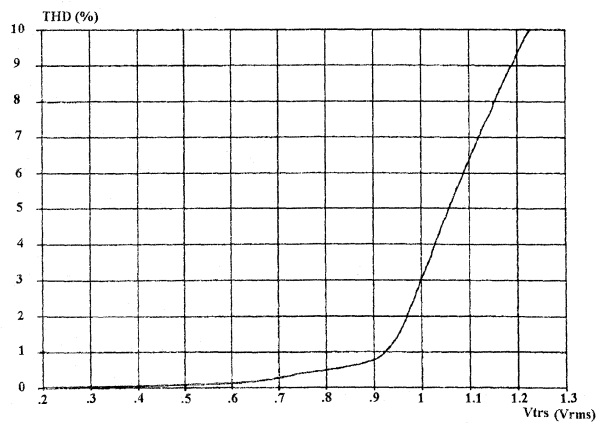


Fig. 18 Distortion on the line versus transmit signal at 5 dB gain on TEA1118

Fig. 19 shows the distortion of the line signal versus the input transmit signal on the line at line current of 4 mA and nominal gain when the TEA1118/A are powered from an external 3.3 V power supply between VCC and VEE.

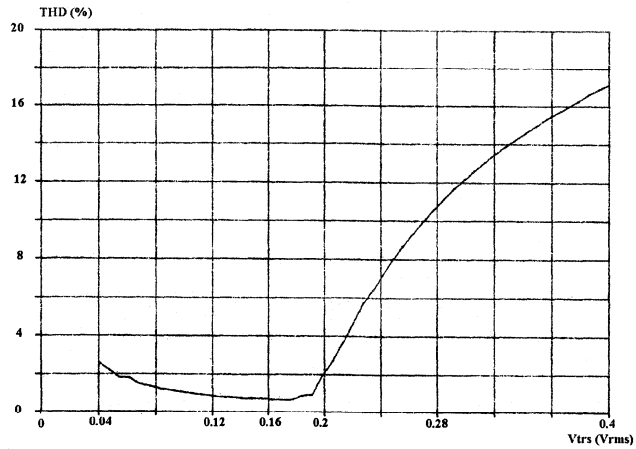


Fig. 19 Distortion of line signal at Iline = 4 mA with external 3.3 V power supply

Fig. 20 shows the transmit noise (psophometrically weighted: P53 curve) versus line current at nominal gain when a 200 Ω resistor is connected between the inputs TX+ and TX-.

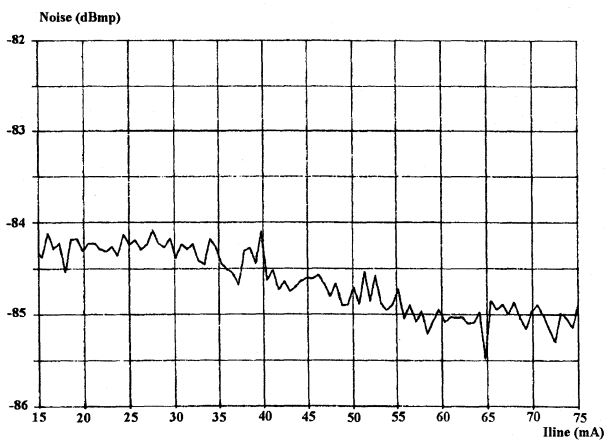


Fig. 20 Transmit noise versus line current

Fig. 21 shows the common mode rejection ratio at 15 mA and at nominal transmit gain. Two curves are present in this fig. 21, the first one is the spectrum of the signal on pin LN when a transmit signal is applied on pin TX- while pin TX+ is shorted to VEE, the second one is the spectrum of the signal on pin LN when a transmit signal is applied on pins TX- and TX+ shorted together. Both signals are at 1 kHz, the difference between the two curves gives the CMRR.

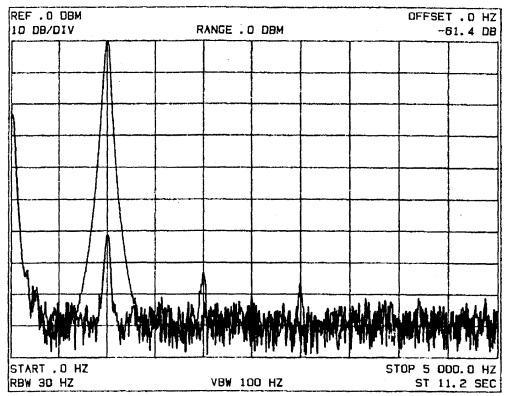


Fig. 21 Common mode rejection ratio on transmit

3.4 TMUTE function (TEA1118A only)

Principle of operation

The transmit mute function realizes an electronic switching between the transmit amplifier and the sending DTMF amplifier. This function disables the transmit channel to provide a kind of privacy function and at the same time enables the DTMF channel if needed for some specific applications; this function has no effect on the receive channel. If a high level is applied to the TMUTE input, the transmit channel is disabled while the DTMF channel is enabled, by applying a low level or leaving pin TMUTE open (if MUTE pin level is low) the transmit channel is enabled. The threshold voltage level is 0.68 V typically with a temperature coefficient of -2 mV/°C. Fig. 22 shows the transmit gain reduction and TMUTE input current versus TMUTE input voltage.

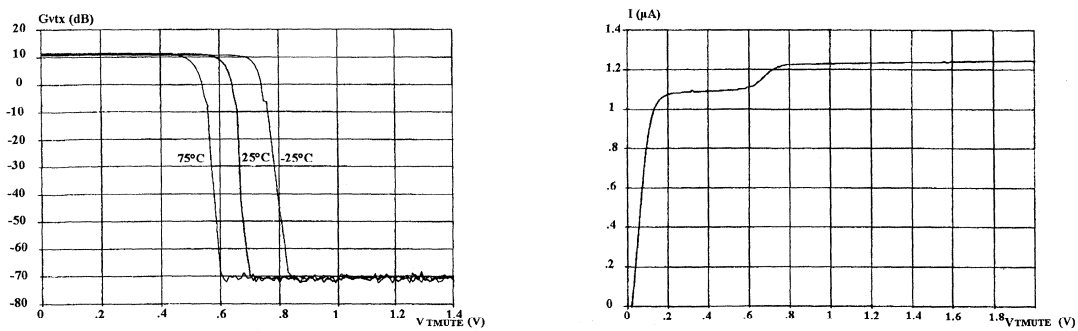


Fig. 22 Transmit gain and TMUTE input current versus TMUTE input voltage

Adjustment and performances

Fig. 23 shows the transmit amplifier gain reduction at Iline = 15 mA for an input signal of 1 kHz. Two curves are present on this fig. 23, the first one shows the spectrum of the signal on the line when a signal is applied on the transmit inputs and when TMUTE is at a low level, the second one shows the same signal when pin TMUTE is at a high level. The difference between the two curves at this frequency gives the gain reduction.

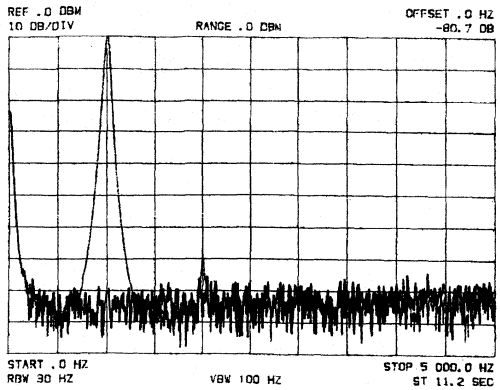


Fig. 23 Transmit gain reduction in TMUTE condition

The TMUTE function works down to a voltage on VCC equal to 1.6 V, below this threshold, the transmit amplifier stays always enabled independently of the TMUTE input level. The maximum voltage allowed at pin TMUTE is VCC +0.4 V.

3.5 Receive amplifier

Principle of operation

In fig. 24, the block diagram of the receive amplifier is depicted.

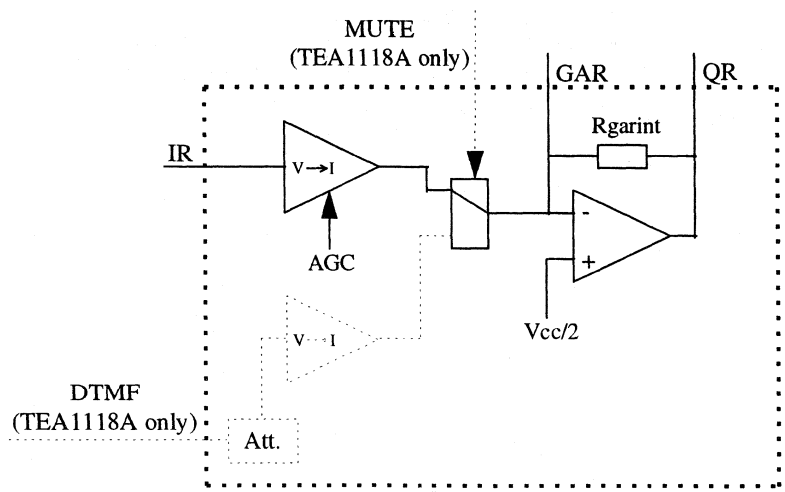


Fig. 24 Receive channel

The receive amplifier has an a-symmetrical high input impedance between pins IR and VEE. It is equal to 20 kΩ with a maximum tolerance of +/-15%. The ICs are able to drive loads down to an impedance of 150 Ω. As can be seen from fig. 24, the receive amplifier itself is built up out of two parts: a preamplifier which realizes a voltage to current conversion and an end-amplifier which realizes the current to voltage conversion. The overall gain Gvrx of the receive amplifier from input IR to output QR is given by the equation:

$$Gvrx = 20 \times \log Avrx$$

$$Avrx = \alpha \times 1.21 \times Rgarint/Rrefint$$

with:

Rgarint = internal resistor realizing the current to voltage conversion (typically 100 kΩ with a spread of +/-15%)

Rrefint = internal resistor determining the current of an internal current stabilizer (typically 3.4 kΩ with a spread of +/- 15% correlated to the spread of Rgasint)

α = gain control factor varying from 1 at Iline = 15 mA to 0.5 at Iline = 75 mA when AGC function is applied (see chapter 3.6 for details)

Using these typical values in the equation, we find a gain equal to:

$$Gvrx = 20 \times \log Avrx = 31 \text{ dB} \quad \text{at Iline} = 15 \text{ mA}$$

The different gain controls (AGC; MUTE for TEA1118A only) act on the receive preamplifier stage, modifying its transconductance.

Adjustments and performances

The receive gain can be decreased on the TEA1118/A by connecting a resistor Rgar between pins GAR and QR. It can be decreased from 31 dB down to 19 dB to suit application specific requirements, however, this gain adjustment slightly increases the gain spread and affects the temperature coefficient due to matching between internal and external resistors. 31 dB of receive gain compensate almost typically the attenuation provided by the antisidetone network. Fig. 25 shows the typicall curve of the receive gain versus the external resistor Rgar. The gain dependancy to this external Rgar resistor is given by the following equation:

$$Gvrx = 20 \times \log [\ 1.21 \times (Rgarint//Rgar\ /\ Rrefint) \times \alpha\ ]$$

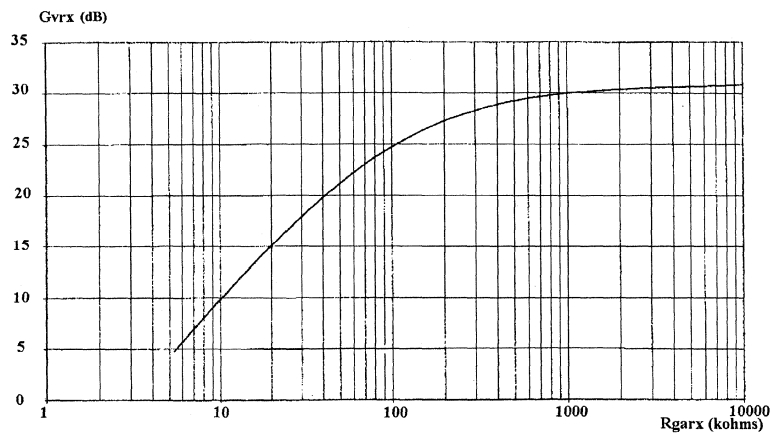


Fig. 25 Receive gain versus Rgar connected between GAR and QR

Two external capacitors Cgar (connected between GAR and QR) and Cgars (connected between GAR and VEE) ensure stability when the relationship Cgars ≥ 10 × Cgar is fulfilled. The Cgar capacitor provides a first order low pass filter, which cut-off frequency is determined with Rgarint//Rgar. Fig. 26 shows the frequency response of the receive amplifier at different temperatures (Cgar = 100 pF, Cgars = 1 nF).

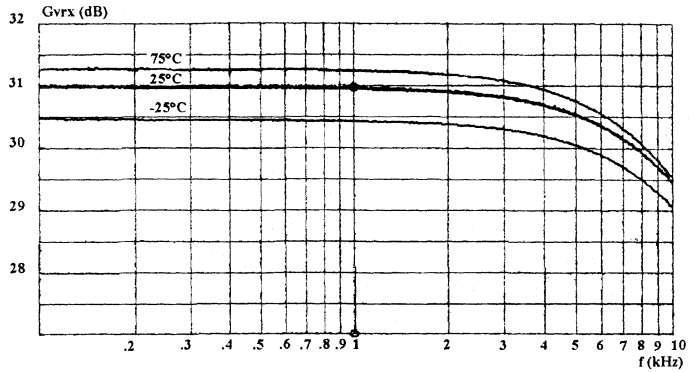


Fig. 26 Receive gain versus frequency and temperature

The maximum output swing on QR depends on the DC line voltage, the Rcc resistor, the Icc current consumption of the circuit, the Ip current consumption of the peripheral circuits and the load impedance on QR. The receiving input IR can handle signals up to 18 mVrms with less than 2% THD. Fig. 27 shows the distortion on QR when the limitation is related to the input voltage for a line current equal to 75 mA. Fig. 28 shows the distortion of the signal on QR as a function of the rms signal on QR with a load of 450 Ω and a line current of 15 mA.

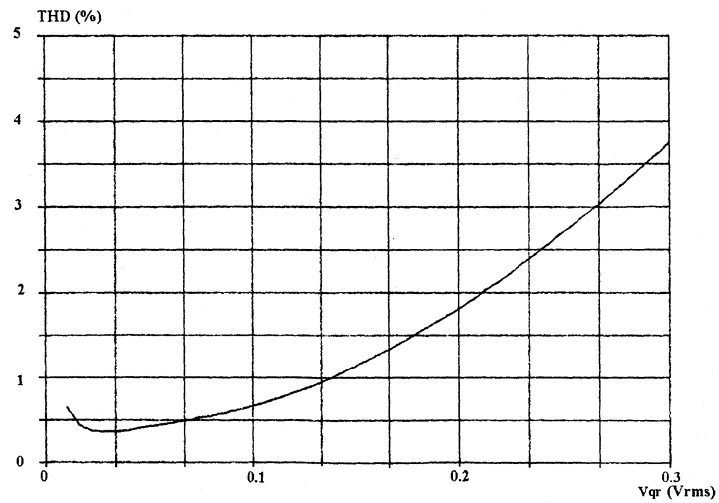


Fig. 27 Distortion on QR versus input signal on IR

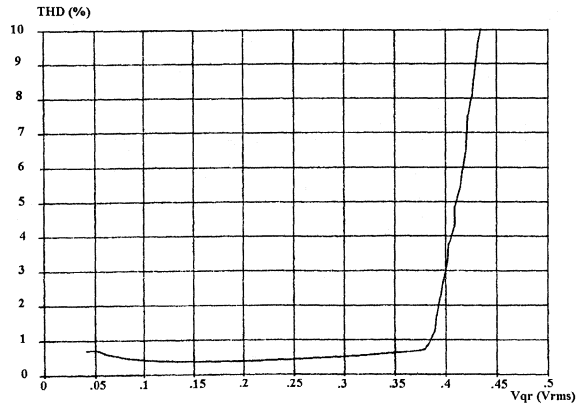


Fig. 28 Distortion on QR versus level with 450 Ω load

Fig. 29 shows the noise on QR loaded with 150 Ω (psophometrically weighted: P53 curve) as a function of the line current. This curve has been done with an open input IR. With the antisidetone network connected to the input IR, part of the transmit noise generated on the line will be added but, thanks to the low transmit noise value, the effect is negligible.

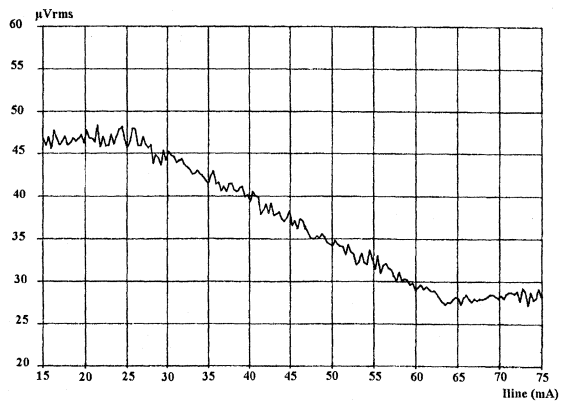


Fig. 29 Noise on QR

3.6 Automatic gain control

Principle of operation

The TEA1118/A perform automatic line loss compensation. The automatic gain control varies the gain of the transmit and receive amplifiers in accordance with the DC line current. To enable this AGC function, the pin AGC must be connected to the pin VEE. For line currents below a current threshold, Istart (typically 25 mA), the gain control factor α is equal to 1, giving the maximum value to the gains Gvtx and Gvrx. If this threshold

current is exceeded, the gain control factor α is reduced and then the gains of the controlled transmit and receive amplifiers are also reduced. When the line current reaches an other threshold current, Istop (typically 63 mA), the gain control factor α is limited to its minimum value equal to 0.5, giving the lower value to the transmit and receive controlled gains. The gain control range of both amplifiers is typically 5.8 dB, which corresponds to a line length of 5 km (0.5 mm twisted pair copper) with an attenuation of 1.2 dB/km.

The attenuation is correlated to the current Iagc sunk at pin AGC: when this current is lower than typically 5 µA the gains are maximum, when this current is higher than typically 13 µA the gains are minimum. This current is proportional to the voltage between pins SLPE and VEE. There is an internal resistor which sets Istart and Istop, adding one externally in series (between pins AGC and VEE) reduces Iagc and increases the values of Istart and Istop.

Adjustments and performances

The ICs are optimized for use with an exchange supply voltage of 48 V, a feeding bridge of $2 \times 300\ \Omega$ and the line previously described. In order to fit with other configurations, a resistor Ragc, can be inserted between pins AGC and VEE. This Ragc resistor increases the two threshold currents Istart and Istop. Fig. 30 shows the control of the transmit gain versus the line current for different values of Ragc. When no AGC function is required, the AGC pin must be left open, then the control factor α equals to 1 and both controlled gains are at their maximum values.

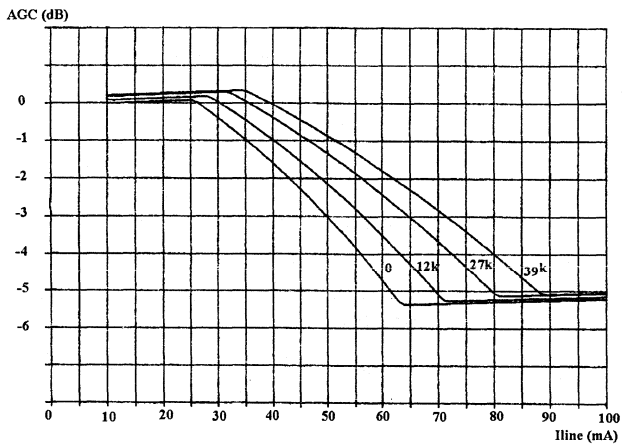


Fig. 30 AGC on the transmit gain versus line current and Ragc

3.7 DTMF amplifier (TEA1118A only)

principle of operation

In fig. 31, the block diagram of the DTMF channel of the TEA1118A is depicted.

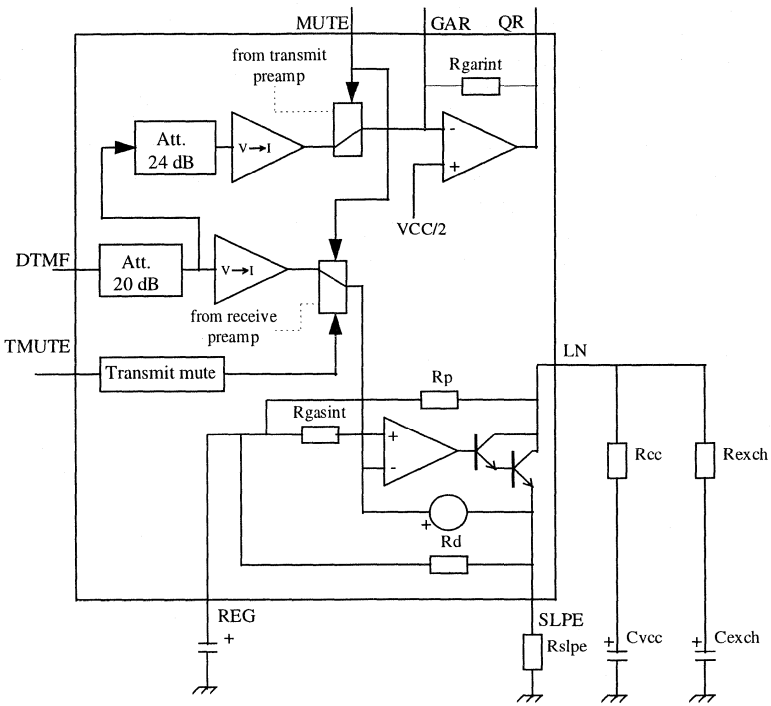


Fig. 31 DTMF channel of the TEA1118A

The DTMF amplifier has an a-symmetrical high input impedance of 20 kΩ between pins DTMF and VEE with a maximum spread of +/-15%. The DTMF amplifier is built up out of three parts: an attenuator by a factor of 10, a preamplifier which realizes the voltage to current conversion and the same end-amplifier as the transmit amplifier. No AGC is applied to the DTMF channel. The overall gain (Gvmf) of the DTMF amplifier from input DTMF to output LN is given by the following equation:

$$Gvmf = 20 \times \log Avmf$$

$$Avmf = 0.032 \times (Rgasint / Rrefint) \times (Ri//Zline / Rslpe)$$

with:

Ri = the AC apparatus impedance, Rcc//Rp (typically 620 Ω // 15.5 kΩ)

Rgasint = internal resistor realizing the current to voltage conversion (typically 27.6 kΩ with a spread of +/-15%)

Rrefint = internal resistor determining the current of an internal current stabilizer (typically 3.4 kΩ with a spread of +/- 15% correlated to the spread of Rgasint)

Zline = load impedance of the line during the measurement

Using these typical values in the equation and assuming Zline = 600 Ω, we find a gain equal to:

$$Gvmf = 20 \times \log Avmf = 17.4 \text{ dB}$$

Fig. 32 shows the frequency response of the DTMF amplifier at 15 mA and different temperatures.

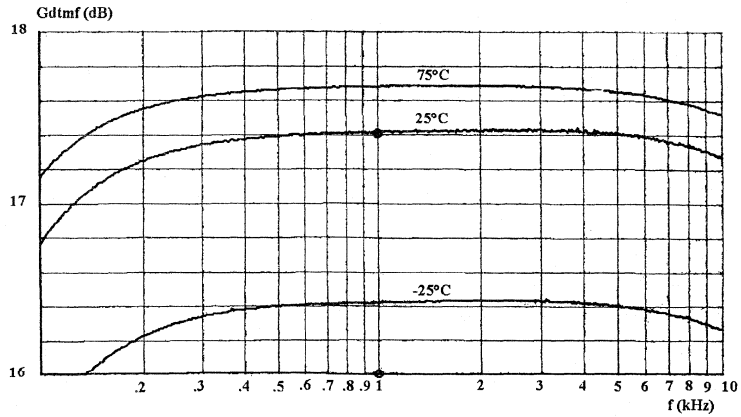


Fig. 32 DTMF gain versus frequency at different temperatures

The input of the DTMF amplifier can handle signals up to 180 mVrms with less than 2% THD. Fig. 33 shows the distortion on line versus the rms input signal at Iline = 15 mA.

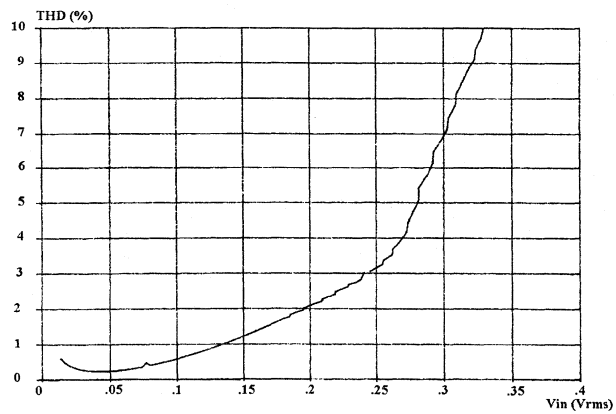


Fig. 33 Distortion of the DTMF signal on line versus input signal

3.8 MUTE function (TEA1118A only)

Principle of operation

The mute realizes an electronic switching between the speech mode and the dialling mode. If a high level is applied to the MUTE input, both the transmit and the receive channels are disabled while the DTMF channel is enabled. By applying a low level or leaving pin MUTE open the receive channel is enabled moreover, if TMUTE pin level is low, the transmit channel is also enabled. The threshold voltage level is 0.68 V typically with a

temperature coefficient of -2 mV/°C. Fig. 34 shows the transmit gain reduction and MUTE input current versus MUTE input voltage.

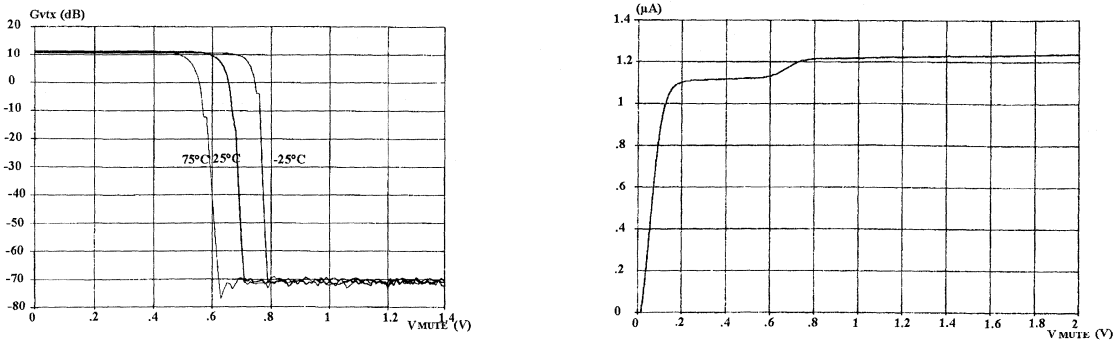


Fig. 34 Transmit gain and MUTE input current versus MUTE input voltage

Adjustments and performances

Fig. 35 shows the transmit and receive amplifier gain reduction at Iline = 15 mA for an input signal of 1 kHz. Two curves are present on these graphics, the first one shows the spectrum of the signal on the line (or on QR) when a signal is applied on the transmit inputs (or respectively on IR) and when MUTE is at a low level, the second one shows the same signal when pin MUTE is at a high level. The difference between the two curves at this frequency gives the gain reduction.

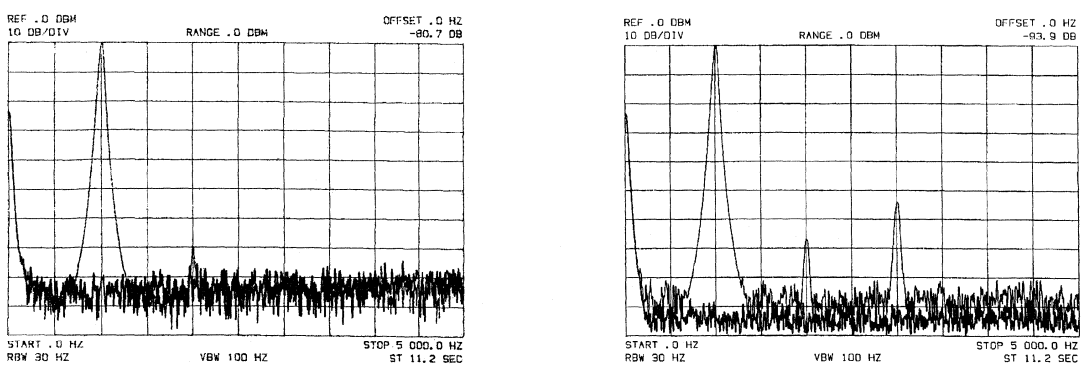


Fig. 35 Transmit and receive gain reduction in MUTE condition on the TEA1118A

The MUTE function works down to a voltage on VCC equal to 1.6 V, below this threshold, the transmit and receive amplifiers stays always enabled independently of the MUTE input level. The maximum voltage allowed at the MUTE input is VCC + 0.4 V.

3.9 Anti-sidetone network

Principle of operation

To avoid the transmit signal to come back with a too high level in the receive channel, the anti-sidetone circuit uses the transmit signal from pin SLPE (which is in opposite phase) to cancel the transmit signal at the IR input of the receive amplifier. The anti-sidetone bridge already used for the TEA106x or the TEA111x families or a conventional Wheatstone bridge as shown in fig. 36 may be used for the design of the anti-sidetone network.

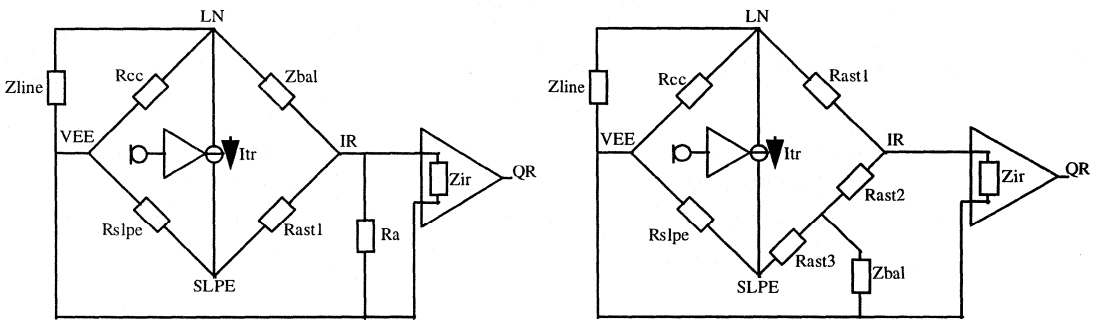


Fig. 36 Wheatstone bridge (left) and TEA106x orTEA111x family anti-sidetone bridge (right)

The TEA106x or TEA111x family anti-sidetone bridge has the advantage of a relative flat transfer function in the audio frequency range between the input IR and the output QR, both with real and complex set impedances. Furthermore, the attenuation of the bridge for the receive signal (between pins LN and IR) is independent of the value chosen for Zbal after the set impedance has been fixed and the condition shown in equation (6) is fulfilled. Therefore, readjustment of the overall receive gain is not necessary in many cases.

Compare to the previous one the Wheatstone bridge has the advantages of needing one resistor less and a smaller capacitor in Zbal. But the disadvantages include the dependence of the attenuation of the bridge on the value chosen for Zbal and the frequency dependence of that attenuation. This requires some readjustment of the overall receive gain.

3.9.1 TEA106x or TEA111x family bridge

The anti-sidetone circuit is composed of: Rcc//Zline, Rast1, Rast2, Rast3, Rslpe and Zbal. Maximum compensation is obtained when the following conditions are fulfilled:

$$Rslpe \times Rast1 = Rcc \times (Rast2 + Rast3) \quad (6)$$

$$k = [Rast2 \times (Rast3 + Rslpe)] / (Rast1 \times Rslpe)$$

$$Zbal = k \times Zline$$

The scale factor k is chosen to meet the compatibility with a standard value of capacitor for Zbal.

In practice, Zline varies strongly with line lenght and line type. Consequently, the value for Zbal has to be chosen to fit with an average line length giving acceptable sidetone suppression with short and long lines. The suppression further depends on the accuracy with which Zbal equals this average line impedance.

Example

Let's optimize for a theorical equivalent average line impedance shown in Fig. 37.

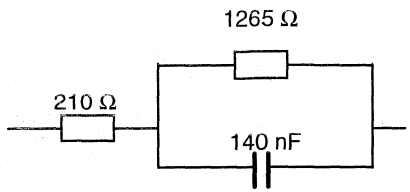


Fig. 37 Equivalent average line impedance

For compatibility of the capacitor value in Zbal with a standard capacitor value from the E6 series (220 nF):

$k = 140 / 220 = 0.636$

For Rast2, a value of 3.92 kΩ has been chosen. So, using the previous equations, we can calculate Zbal, Rast1, Rast3. We find Rast1 = 130 kΩ, Rast3 = 390 Ω, and for Zbal 130 Ω in series with 220 nF // 820 Ω.

The attenuation of the receive line signal between LN and IR can be derivated from the following equation:

$$Vir / Vin = (Zir // Rast2) / [Rast1 + (Zir // Rast2)]$$

If Rast2 >> (Rast3 // Zbal).

With the values used in this example, it gives 32 dB at 1 kHz.

Zir is the receive amplifier input impedance, typically 20 kΩ.

3.9.2 Wheatstone bridge

The conditions for optimum suppression are given by:

$Zbal = (Rast1 / Rslpe) \times (Rcc // Zline)$

Also, for this bridge type, a value for Zbal has to be chosen that corresponds with an average line length.

The attenuation of the received line signal between LN and IR is given by:

$$Vir / Vln = (Zir // Rast1 // Ra) / [Zbal + (Zir // Rast1 // Ra)]$$

Ra is used to adjust the bridge attenuation; its value has no influence on the balance of the bridge.

4. APPLICATION COOKBOOK

In this chapter, the procedure for making a basic application is given. Reffering to fig. 38, the design flow is given as a number of steps which should be made. As far as possible for every step, the components involved and their influence on every step are given.

Step	Adjustment
DC setting :	
Adjust the DC setting of the TEA1118/A to the local PTT requirements.	
Voltage LN-VEE	This voltage can be adjusted by changing Vref: increased up to 7 V with a resistor between pins REG and SLPE or decreased down to 3 V with a resistor between REG and LN.
DC slope	The DC slope might be modified by changing the value of Rslpe (this is not advised: all gains are modified, AGC characteristic is modified).
Supply point VCC	In line powered applications, depends on the values of Vref and the resistive part of the impedance network (Rcc + Rz). External power supply can be applied.
Artificial inductor	Its value can be adjusted by changing the value of Creg: a smaller value speeds-up the DC current shape during transients but decreases the value of the inductance and then affects the BRL.
Impedance and sidetone :	
After setting the required set impedance, the sidetone has to be optimized using the sidetone network in order to minimize the loop gain in all line conditions. AGC can be adjusted at that step.	
Application impedance	The BRL is adjusted with the impedance network connected between LN and VCC (Rcc + Rz//Cz).
Sidetone	Adjust Zbal (Rbal1, Rbal2, Cbal) according to the line characteristics.
AGC	Internally defined, the characteristics (Istart and Istop) can be shiftted to higher line currents with an external Ragc resistor connected between AGC and VEE.

Step	Adjustment
TEA1118/A transmit and receive gains	
Transmit gain	The transmit gain of the application has to be adjusted preferably before entering pins TX+/TX- for the TEA1118/A. For the TEA1118 only, it is also possible to reduce the transmit gain with the resistor Rgat. Ctx1, Ctx2 and TX+/TX- input impedance form a high-pass filter. A capacitor Cgat in parallel with the transmit gain resistor (between TEA1118 pins REG and GAT) form a low-pass filter.
Receive gain	The receive gain of the application has to be adjusted preferably after the output QR, nevertheless, it is possible to reduce the receive gain with the resistor Rgar. A capacitor in parallel with the receive gain resistor (between TEA1118/A pins QR and GAR) form a low-pass filter, stability is ensured with capacitor Cgars (>10 × Cgar) between pins GAR and VEE.
TEA1118A only DTMF gain	
DTMF	The DTMF level on line must be adjusted before entering pin DTMF. It is selected with a high level either on pin TMUTE or on pin MUTE.

5. EXAMPLE OF APPLICATION

A demo board (OM4789) is available, as the TEA1118/A may be used in various applications, this demo board includes only the TEA1118A with its basic environment. Replacing the TEA1118A by a TEA1118 may make it usable also for the evaluation of the TEA1118 which offers the possibility to reduce the transmit gain.

Fig. 38 gives the basic application of the TEA1118/A. On this schematic, the capacitors connected with doted lines and the resistors drawn with dotted lines are indicated for RFI immunity purpose.

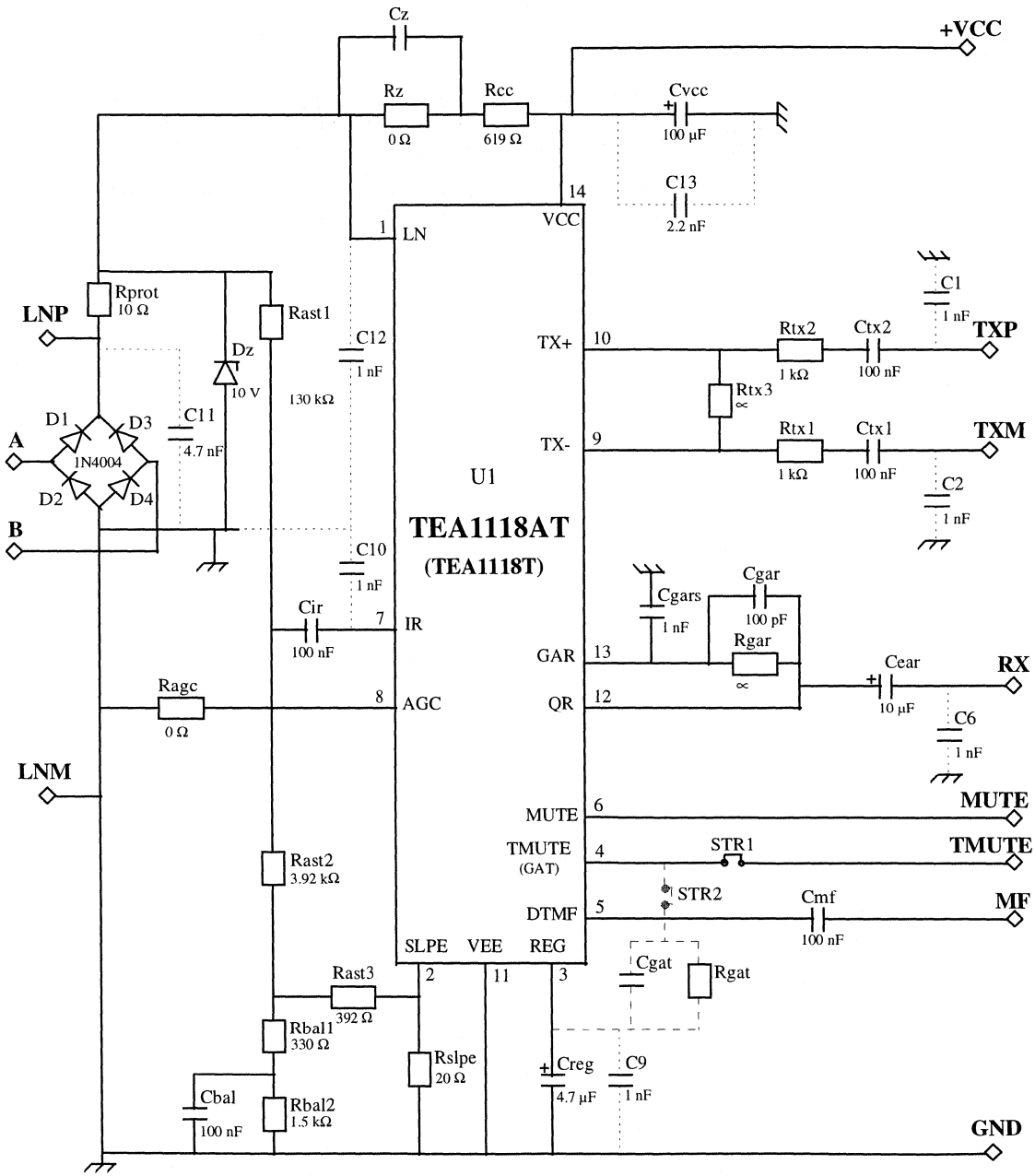


Fig. 38 Basic application of the TEA1118A

6. ELECTROMAGNETIC COMPATIBILITY

As no common international specification exists for RFI immunity, and as different assembly methods may lead to different solutions, only some advices can be provided.

It is advisable to take care of the impedance of the GND, the smallest is always the best. This means that the GND (VEE) trace must always be as large as possible, the best is to have a second layer dedicated to this purpose.

TX+/TX- inputs may also be sensitive (RF signals entering these pins would be amplified). Care has to be taken with the lay-out of the transmit amplifier, which is also helpfull for the noise, providing a good decoupling to GND. A low-pass RC filter may be added at the input of the amplifier.

Low impedance capacitors in parallel with the electrolythic one between VCC and GND as well as in parallel with the Creg capacitor may help.

Usually a low impedance capacitor connected between LN and GND helps for the conducted interferences, but this capacitor is in parallel with the impedance network of the apparatus, so, its value must be small enough.

In general when connections are coming from external environment (e.g. TXP, TXM, A, B on the demoboard), it is better to filter the RFI signal before it influences the close environment of the TEA1118/A (e.g. action of C1,C2,C11 on the demoboard).

7. REFERENCES

[1] TEA1118/A Versatile cordless transmission circuit
Device specification

[2] TEA1118/A Line Interface Demonstration Board
USER MANUAL of OM4789 (report n°: CTT96001)

[3] Philips Semiconductors
SEMICONDUCTORS FOR TELECOM SYSTEMS -IC03-

APPENDIX LIST OF ABBREVIATIONS AND DEFINITIONS

A-B	Line terminals of application example
AGC	Automatic Gain Control: line loss compensation
BRL	Balance Return Loss: matching between the apparatus impedance and a reference
DTMF	Dual Tone Multi Frequency
EMC	ElectroMagnetic Compatibility
GAR	Receive gain adjustment pin of the TEA1118/A
GAT	Transmit gain adjustment pin of the TEA1118
GND	Ground
Gvmf	DTMF amplifier gain
Gvrx	Receive gain
Gvtx	Transmit gain
IC	Integrated circuit
Icc	Current consumption of the TEA1118/A
Iline	Line current
Ip	Current consumption of the peripherals
Iqr	Internal current consumption (fromVCC) of the receive amplifier
IR	Receive amplifier input pin of the TEA1118/A
Islpe	Part of the line current flowing through SLPE pin
Istart	Start current of the AGC function
Istop	Stop current of the AGC function
Ith	Threshold current of the low voltage part
k	Scale factor of anti-sidetone network
Leq	Artificial inductor of the voltage stabilizer
MUTE	MUTE input of the TEA1118A
TMUTE	TMUTE input of the TEA1118A (transmit channel)
OM4789	Demoboard of the TEA1118A
QR	Receive amplifier output pin of the TEA1118/A
Ra	Resistor to adjust the sidetone bridge attenuation
Rast	Antisidetone resistor
REG	Filter capacitor of the equivalent inductor connection pin of the TEA1118/A
Rexch	Bridge resistance of exchange
RFI	Radio Frequency Interference

Rgar	External resistance to reduce receive gain of TEA1118/A
Rgarint	Internal resistance (100 kΩ) which sets the receive gain
Rgasint	Internal resistance (27 kΩ) which sets the transmit gain
Rgat	External resistance to reduce transmit gain of TEA1118
Rp	Internal resistance between LN and REG
SLPE	Slope input pin of the TEA1118/A
THD	Total Harmonic Distortion (%)
TX+/TX-	Transmit amplifier input pins of the TEA1118/A
VCC	Positive supply of the TEA1118/A
VEE	Ground reference of the TEA1118/A
Vln	DC voltage between LN and VEE
Vref	Stabilized reference voltage between LN and SLPE
Vslpe	DC voltage level between SLPE and VEE
Zir	Input impedance of the receive amplifier of the TEA1118/A
Zbal	Anti-sidetone network
α	Gain control factor of the AGC

Summary

This application note describes the UMA1021M IC from Philips Semiconductors. It permits low noise, low power single chip solution for designing a PLL frequency synthesizer. It is primarily intended for use in digital cellular and cordless communication equipment. Typical applications include GSM, DCS1800, PCS1900, DECT, PHS, CT2, DAMPS... It can also be used for any other radio applications up to 2 GHz, which need a single synthesizer, like PMR, marine, spread spectrum, security, ...

Section 1 contains a general presentation of the UMA1021M and section 2 details each part of the IC. Since the overall performance of any PLL frequency synthesizer system is critically determined by the lowpass filter used, a worked example of a PLL design is described in section 3. The following section shows measurement results from different applications (GSM, DCS1800, PHS, DECT and DAMPS). Guidance for the assembly and operation of the demonstration board is included in the annexe. Some rules of thumb and tricks are indicated in the last section in "Frequently Asked Questions".

All data presented in this report have been obtained from the characterisation of a few typical samples. Whilst most samples have similar performance, only values indicated on the UMA1021M specification are guaranteed by Philips. These results must be considered as an aid to design the PLL in your application.

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1. Introduction to the UMA1021M single synthesizer

1.1 General description

The UMA1021M [1] is a low phase noise, low power, low voltage, one chip solution to a single frequency synthesizer for use in radiocommunications. Designed in a BICMOS process, it operates from 2.7 (3 NiCd cells) to 5.5 V. The UMA1021M contains all the necessary elements with the exception of the VTCXO, VCO and loop filter to build a PLL frequency synthesizer.

The synthesizer operates at RF input frequencies up to 2.2 GHz, with fully programmable main and reference dividers. The reference input operates from 3 to 35 MHz. Fast programming is possible via the three wire serial bus with clock speeds up to 10 MHz.

The phase detector drives low and high current charge pump simultaneously. Maximum current is 0.4 mA with the low current charge pump (pin CP) and 3.2 mA with the fast charge pump (pin CPF). The latter can be disabled by the pin FAST. The programmable charge pump currents are fixed by an external resistance R_{SET} (at pin I_{SET}). Only passive loop filters are necessary.

Separate power supply and ground pins are provided to the analog (charge pumps) and digital parts of the IC.

The synthesizer can be powered down to save current via software programming or by hardware pin PON.

1.2 Features

- Low power / power-down
- Very low noise BICMOS design (-90 dBc/Hz typically measured in the loop bandwidth in a GSM application)
- Small SSOP-20 package
- Fast 3-line serial bus interface
- RF input from 300 to 2200 MHz
- Fully programmable main and reference dividers
- Programmable charge pump currents
- Dual phase comparator outputs to allow fast frequency switching
- Out-of-lock indicator

1.3 Typical application

The UMA1021M single synthesizer is typically used in digital radiotelephone systems which require very low phase noise and spurious like GSM and DCS1800. It can also be used with applications which need fast switching like DECT. Fig. 2 shows a typical application which allows the use of the UMA1021M.

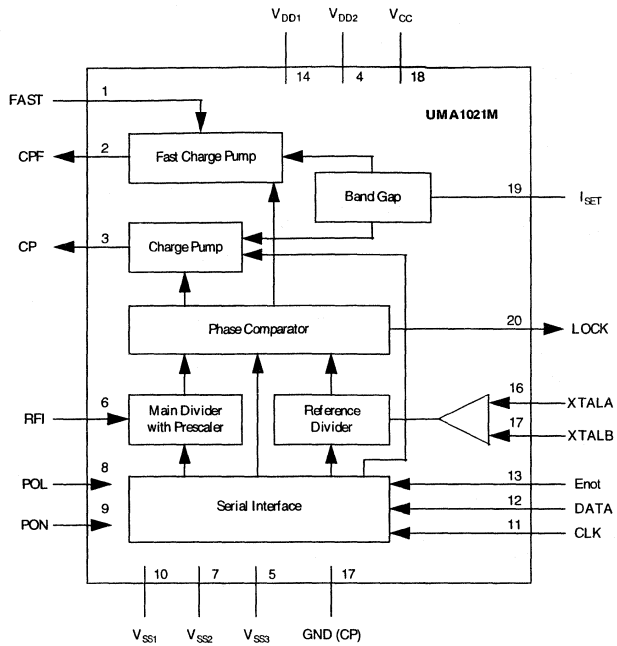


Fig. 1 - UMA1021M Block Diagram.

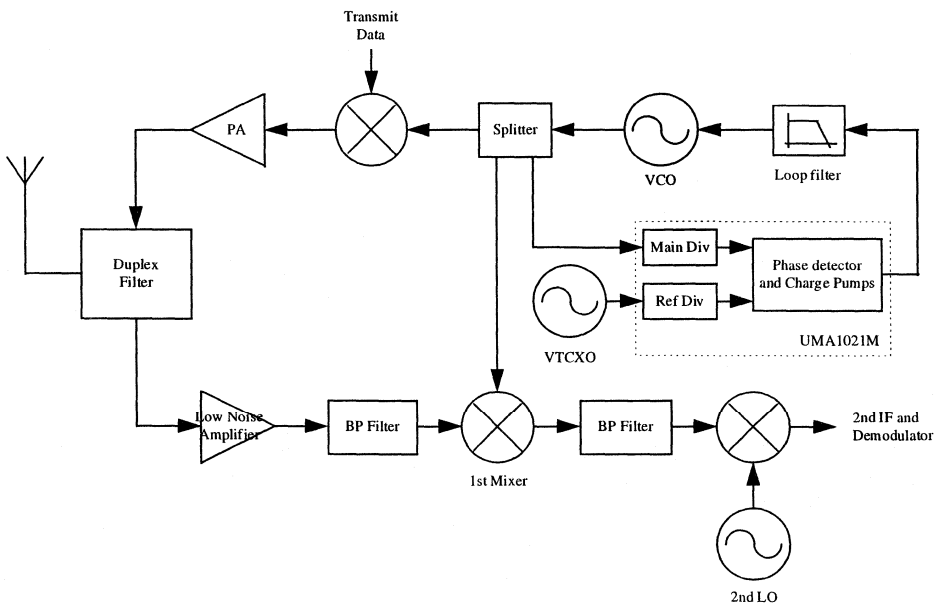


Fig. 2 - Typical Application Block Diagram.

2. Functional description of the UMA1021M synthesizer

Refer to the UMA1021M PLL block illustrated in the application diagram (Fig. 2).

A crystal (VTCXO) provides a high purity, stable reference frequency to the PLL. VCO and crystal frequencies are divided down to a common comparison frequency to feed the phase detector. The phase detector drives a charge pump to send correction current pulses to a low pass filter. The current pulses are proportional to the difference in phase between the two phase detector input signals. The filter integrates the pulses giving a voltage which controls the Voltage Controlled Oscillator. The PLL is locked when the phase difference between input signals to the phase detector is maintained zero.

2.1 Phase detector and charge pump

2.1.1 Description

The phase detector is sensitive to both phase and frequency. It reacts to very small phase differences between the main divider and reference divider inputs. The design responds to the full $\pm 2\pi$ radians range of phase inputs.

The operating principle of the phase detector is depicted in Fig. 3. The comparison frequency f_{PC} at the input of the phase detector is typically the same as the radio system channel spacing.

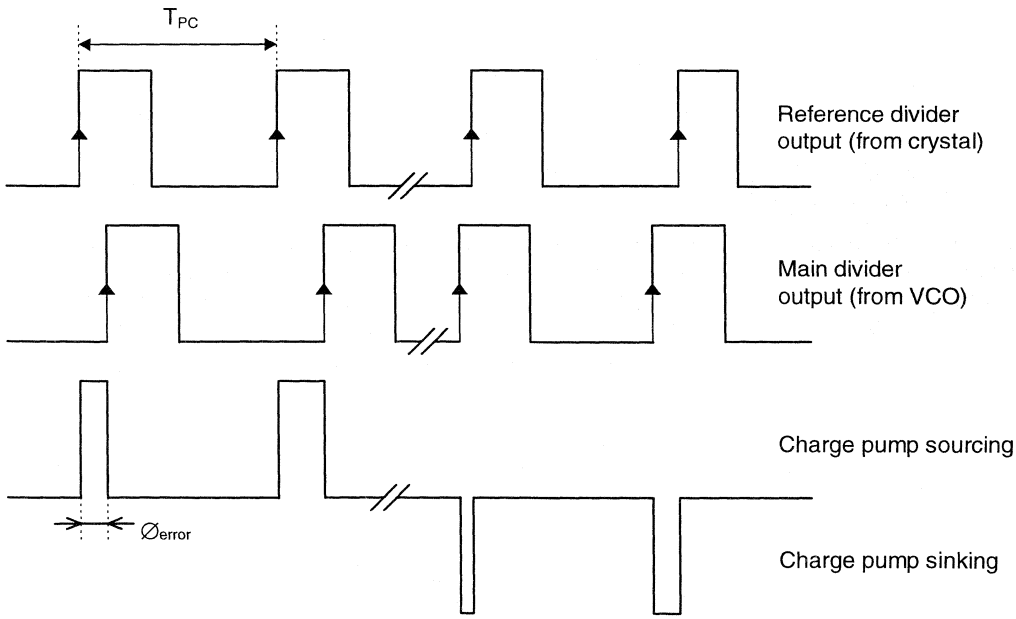


Fig. 3 - Principle of UMA1021M Phase Detector.

The charge pump outputs of the synthesizer are either sourcing, sinking or in high impedance. When the loop is locked, i.e. when the phase error at the input of the phase detector is zero, the charge pump output is in the high impedance state. When the loop is not locked, a phase error between the input signals is seen by the

phase detector and the charge pump sends correction pulses to the loop filter. If the output of the reference divider is leading, then the charge pump sources current pulses to increase the VCO control voltage and frequency. If the output of the reference divider is lagging, the charge pump sinks current pulses to decrease the VCO control voltage and frequency. The pulse duration is proportional to the phase error. The sinking and sourcing pulses charge or discharge the capacitors in the loop filter, to a voltage required to bring the PLL back into lock.

The phase detector drives two charge pumps (pins CP and CPF). The charge pump currents (the « height » of the positive or negative pulses in Fig. 3) are switch-selectable by software. The I_{CP}/I_{CPF} current ratio between the two charges pumps varies from 4 to 16. The reference current I_{SET} is set by an external resistance R_{SET} at pin I_{SET}, where a temperature independent voltage of 1.2 volts is generated. R_{SET} should be between 5.6 kΩ and 12 kΩ to give an I_{SET} between 200 µA and 100 µA approximately. The charge pump output currents can be programmed as shown below.

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	2 x I_{SET}	8 x I_{SET}	4:1
0	1	2 x I_{SET}	16 x I_{SET}	8:1
1	0	1 x I_{SET}	12 x I_{SET}	12:1
1	1	1 x I_{SET}	16 x I_{SET}	16:1

Table 1 - Charge Pumps Current Ratio Relationships.

There are two ways to connect the charge pump outputs to the principal loop filter:

- Generally, the two charge pump outputs (CP and CPF) are connected together to the loop filter. The loop filter design is given in section 3.1.
- The second way is to have a dual time constant loop. The loop uses both charge pumps during frequency switching. The phase detector drives just the slow charge pump after the required frequency is obtained. The fast charge pump is disabled by the pin FAST. A narrower loop filter allows the modulation of the VCO, with lower modulation frequencies than those possible with a wider loop filter.

The curves on the following pages show dc measurements of sink and source currents of the two charge pumps.

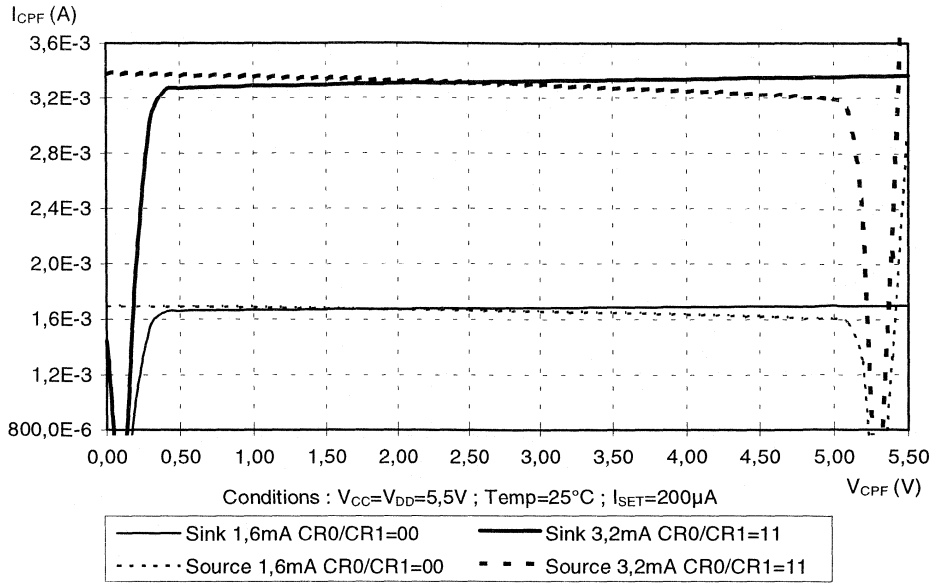


Fig. 4 - Fast Charge Pump (CPF) Output Current vs Voltage.

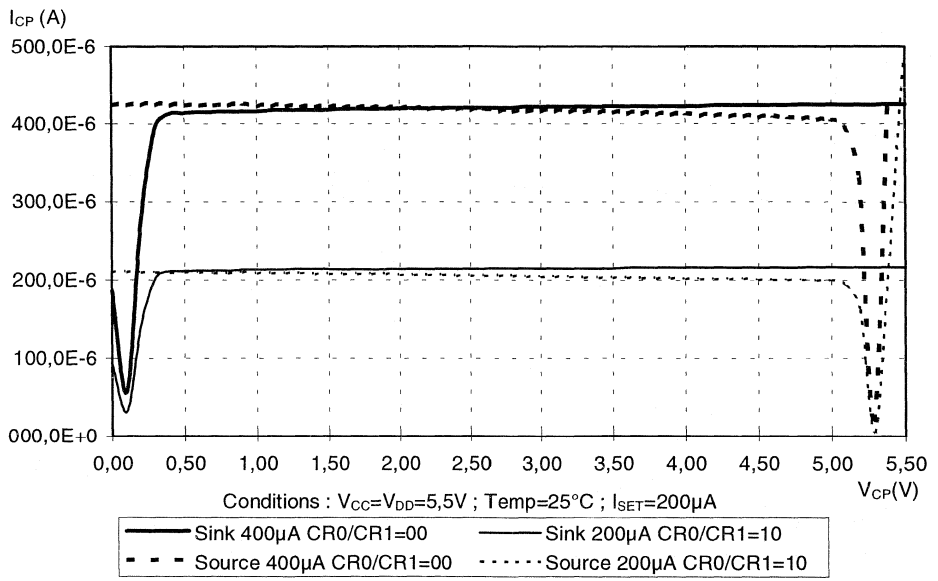


Fig. 5 - Slow Charge Pump (CP) Output Current vs Voltage.

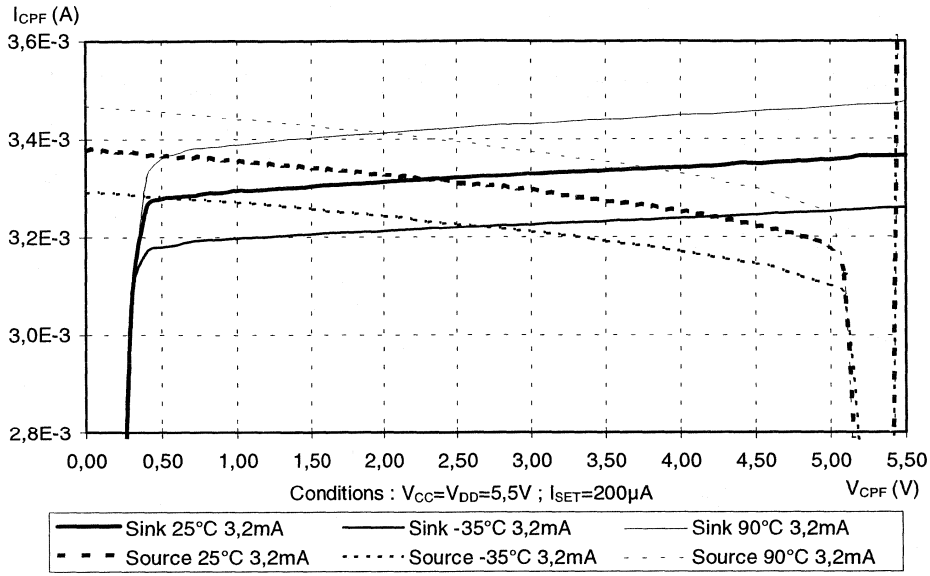


Fig. 6 - Fast Charge Pump (CPF) Output Current vs Voltage and Temperature.

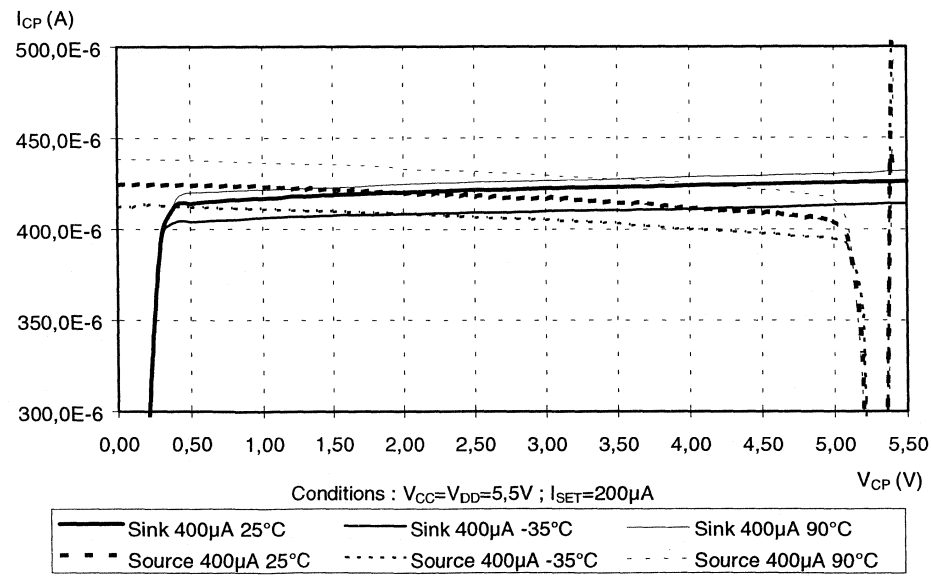


Fig. 7 - Slow Charge Pump (CP) Output Current vs Voltage and Temperature.

2.1.2 Dynamic characteristics

The method used to measure the charge pump dynamic characteristics is described on the next few pages. A multimeter with a resolution less than 1 nA and a frequency generator with a phase variation option are needed.

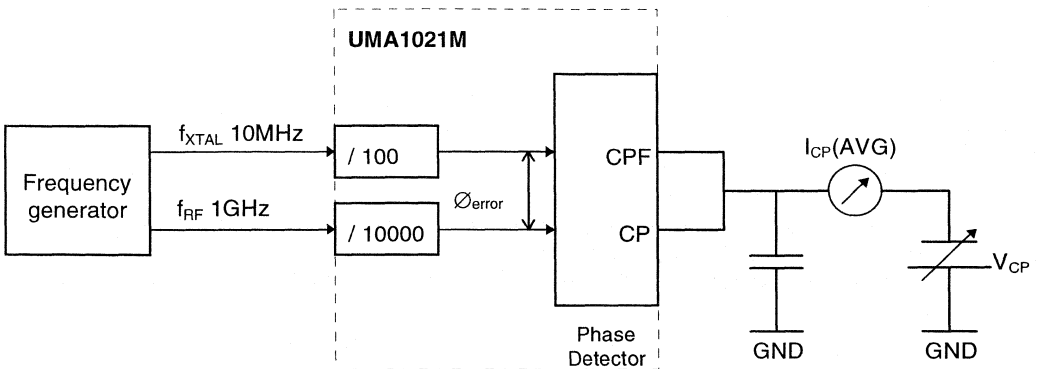
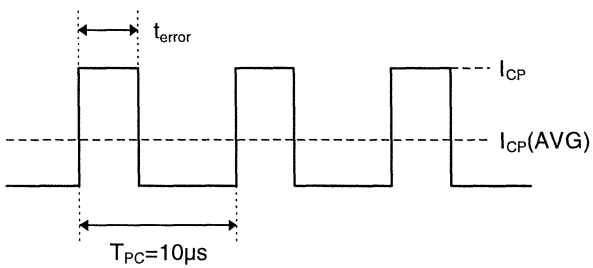
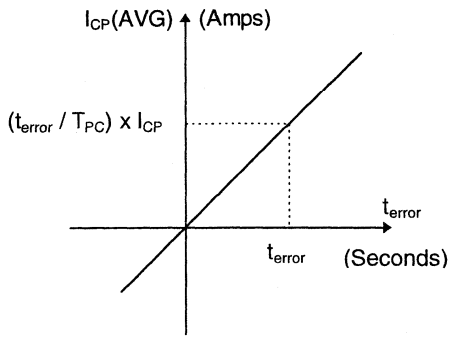


Fig. 8 - UMA1021M Principal Synthesizer Phase Detector Linearity Measurement.

A frequency generator supplies the reference divider (frequency f_{XTAL}) and the main divider (frequency f_{RF}). These frequencies are divided down to obtain a comparison frequency of 100 kHz. The generator allows the phase of the 1 GHz signal to be controlled with respect to the 10 MHz reference signal. The I_{CP}(AVG) phase detector current is measured as a function of the phase error.



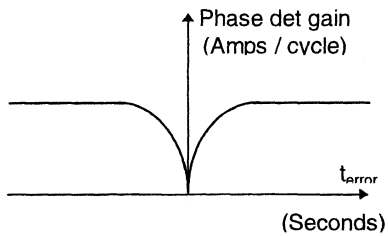
$$I_{CP}(AVG) = \left(\frac{t_{error}}{T_{PC}}\right) \times I_{CP}$$



In order to find the real phase detector and charge pump gain for very small phase errors, we transform this curve by the equation: Phase Detector Gain (Amps/cycle) = I_{CP}(AVG) x (T_{PC} / t_{error}). So the charge pump dynamic characteristics are obtained (see Fig. 10, Fig. 12, Fig. 14 and Fig. 16). Curves show measurements for source and sink gains.

Phase error values are taken in the region of ± 16 ns. This is where the phase detector and the charge pump are less linear and where the loop spends most of its time, i.e. when it is locked or nearly locked.

The charge pump must remain linear for small phase errors, to ensure a low and stable value of close in noise and to optimise settling time. Traditionally this has caused problems to PLL designers, the worst being the so-called "dead zone" in which the dynamic gain falls to zero (as shown below) due to the charge pump not reacting to small phase errors.



Philips Semiconductors has focused effort on the design of a very linear charge pump for the UMA1021M. Different curves show that the real charge pump gain for very small phase errors is mostly maintained within 15% of ideal value. The jagged nature of the curves can partly be explained by very small values of I_{CP}(AVG), and phase error granularity problems.

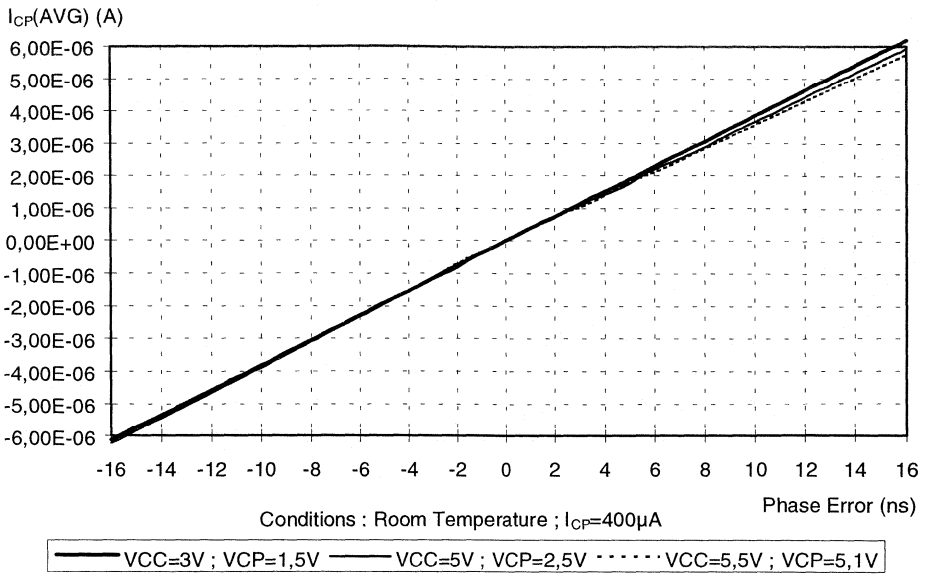


Fig. 9 - Phase Detector and Slow Charge Pump Characteristic vs V_{cc}.

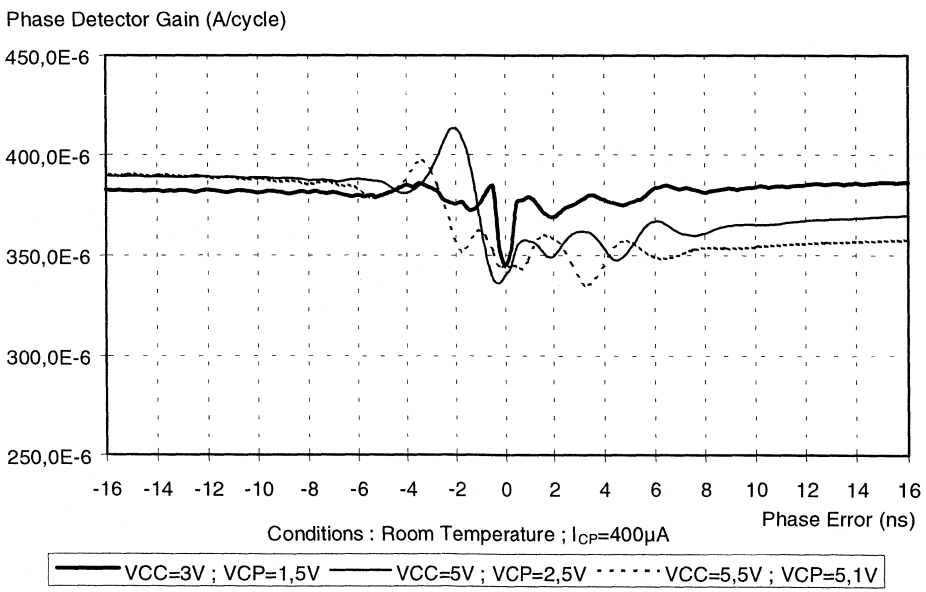


Fig. 10 - Phase Detector and Slow Charge Pump Gain vs V_{cc}.

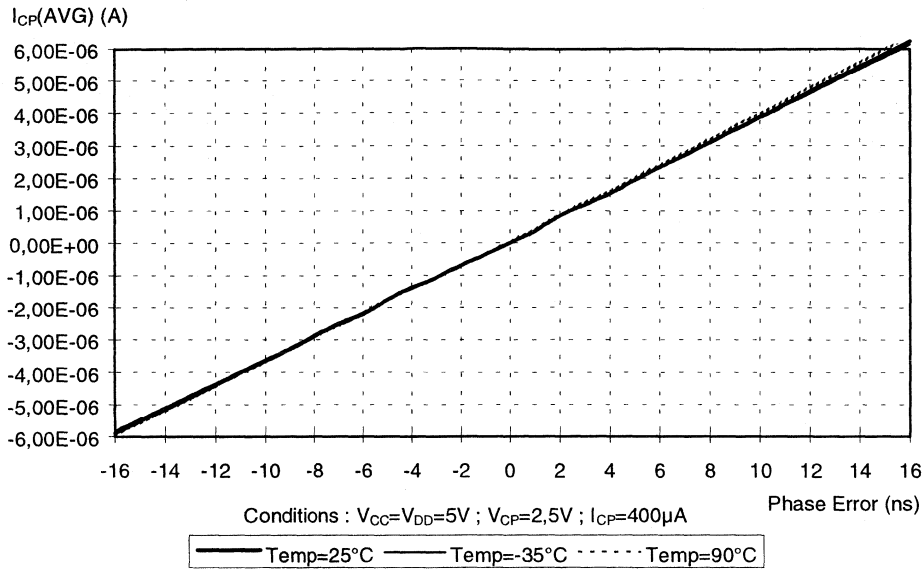


Fig. 11 - Phase Detector and Slow Charge Pump Characteristic vs Temperature.

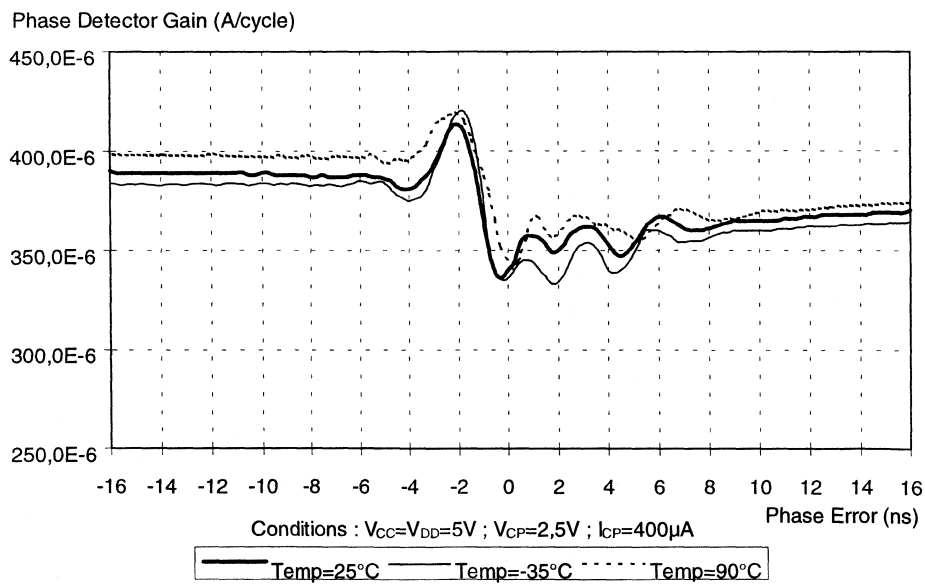


Fig. 12 - Phase Detector and Slow Charge Pump Gain vs Temperature.

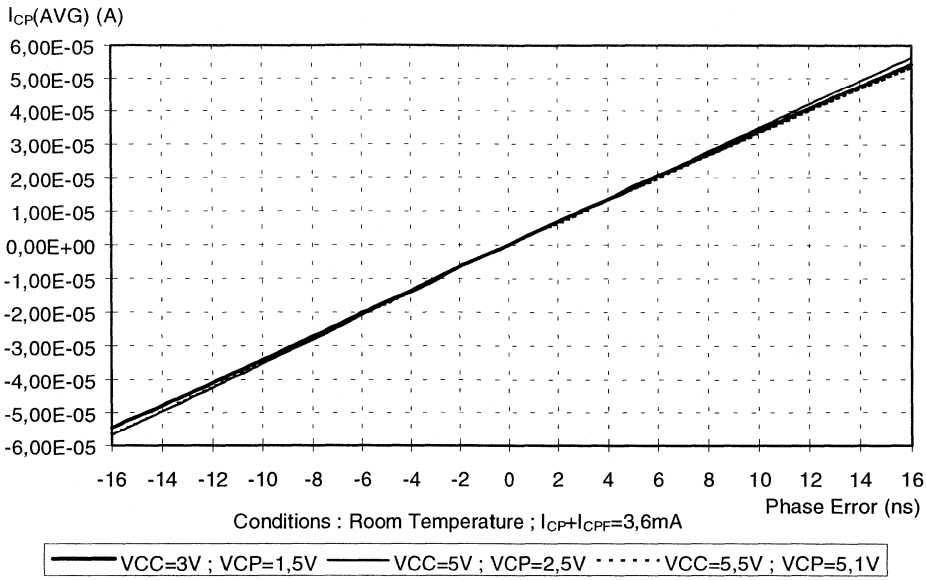


Fig. 13 - Phase Detector and Charge Pumps Characteristic vs V_{cc}.

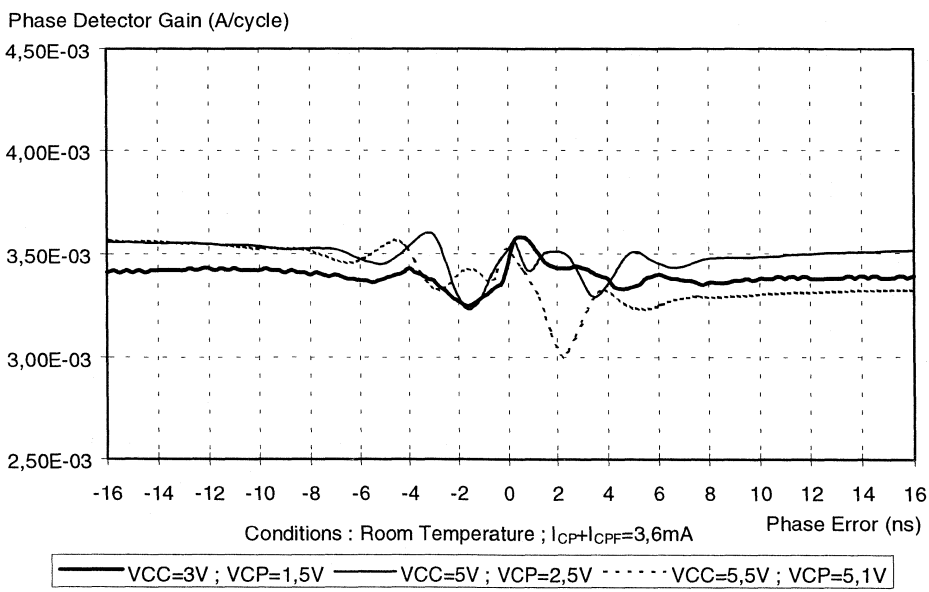


Fig. 14 - Phase Detector and Charge Pumps Gain vs V_{cc}.

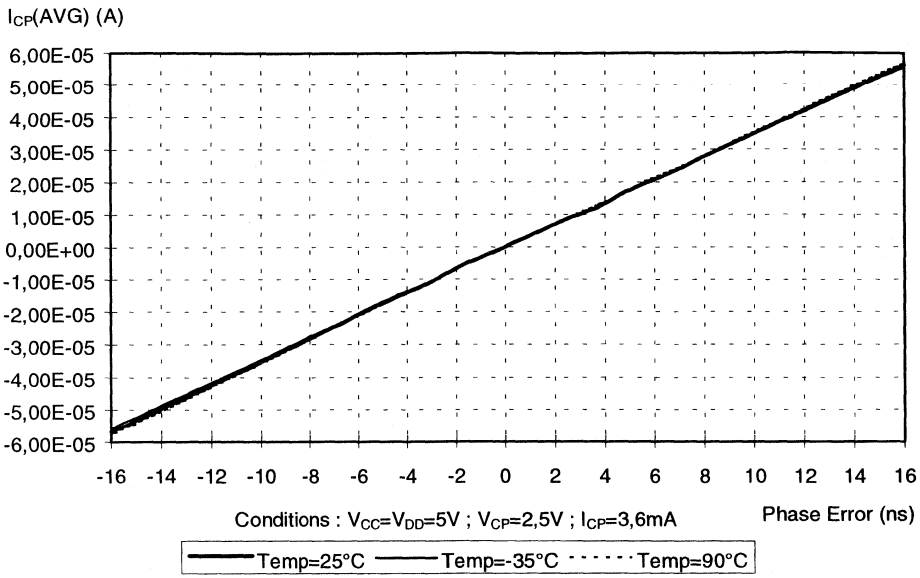


Fig. 15 - Phase Detector and Charge Pumps Characteristic vs Temperature.

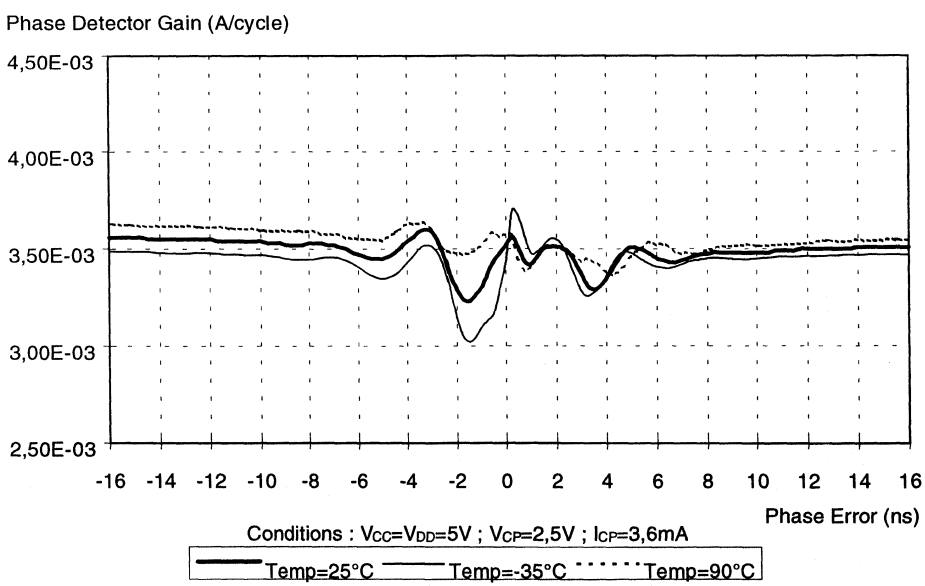


Fig. 16 - Phase Detector and Charge Pumps Gain vs Temperature.

2.2 Programming

A simple three wire unidirectional serial bus is used to program the synthesizer. The three lines are DATA, CLK (Clock) and Enot (Enable). The data sent to the device is loaded in bursts framed by Enot. Programming clock edges are ignored until Enot goes active low. The programmed information is loaded into the addressed latch when Enot returns inactive high. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down. After software or hardware power down is terminated, it is not necessary to reprogram the device. Previous programming data is preserved during power-down.

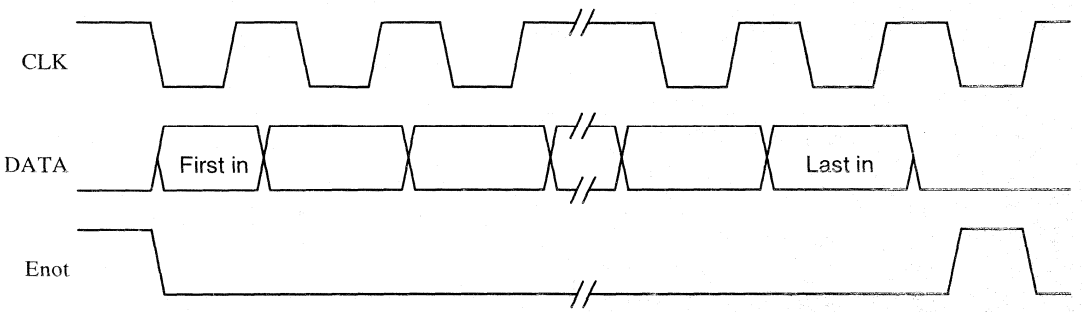


Fig. 17 - Serial Interface Timing Diagram.

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are used for the address. The bits are decoded on the rising edge of Enot. A worked example of programming is shown in section 2.2.2 below.

2.2.1 Power-down mode

The synthesizer is on when both the input signals PON and the programmed bit sPON are active. The 'active' level for these two signals is chosen at pin POL. When turned on, the dividers and phase detector are synchronized to avoid random phase errors. When turned off, the phase detector is synchronized to avoid interrupting charge-pump pulses. For synchronization functions to work correctly on power-up or power-down (using either hardware or software programming), the presence of TCXO and VCO signals is required to drive the appropriate divider inputs. The UMA1021M has a very low current consumption in the power-down mode.

2.2.2 UMA1021M typical programming example

Crystal reference input frequency: 13 MHz

RF input frequency: 902 MHz (Main divider ratio = PM = 4510)

Comparison frequency: 200 kHz (Reference divider ratio = PR = 65)

Synthesizer ON (PON=1) ; POL pin is pulled up

Out of lock indication (OOL=1)

Charge pump currents: $I_{CPF} = 16 \times I_{SET}$; $I_{CP} = 2 \times I_{SET}$ (CR1 = 0 ; CR0 = 1)

first in	Register bit allocation in	last
dt16	Data field dt0	Address
Control reg = 0 0001 0010 0100 0000b		1 h
Main divider coefficient = 4510d = 0119Eh		4 h
Reference divider coefficient = 65d = 00041h		5h

Table 2 - UMA1021M Register Data Allocations Expressed in Decimal and Hexadecimal.

first in (msb)								Data field in								(lsb) last		Adress			
0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	1	1	0	0	1	1	1	1	0	0	1	0	0	
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	

Table 3 - UMA1021M Register Data Allocations Expressed in Binary.

2.2.3 UMA1021M preset values

After the supply voltage is switched on, the different registers are loaded with following preset values. They correspond to a typical GSM application. When using a 13 MHz VTCXO, the PLL is directly locked at 910 MHz (if it is within the VCO range) with a 200 kHz comparison frequency.

Main divider ratio	4550
Reference divide ratio	65
Control register	OOL=0 ; CR1=1 ; CR0=1 ; sPON=1
Test register	all 0

Table 4 - UMA1021M Preset Values.

Since the preset state is not tested, Philips Semiconductors does not guarantee these values. Programming of all registers is recommended after switching ON the synthesizer supply voltage.

2.3 Reference divider

The input f_{XTAL} drives a pre-amplifier to provide the clock input for the reference divider. Fig. 18 shows the typical measured input sensitivity of the reference divider at room temperature.

Fig. 19 shows the sensitivity with different temperature measurements which were carried out for the worst case supply (i.e. V_{DD} = 2.7 V). Reference divider has been observed to work correctly for high input levels up to 10 dBm. For reference and main dividers sensitivity measurements, the input pins have been externally terminated by a capacitivly decoupled 50 Ω load.

Fig. 20 and Table 5 show the Fxtal input admittance. These parallel elements (conductance and susceptance) are given for typical samples. A high input resistance has been measured, 10 kΩ typically. There is no significant impedance change when powering down the synthesizer (as shown in Table 5).

Since the Fxtal input DC voltage is internally fixed, a DC decoupling capacitor must be inserted between these pins (XTALA and XTALB) and the reference source or ground.

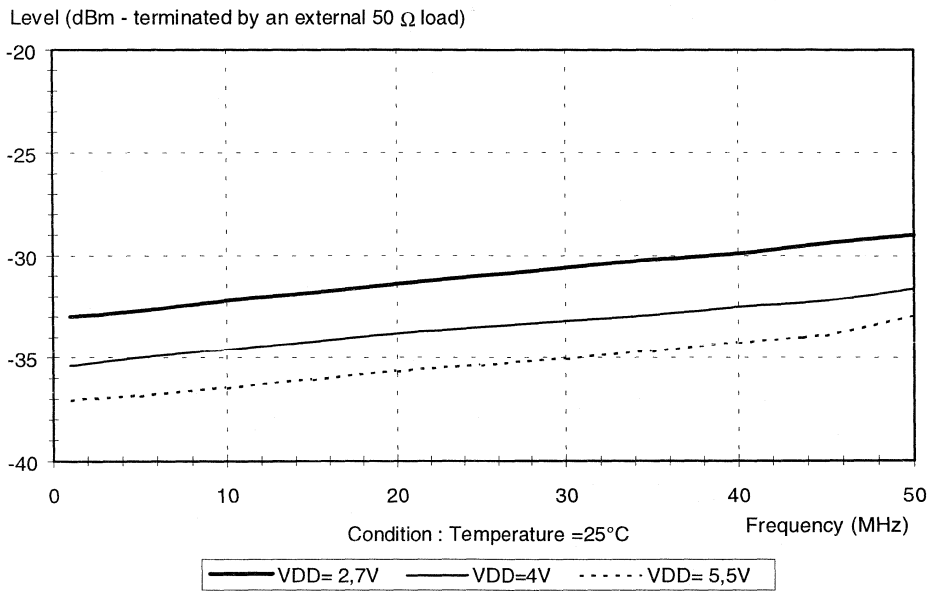


Fig. 18 - Reference Divider Input Sensitivity vs Frequency and Supply.

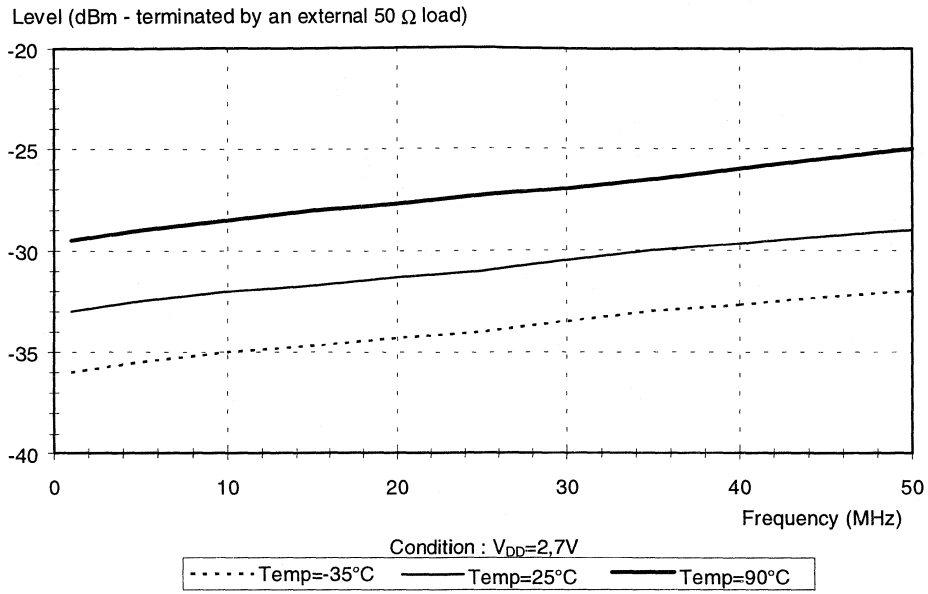


Fig. 19 - Reference Divider Input Sensitivity vs Frequency and Temperature.

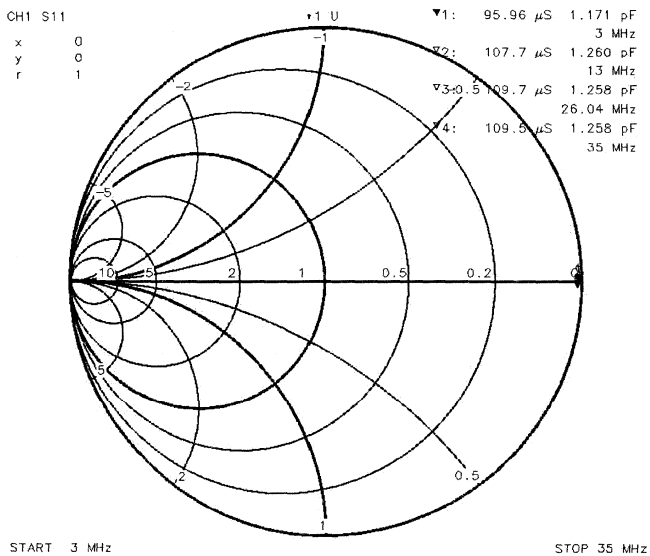


Fig. 20 - Typical F_{xtal} Input Admittance (IC powered up).

Input Frequency	Power Up		Power Down	
(MHz)	Real Part	Imaginary Part	Real Part	Imaginary Part
3	96 µS (10.4 kΩ)	22 µS (1.15 pF)	70 µS (14.3 kΩ)	29 µS (1.19 pF)
13	108 µS (9.3 kΩ)	102 µS (1.26 pF)	79 µS (12.7 kΩ)	100 µS (1.23 pF)
26	109 µS (9.2 kΩ)	205 µS (1.26 pF)	81 µS (12.3 kΩ)	200 µS (1.23 pF)
35	108 µS (9.3 kΩ)	276 µS (1.26 pF)	80 µS (12.5 kΩ)	270 µS (1.23 pF)

Table 5 - Typical F_{xtal} Input Admittance.

2.4 Main Divider

The RF input drives a pre-amplifier to provide the clock for the main divider. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The high frequency sections of the main dividers are implemented using bipolar logic, while the slower sections use lower current CMOS logic. Fig. 21 shows the typical measured input sensitivity of the main divider at room temperature. For frequency sensitivity versus temperature measurement (Fig. 22), the IC is supplied with the worst case for V_{DD} (i.e. V_{DD} = 2.7 V).

Fig. 23 and Table 6 show RF input admittances. These parallel elements (conductance and susceptance) are given for typical samples. There is no significant impedance variation observed between power up and power down states.

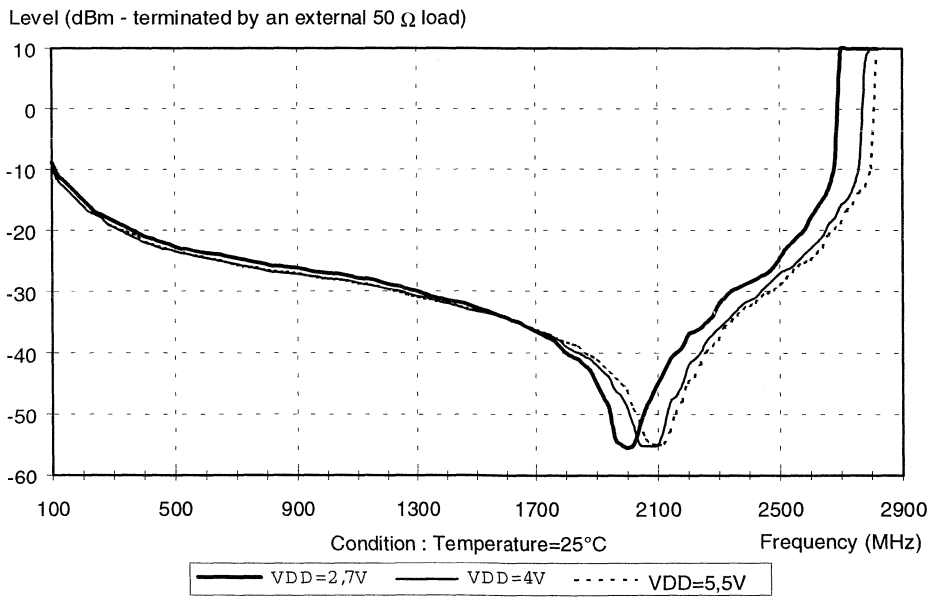


Fig. 21 - Main Divider Input Sensitivity vs Frequency and Supply.

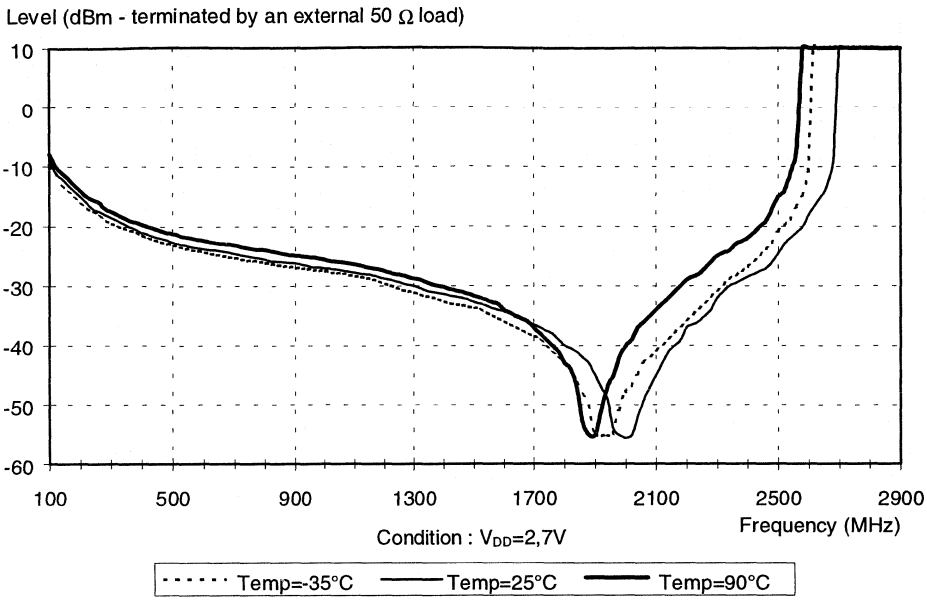


Fig. 22 - Main Divider Input Sensitivity vs Frequency and Temperature.

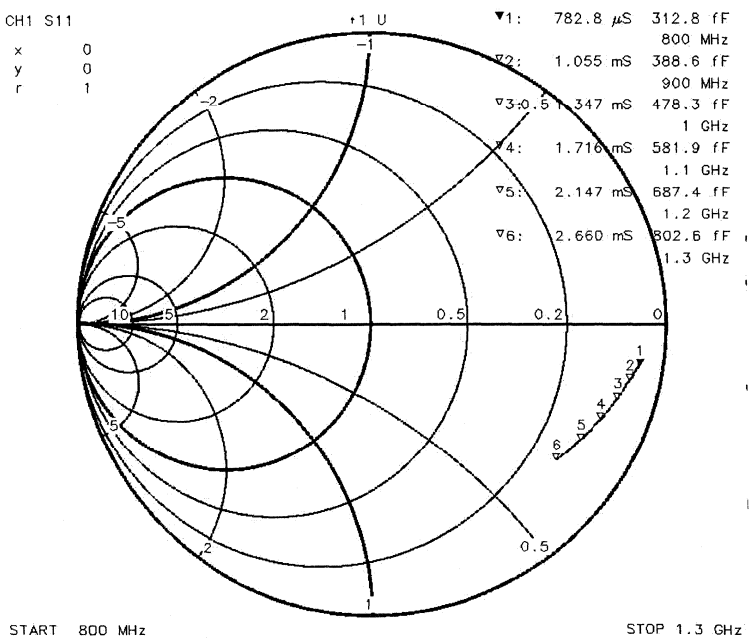


Fig. 23 - Typical RF Input Admittance (IC powered up).

Input Frequency	Power Up		Power Down	
(MHz)	Real Part	Imaginary Part	Real Part	Imaginary Part
300	279 µS (3.6 kΩ)	174 µS (90 fF)	262 µS (3.8 kΩ)	114 µS (60 fF)
400	348 µS (2.9 kΩ)	266 µS (110 fF)	322 µS (3.1 kΩ)	184 µS (70 fF)
500	454 µS (2.2 kΩ)	425 µS (136 fF)	420 µS (2.4 kΩ)	318 µS (100 fF)
600	558 µS (1.8 kΩ)	690 µS (180 fF)	513 µS (1.9 kΩ)	555 µS (150 fF)
700	688 µS (1.5 kΩ)	1.038 mS (240 fF)	632 µS (1.6 kΩ)	878 µS (200 fF)
800	784 µS (1.3 kΩ)	1.575 mS (310 fF)	722 µS (1.4 kΩ)	1.39 mS (280 fF)
900	1.06 mS (940 Ω)	2.2 mS (390 fF)	1 mS (1 kΩ)	1.98 mS (350 fF)
1000	1.35 mS (740 Ω)	3 mS (480 fF)	1.3 mS (770 Ω)	2.74 mS (435 fF)
1100	1.72 mS (580 Ω)	4.02 mS (580 fF)	1.66 mS (600 Ω)	3.65 mS (530 fF)
1200	2.15 mS (470 Ω)	5.18 mS (690 fF)	2.07 mS (480 Ω)	4.73 mS (630 fF)
1300	2.66 mS (380 Ω)	6.54 mS (800 fF)	2.55 mS (390 Ω)	6.01 mS (735 fF)
1400	3.29 mS (300 Ω)	8.11 mS (920 fF)	3.13 mS (320 Ω)	7.45 mS (850 fF)
1500	3.99 mS (250 Ω)	9.88 mS (1.05 pF)	3.76 mS (270 Ω)	9.07 mS (960 fF)
1600	4.8 mS (210 Ω)	11.75 mS (1.17 pF)	4.47 mS (220 Ω)	10.08 mS (1.07 pF)
1700	5.46 mS (180 Ω)	13.56 mS (1.27 pF)	5.11 mS (200 Ω)	12.57 mS (1.17 pF)
1800	6.08 mS (160 Ω)	15.3 mS (1.35 pF)	5.69 mS (180 Ω)	14.3 mS (1.26 pF)
1900	6.88 mS (150 Ω)	17.2 mS (1.44 pF)	6.37 mS (160 Ω)	16.1 mS (1.35 pF)
2000	7.6 mS (130 Ω)	18.9 mS (1.5 pF)	6.99 mS (140 Ω)	17.7 mS (1.4 pF)
2100	8.27 mS (120 Ω)	20.3 mS (1.54 pF)	7.56 mS (130 Ω)	19.2 mS (1.45 pF)
2200	8.87 mS (110 Ω)	21.5 mS (1.56 pF)	8.1 mS (120 Ω)	20.4 mS (1.47 pF)

Table 6 - Typical RF Input Admittance.

2.5 Voltage and Ground Pins

Separate power and ground pin are provided to the analog and digital sections. To reduce crosstalk between CMOS and bipolar parts, two independent pins supply the digital parts of the integrated circuit (V_{DD1} and V_{DD2}). V_{DD2} supplies the main divider bipolar section and V_{DD1} the other remaining digital sections. V_{DD1} and V_{DD2} could be shorted at the pins, however separate decoupling is better. The voltage difference between these pins should be no greater than 300 mV.

The ground leads should be externally shorted together otherwise large currents may flow across the die, and damage it.

2.6 In lock detector

The out-of-lock functions works in the following way:

- When the phase error ϕe is greater than T_{OOL} with $T_{OOL} \cong 20$ ns (approximately), the OOL signal goes low.
- When coming back into lock, ϕe has to be smaller than T_{OOL}. Then, the OOL signal goes high again.

This procedure is illustrated in the diagram below.

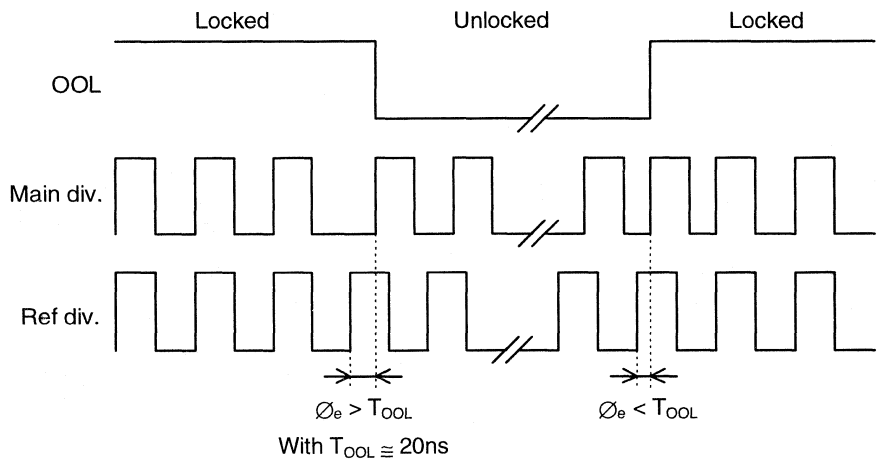
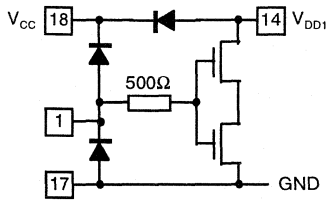
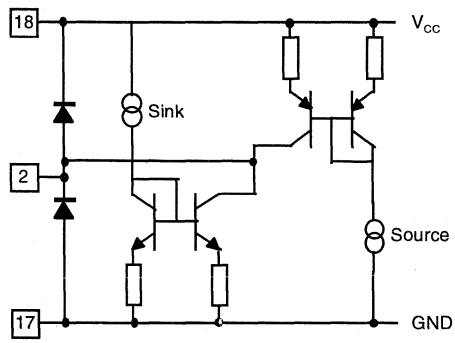
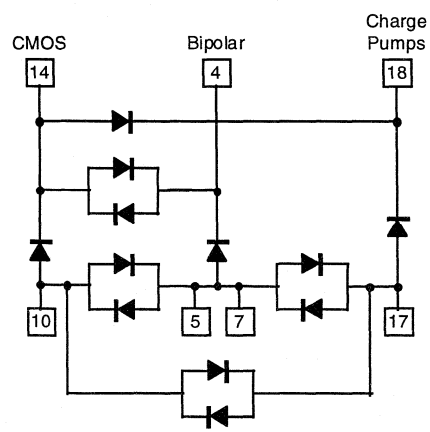
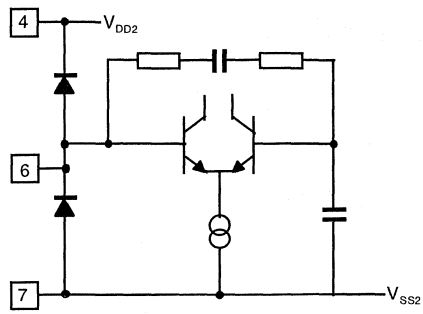
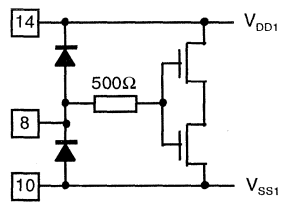
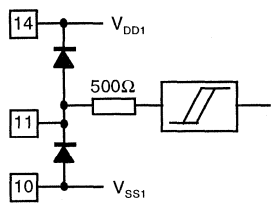
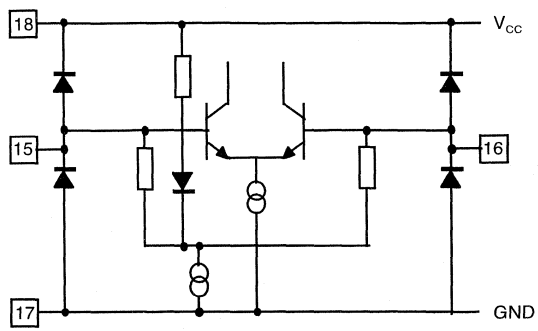


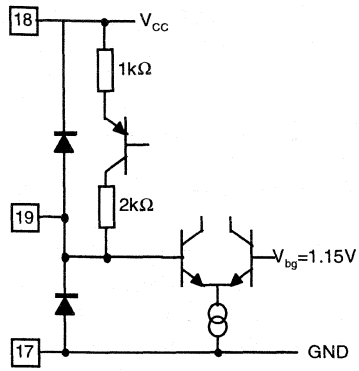
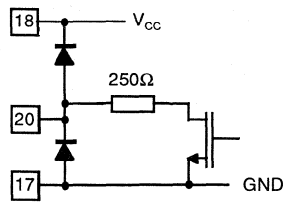
Fig. 24 - Operating Principle of the Out-Of-Lock Detector.

2.7 Functional pin description

DC voltage measurements were made on a demonstration board powered by 5 V analog and digital voltage supplies.

Pin No.	Pin Mnemonic	DC V	Equivalent Circuit
1	FAST	+5	
2 3	CPF CP	- -	
4 14 18 5 7 10 17	V_{DD2} V_{DD1} V_{CC} V_{SS3} V_{SS2} V_{SS1} GND	+5 +5 +5 0 0 0 0	

6	RFI	+4	
8 9	POL PON	+5 +5	
11 12 13	CLK DATA Enot	+5 0 +5	
15 16	XTALA XTALB	+3.5 +3.5	

19	I_{SET}	+1.2	
20	LOCK	+5	

3. Loop Filter Design

3.1 Basic Loop Filter Design Procedure

This section gives the procedure to ensure a quick and simple loop filter design. The method is based on first order approximations, and provides a working solution without the need for computer simulation. Reading appendixes 6.1 and 6.2 can be useful to clarify some PLL terms and equations in this section.

The purpose of a Phase Locked Loop (PLL) frequency synthesizer as shown in Fig. 25 is to transfer the spectral purity and stability of a fixed reference frequency oscillator (TCXO or VTCXO) to that of the Voltage Controlled Oscillator (VCO) for a number of output frequencies.

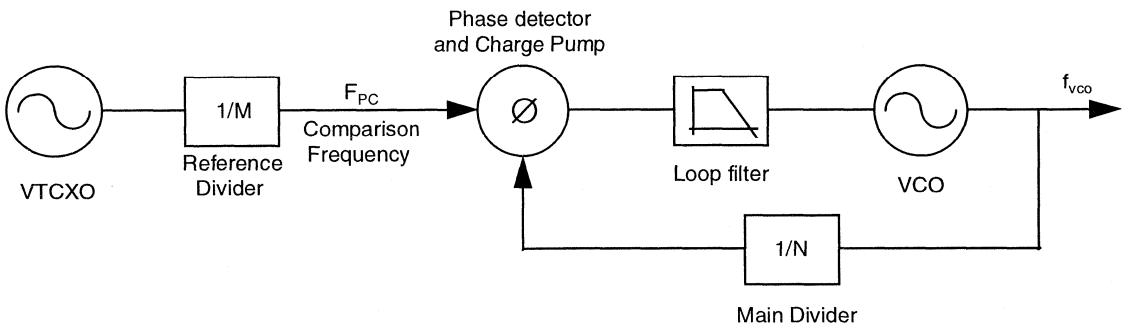
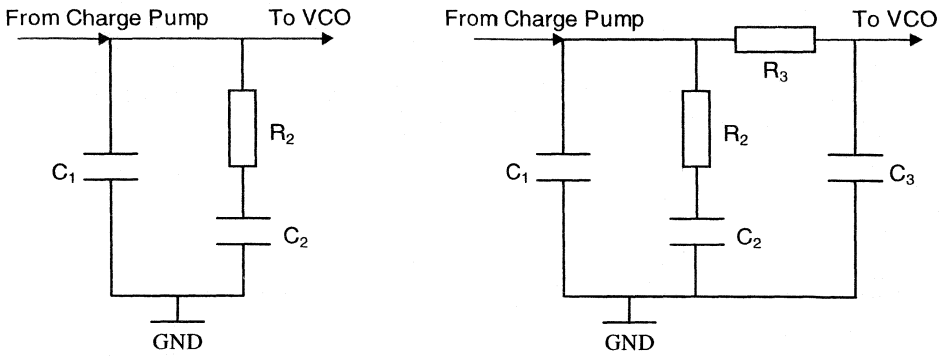


Fig. 25 - Basic Phase Lock Loop Block Diagram.

The correct design of the loop filter is of considerable importance to have the optimum performance from the synthesizer. The filter should be designed so as to achieve the required compromise between noise performance, switching time, comparison frequency spur rejection and modulation requirements.

Loop filters are usually passive when used with current charge pumps, but can be active if desired. Passive loops have the advantage of reduced noise, fewer parts count and low cost. With UMA1021M synthesizer, only passive loop filters are necessary. Two common configurations are shown overleaf. The filters in Fig. 26 are classified in terms of the order of the control loop formed.

With UMA1021M, the use of the loop filter (a) is often sufficient. For applications requiring further comparison frequency breakthrough rejection, a low pass filter stage (R_3, C_3) can be added. This reduces comparison frequency breakthrough spurs without affecting too much the transient response of the loop, with appropriate design.



(a) Third Order PLL (b) Fourth Order PLL

Fig. 26 - Different Types of Passive Loop Filter.

Loop parameters are first chosen:

- f_{VCO}: VCO frequency (in Hz)
- f_{PC}: Phase comparator frequency (in Hz)
- t_s: Switching time (in seconds)
- K_{vco}: VCO gain (in Hz/V)
- I_{CP}: Phase comparator gain (in Amps/cycle)

As a starting point, the equations below are used.

- $$w_n = 2 \times \Pi \times f_n = \sqrt{\frac{K_{VCO} \times I_{CP}}{C_2 \times N}} \quad (1)$$
- $$R_2 = 2 \times \rho \times \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} \quad (2)$$

Where f_n is the natural frequency (in Hz) and ρ is the damping coefficient.

☞ Calculate the resistor R_{SET} for setting the charge pump output current from:

$$R_{SET} = \frac{1.2}{I_{SET}} \quad (3)$$

Charge pump current is related to I_{SET} according to the relationship given in the Table 1 and whether the two charge pumps CP and CPF are connected together or not.

☞ Use rule of thumb to determine the natural frequency f_n based on desired switching time t_s.

$$f_n = \frac{2.5}{t_s} \quad (4)$$

It has been found by experience that a good PLL loop filter design takes a switching time (t_s) of less than $2.5/f_n$ to settle to a new frequency. This rule of thumb allows a good compromise between switching time, stability and noise performance when using the UMA1021M synthesizer. Of course the switching time will also depend on the size of the frequency jump and the definition of when the PLL is settled (i.e. acceptable frequency or phase error with respect to target).

☞ Determine main divider ratio from:

$$N = \frac{f_{VCO}}{f_{PC}} \quad (5)$$

☞ Determine angular velocity w_n (in rad/seconds) from:

$$w_n = 2 \times \Pi \times f_n \quad (6)$$

☞ Determine C_2 from (1)

$$C_2 = \frac{K_{VCO} \times I_{CP}}{w_n^2 \times N} \quad (7)$$

☞ Select damping ratio of approximately 0.9 for a good compromise between switching time and stability.

☞ Determine R_2 from (2)

☞ $$R_2 = 2 \times \rho \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} \quad (8)$$

☞ Choose C_1 between 1/10 and 1/15 the value of C_2

☞ Determine R_3 from:

$$R_3 \geq 2 \times R_2 \quad (9)$$

☞ Determine C_3 from:

$$C_3 \leq \frac{R_2 \times C_2}{20 \times R_3} \quad (10)$$

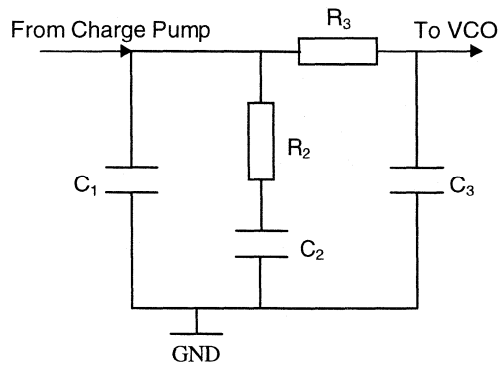
A program using this cook book method has been written for use on IBM PC (and compatibles). It is included with the three wire serial bus control software diskette. Values given by the program are approximate and the final values should be optimised. For further optimisation both computer simulation programs as well as practical experiments are required.

Capacitors with high leakage currents and other undesirable effects such as capacitance value dependant on voltage across dielectric are not preferred because of higher comparison frequency breakthrough and increased switching times. A polyester film capacitor is recommended for C_2. However in many cases high quality NP0 surface mount capacitors are adequate for values up to 100 nF.

3.2 Analysis and Simulation

For detailed analysis, optimisation and worst case design with more complex filters, use of a PLL simulation program may be needed.

Normally a stable loop with an acceptable phase noise performance and a given switching time is required. Unfortunately, these two requirements are in conflict and a compromise must be found. Generally, the optimum compromise between stability and fastest switching time is reached when the phase margin is at its maximum at the open loop gain crossover frequency.



$T_1 = (R_2 \times C_2 \times C_1) / (C_1 + C_2)$; $T_2 = R_2 \times C_2$; $T_3 = R_3 \times C_3$ if $C_2 >> C_1 >> C_3$

Fig. 27 - Third Order Loop Filter.

The phase margin is easily determined from Bode plot. A Bode plot displays the open loop transfer function magnitude and phase. Fig. 28 shows Bode plot of a fourth order loop with third order filter (see Fig. 27) and a pole in the origin due to the VCO.

The phase margin is defined as the different between 180° and the phase of the open loop transfer function at the frequency where the gain is 1 (Gain cross over). The critical point for stability is a phase margin of 0°. The factor by which the system gain would have to be increased for the phase margin to reach the critical value of 0° is called the gain margin.

The time constants in the loop filter are key to controlling the overall loop performance and phase margin. The effect of different time constants can be evaluated from the Bode diagram. The reciprocal of the time constants of the loop filter in Fig. 27 are the breakpoints in the magnitude plot of Fig. 28.

When increasing the time constant $T_3 = C_3 \times R_3$, the breakpoint $(T_3)^{-1}$ will move left and the magnitude curve will start to roll off at a lower frequency. Therefore, the greater the time constant T_3, the better the comparison frequency breakthrough is suppressed. But increasing T_3 will force the point of inflection of the phase margin curve to move to the left as well, this decreasing the phase margin and eventually reducing system stability.

By iteration and inspection of the Bode plot, adjusting the loop filter values and measuring the performance, a compromise between switching time, stability and noise can be reached. Simulation programs may give reasonable approximations of PLL behaviour, but their accuracy is limited due to the fact that many practical imperfections, non linearities and saturation effects are often not taken into account.

Phase margin between 30° and 70° is required for most applications. The larger the phase margin, the more stable the loop, but slower the transient response and hence the switching time. A loop with a low phase margin may still be stable but could exhibit oscillatory problems, associated with undamped loops which also give longer switching times and increased noise. A phase margin of 45° is a good compromise between desired stability and the other generally undesired effects.

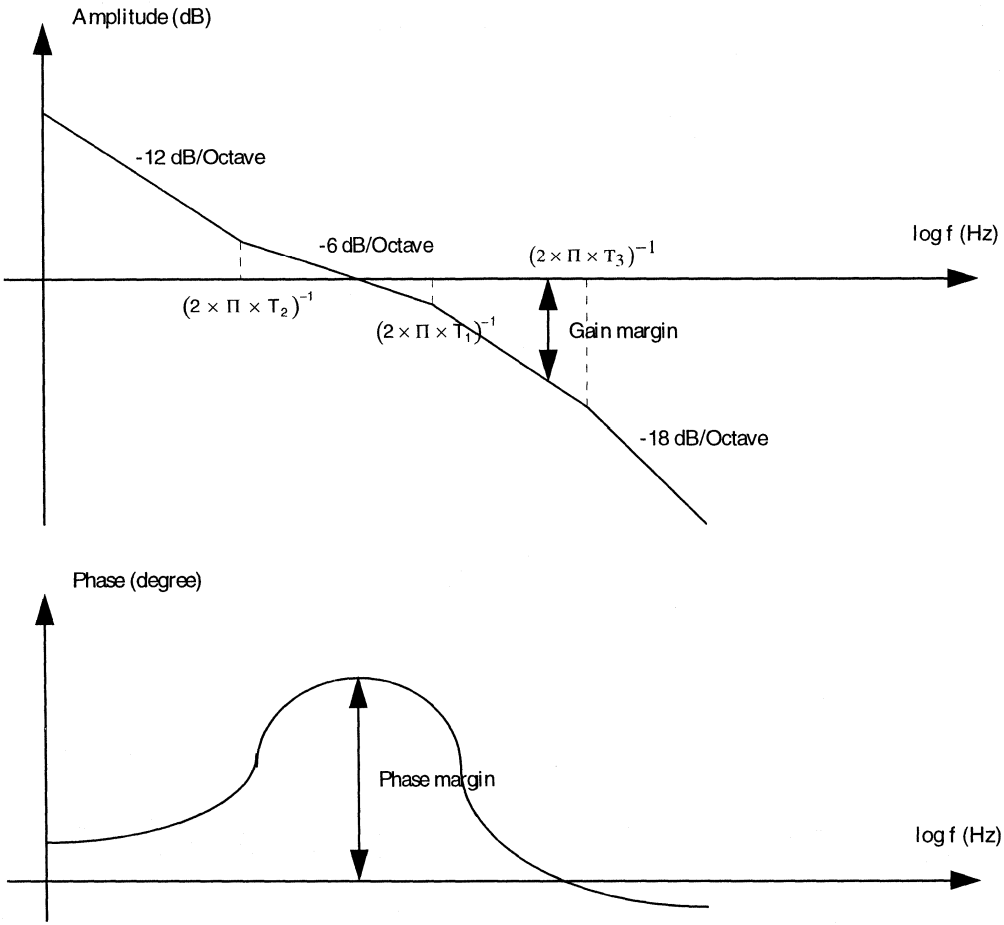


Fig. 28 - Bode Plot 4th Order Open PLL Transfer Function Magnitude and Phase.

3.3 Worked Example

In this section, a design example based on the third order PLL for GSM is shown.

As close in noise is improved by using higher charge pump gains, both charge pumps outputs (pin 2 and 3) are connected together before the loop filter.

Loop parameters relevant to meet the GSM application:

- VCO frequency f_{VCO} = 902 MHz
- Phase comparator frequency f_{PC} = 200 kHz
- Switching time t_s = 600 µs
- VCO gain K_{VCO} = 26 MHz/V
- Phase comparator gain I_{CP} = 3.6 mA/cycle

  R_{SET} = 5.6 kΩ ; With CR1 bit set to 0 and CR0 bit set to 1.

Following the basic design procedure from paragraph 3.1 yields:

I_{CP} = 3.6 mA/cycle = 18 x I_{SET} --> I_{SET} = 200 µA

R_{SET} = 1.2 / I_{SET} = 1.2 / 200 µA ≅ 5.6 kΩ

Natural frequency f_n = 2.5 / t_s = 2.5 / 600 µS = 4170 Hz

Main divider ratio N: f_{VCO} / f_{PC} = 902 MHz / 200 kHz = 4510

The main components in the loop filter are:

☞ Main capacitor $$C_2 = \frac{K_{VCO} \times I_{CP}}{w_n^2 \times N} = \frac{26e6 \times 3.6e-3}{(2 \times \Pi \times 4170)^2 \times 4510}$$

$$C_2 = 33 \text{ nF}$$

☞ Damping resistor $$R_2 = 2 \times \rho \times \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} = 2 \times 0.9 \times \sqrt{\frac{4510}{26e6 \times 3.6e-3 \times 33e-9}}$$

$$R_2 = 2.2 \text{ k}\Omega$$

☞ Filter capacitor $$\frac{C_2}{15} \leq C_1 \leq \frac{C_2}{10}$$

$$C_1 = 220 \text{ pF}$$

An extra order (R_3 and C_3) is not needed as UMA1021M charge pump leakage current and comparison frequency breakthrough are very low.

A software simulation program has been used to verify the stability of this loop filter. The phase margin is nearly maximum and equal to 61° at the gain cross over point, the requirement for basic loop stability is fulfilled as shown below.

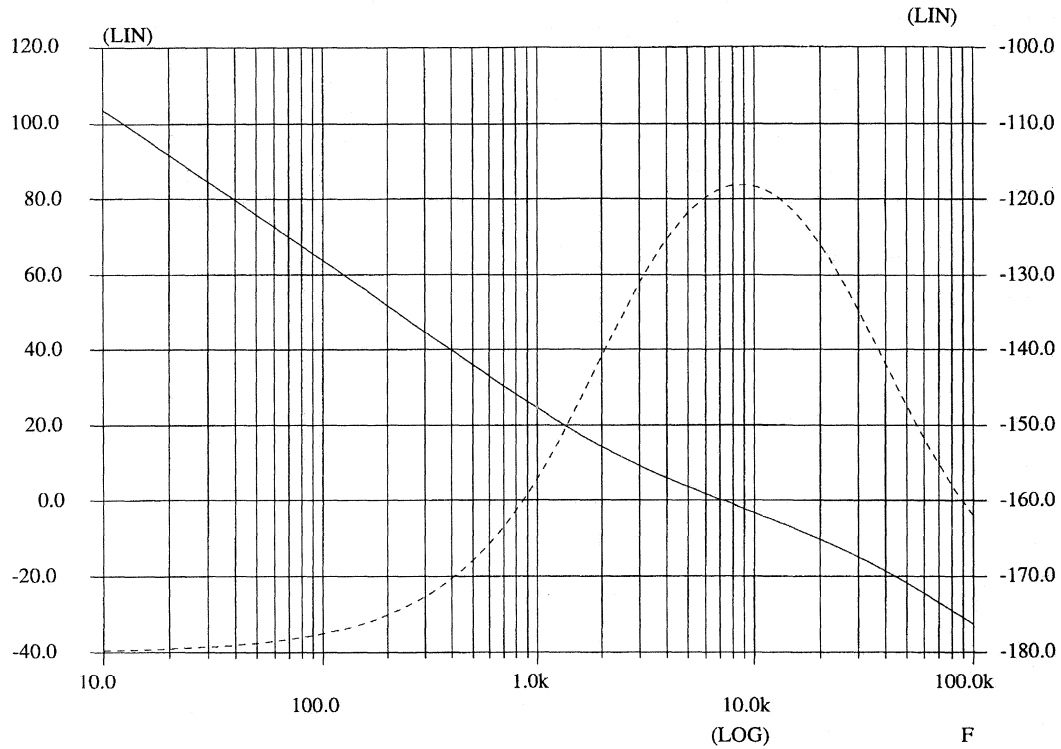


Fig. 29 - Simulated Bode Plot of Open Loop Transfer Function, Magnitude and Phase vs Frequency.

4. Measurements and typical results

Measurements

This section gives the performance of UMA1021M in different applications.

The relevant performance criteria for a synthesizer are usually:

- Close in phase noise / Integrated phase jitter
- Comparison frequency breakthrough
- Switching time

Close in noise was measured using a direct reading from the spectrum analyser and referred to 1 Hz bandwidth. This was done at a specified offset from the carrier whilst still inside the loop bandwidth. It is expressed in dBc/Hz.

Integrated phase jitter was measured on a Rohde and Schwarz Modulation Analyser in a 10 Hz to 200 kHz audio bandwidth. Residual FM (for DAMPS application) was measured using a CCITT filter.

Switching time was measured using a HP 53310A Modulation Domain Analyser (MDA) with option 031. Under the TRIGGER Menu of the MDA, "Triggered", "Ext Edge" and "Arm Only" were selected. The instrument was setup to accept an external trigger, which was the Enot (Enable) signal used for programming the synthesizer. This signal was connected to the Ext Arm input while the RF signal was fed into the Channel C. The MDA would display the frequency versus time variation of the VCO signal upon the arrival of the Enot rising edge signal.

Table 7 to Table 11 summarise the measurement results. Fig. 30 to Fig. 41 show some of the actual measurements.

Parameters			
Conditions: $V_{CC} = V_{DD} = 5$ volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		$C_1 = 2.2$ nF $C_2 = 33$ nF $C_3 = NNP^*$	 $R_2 = 2.2$ kΩ $R_3 = NNP$
VCO EX814A ALPS (5V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	26 MHz/V 902 MHz 864 - 915 MHz	
Comparison frequency f_{PC}		200 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: VTCXO TOYOCOM TCO982 (3V)		13 MHz	
Results			
Closed loop bandwidth		7.5 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 30)		-90 dBc/Hz	
Integrated phase jitter	890 MHz 902 MHz 915 MHz	5.8 mrad rms 5.9 mrad rms 5.9 mrad rms	
Comparison frequency breakthrough at 200 kHz (see Fig. 31)		88 dBc	
Switching time to within 1 kHz	890 to 915 MHz (see Fig. 32) 915 to 890 MHz (see Fig. 33)	578 µs 567 µs	

Table 7 - Demoboard Measurement Results on UMA1021M Synthesizer. GSM Application.

(*) NNP Normally Not Populated

Parameters			
Conditions: V_{CC} = V_{DD} = 5 volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		C_1 = 1.2 nF C_2 = 18 nF C_3 = 270 pF	 R_2 = 3.3 kΩ R_3 = 8.2 kΩ
VCO URAE8X812A ALPS (5V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	41 MHz/V 2082 MHz 2070 - 2095 MHz	
Comparison frequency f_{PC}		200 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: VTCXO TOYOCOM TCO982 (3V)		13 MHz	
Results			
Closed loop bandwidth		7.5 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 34)		-82.5 dBc/Hz	
Integrated phase jitter	2070 MHz 2082 MHz 2095 MHz	15.8 mrad rms 16 mrad rms 15.9 mrad rms	
Comparison frequency breakthrough at 200 kHz (see Fig. 35)		75 dBc	
Switching time to within 1 kHz	2070 to 2095 MHz 2095 to 2070 MHz	550 µs 550 µs	

Table 8 - Demoboard Measurement Results on UMA1021M Synthesizer. DCS1800 Application.

Parameters			
Conditions: $V_{CC} = V_{DD} = 3$ volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		$C_1 = 1.2$ nF $C_2 = 18$ nF $C_3 =$ NNP	 $R_2 = 2.7$ kΩ $R_3 =$ NNP
VCO URAP8x431A ALPS (2.8V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	40 MHz/V 1668 MHz 1662 - 1674 MHz	
Comparison frequency f_{PC}		300 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: VTCXO TOYOCOM TCO982		19.2 MHz	
Results			
Closed loop bandwidth		13 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 36)		-86 dBc/Hz	
Integrated phase jitter	1662 MHz 1668 MHz 1674 MHz	11.6 mrad rms 11.6 mrad rms 11.5 mrad rms	
Comparison frequency breakthrough at 300 kHz (see Fig. 37)		79 dBc	
Switching time to within 1 kHz	1662 to 1674 MHz 1674 to 1662 MHz	320 µs 315 µs	

Table 9 - Demoboard Measurement Results on UMA1021M Synthesizer. PHS Application.

Parameters			
Conditions: $V_{CC} = V_{DD}$ = 3 volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		C_1 = 680 pF C_2 = 10 nF C_3 = NNP	 R_2 = 2.2 kΩ R_3 = NNP
VCO URAEX845 ALPS (3V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	20 MHz/V 1890 MHz 1880 - 1890 MHz	
Comparison frequency f_{PC}		1728 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: Frequency Generator SMHU (R&S)		13.824 MHz	
Results			
Closed loop bandwidth		26 kHz	
Close in noise (at 2 kHz distance from carrier) (see Fig. 38)		-92 dBc/Hz	
Integrated phase jitter	1881.792 MHz 1890.432 MHz 1897.344 MHz	5.8 mrad rms 6.1 mrad rms 5.9 mrad rms	
Comparison frequency breakthrough at 1728 kHz (see Fig. 39)		79 dBc	
Switching time to within 1 kHz	1881.792 to 1897.344 MHz 1897.344 to 1881.792 MHz	170 µs 170 µs	

Table 10 - Demoboard Measurement Results on UMA1021M Synthesizer. DECT Application.

Parameters			
Conditions: $V_{CC} = V_{DD} = 5$ volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		$C_1 = 1.5$ nF $C_2 = 22$ nF $C_3 =$ NNP	 $R_2 = 10$ kΩ $R_3 =$ NNP
VCO MQE001 MURATA (4.2V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	11 MHz/V 836 MHz 824 - 849 MHz	
Comparison frequency f_{PC}		30 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: VTCXO TOYOCOM 982P (3V)		15.36 MHz	
Results			
Closed loop bandwidth		4 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 40)		-81.4 dBc/Hz	
Integrated phase jitter FM demodulation ; CCITT filter	824 MHz 836 MHz 849 MHz	8.5 Hz rms 8.6 Hz rms 8.6 Hz rms	
Comparison frequency breakthrough at 30 kHz (see Fig. 41)		75 dBc	
Switching time to within 2.5 kHz	824 to 849 MHz 849 to 824 MHz	2.05 ms 1.98 ms	

Table 11 - Demoboard Measurement Results on UMA1021M Synthesizer. DAMPS Application.

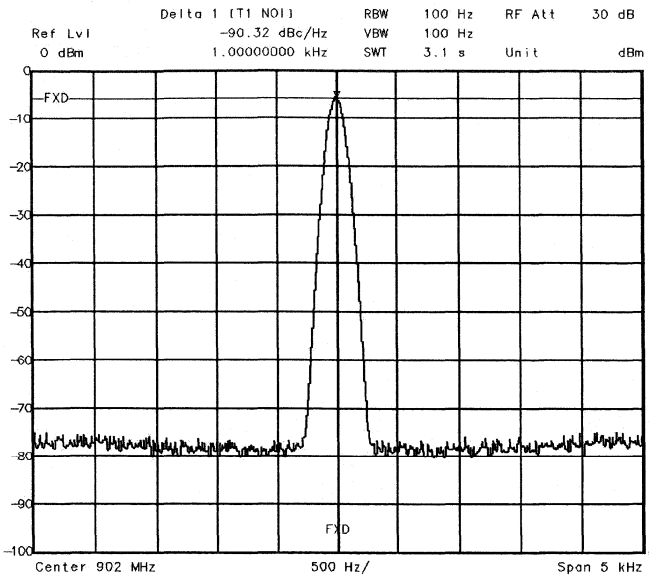


Fig. 30 - UMA1021M Synthesizer Output Spectrum - Close in Noise (GSM Application).

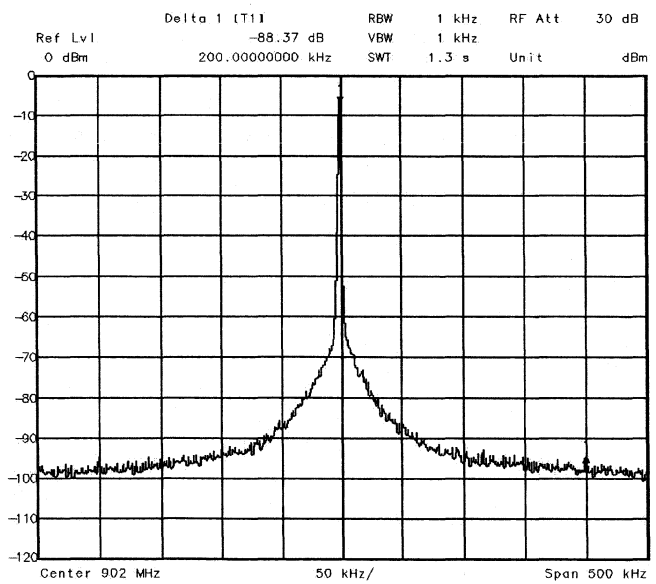


Fig. 31 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (GSM Application).

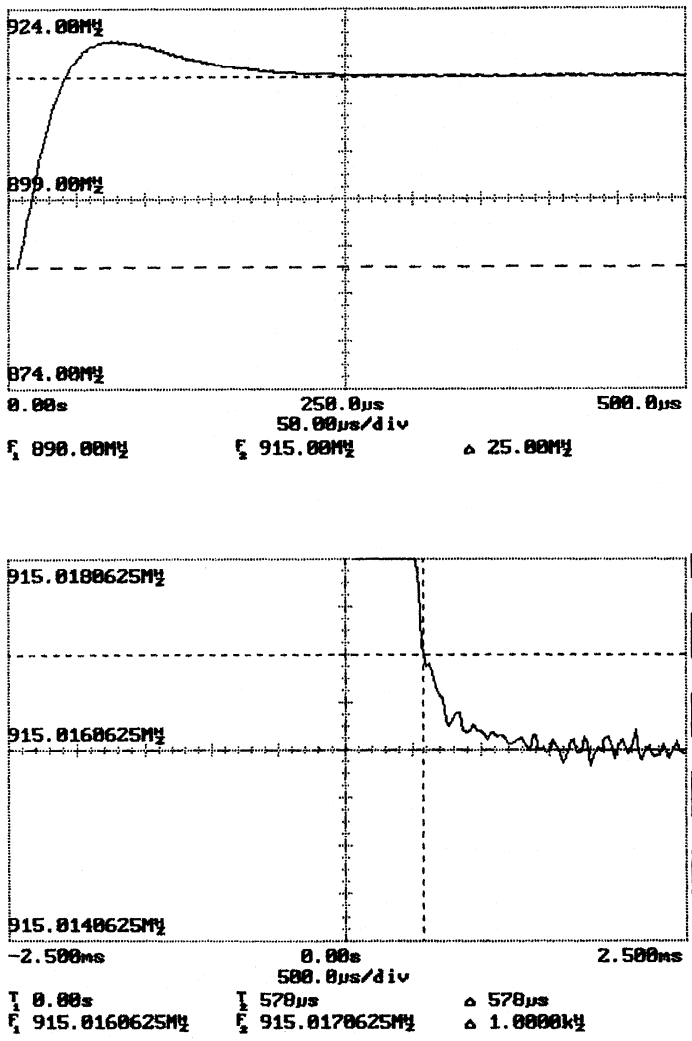
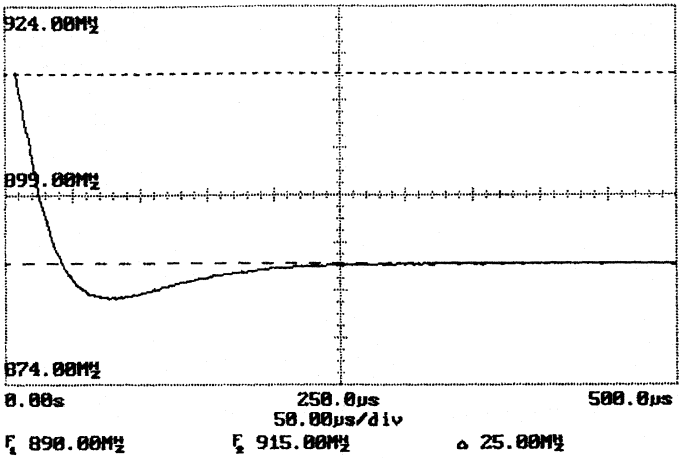


Fig. 32- Settling Time (890 to 915 MHz Step to Within 1 kHz).



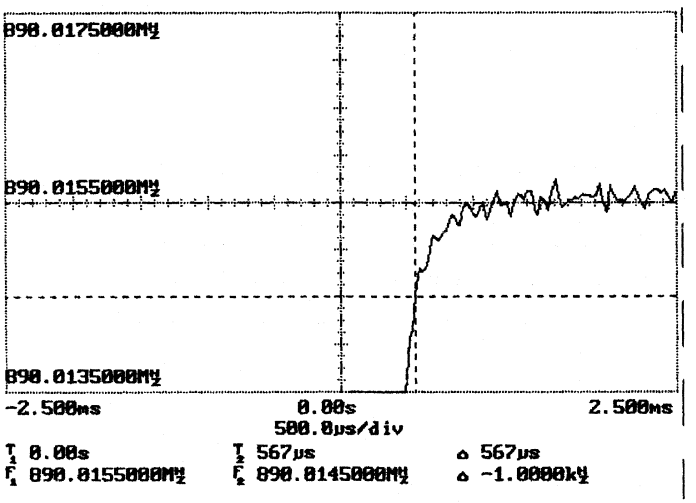


Fig. 33- Settling time (915 to 890 MHz Step to Within 1 kHz).

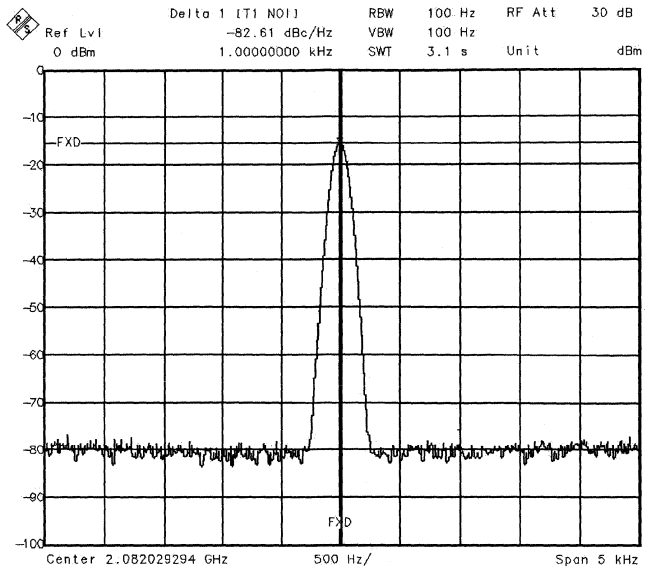


Fig. 34 - UMA1021M Synthesizer Output - Close in Noise (DCS Application).

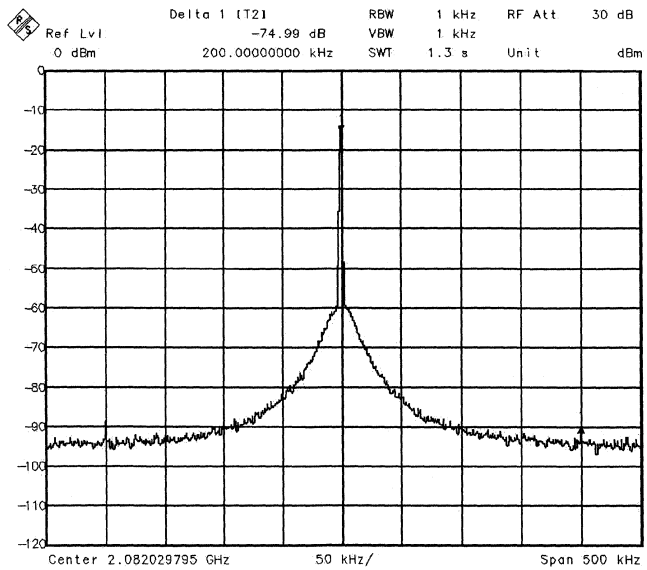


Fig. 35 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (DCS Application).

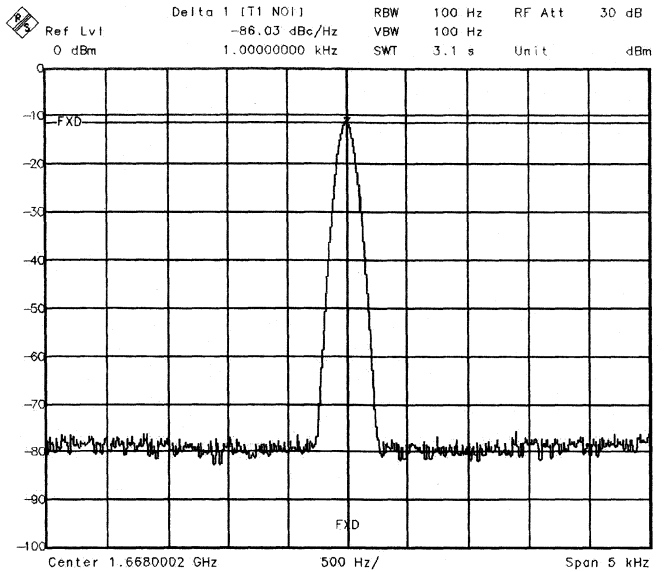


Fig. 36 - UMA1021M Synthesizer Output - Close in Noise (PHS Application).

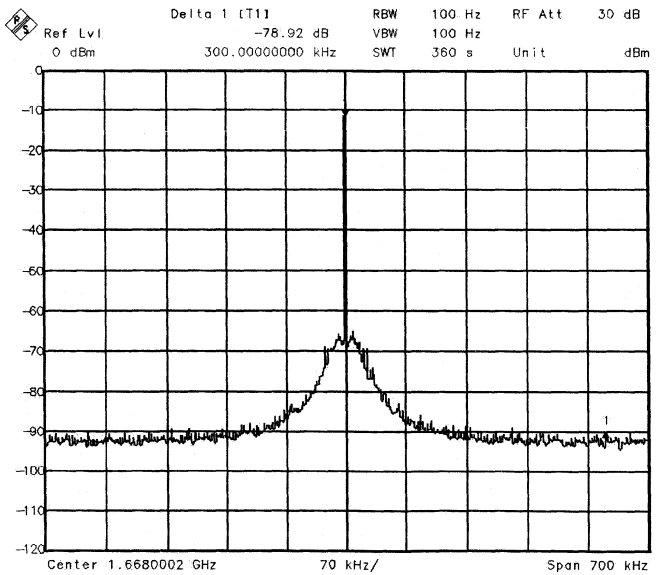


Fig. 37 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (PHS Application).

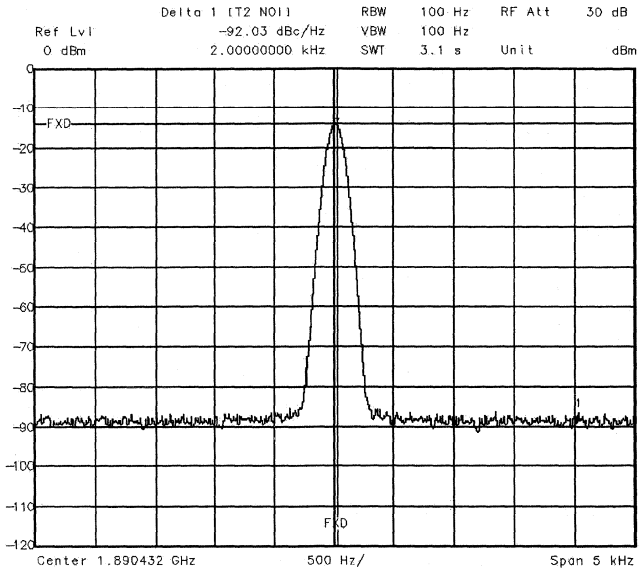


Fig. 38 - UMA1021M Synthesizer Output - Close in Noise (DECT Application).

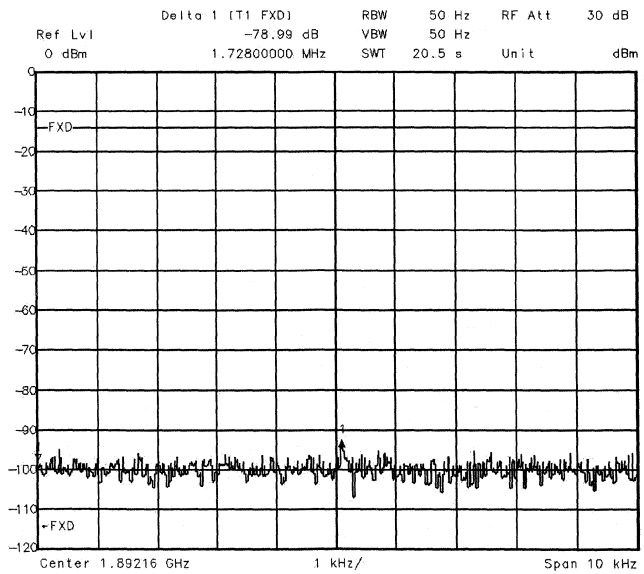


Fig. 39 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (DECT Application).

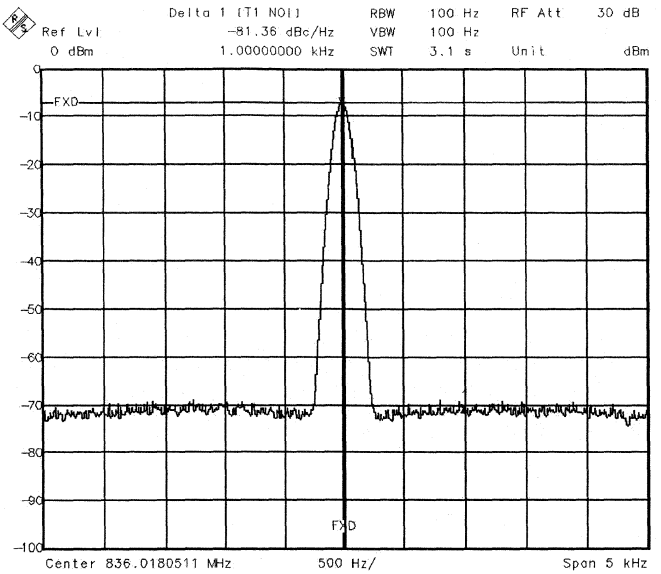


Fig. 40 - UMA1021M Synthesizer Output - Close in Noise (DAMPS Application).

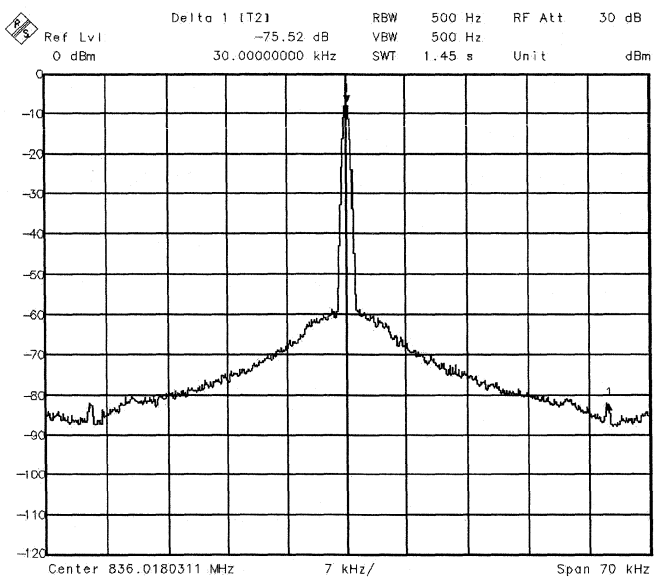


Fig. 41 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (DAMPS Application).

5. Frequently Asked Questions

Question 1: How can the synthesizer noise be improved?

Answer: Five things can be done to improve the synthesizer noise.

1/ Use a higher crystal frequency. Doubling the reference frequency can improve the close in noise by 3 dBc/Hz.

2/ With a VTCXO as the reference frequency, use the pin XTALA as input and decouple to ground the pin XTALB (see explanations next question).

3/ Use the bigger charge pump current. In a typical GSM application, a difference of 7 dB has been measured between the lowest charge pump current (0.2 mA) and the biggest (3.6 mA). It is also recommended to use the lowest external resistor (5.6 kΩ), in order that the charge pump works with the highest current density.

4/ Use a narrower loop filter. But this increases the switching time.

5/ Ensure that the supply is well decoupled.

Number 4 does not improve the close in noise, just the total phase noise. Other points can improve the close in noise and also the total phase noise of the PLL.

Question 2: Do you recommend the use of a particular reference input (XTALA or XTALB)?

Answer: The pin XTALA (and so the reference divider) is driven by the rising edge of the reference signal, whilst the pin XTALB is driven by the falling edge.

Since this signal is the reference in term of frequency but also purity, the reference input must be chosen according to the phase jitter of the edge. The better the phase jitter of the reference edge, the better will be the total close in noise (in the loop bandwidth).

Normally with a VTCXO the rising edge has a better jitter than the falling edge. So we recommend to use the pin XTALA with such a VTCXO.

Question 3: What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?

Answer: The phase detector gain is equal to the charge pump output current I_{CP} divided by 2π since the phase detector covers 2π range. However, when using the design formulas, the phase detector gain be replaced directly by I_{CP} (or $I_{CP} + I_{CPF}$ if both charge pumps are enabled) because the 2π factor will be cancelled out by the 2π also in the VCO gain, when given in Hz/volt.

Question 4: What kind of main capacitor should be used in the loop filter?

Answer: Higher leakage current raises comparison frequency breakthrough and the memory effect of some dielectric (COG, X7R series) or, worse, electrolytic types can degrade the settling time. A polyester film capacitor is recommended for the main capacitor of the loop filter.

Question 5: How to use the synthesizer with V_{DD} < 4.5 V whereas DATA, CLK and Enot signals are at 5 V logic?

Answer: Because of protection against electrostatic discharge (see section 2.7), the input voltage for these logic pins can not be greater than V_{DD} + 0.3 V. An interface between the microcontroller and the synthesizer is then needed to reduce voltage at serial bus pins. A voltage divider using two resistors is a simple and cheap solution to implement.

The design of this interface involves performance compromise between the current consumption and the programming speed, which depend on the resistor values in the voltage divider and the parasitic capacitance from the demonstration board.

Question 6: Can UMA1021M be used in open loop modulation?

Answer: Two methods of open loop modulation are briefly described.

☞ Method 1: Only the fast charge pump is used, and it is enabled/disabled using the pin FAST. The slow charge pump (pin CP) is grounded. An internal circuit synchronises the FAST signal with the fast charge pump correction current pulses. This avoids opening the loop when the fast charge pump is still active, which could cause a frequency drift. After the loop is opened, the UMA1021M synthesizer can then be powered down to reduce consumption.

Some precautions must be taken when the fast charge pump is switched off. A parasitic capacitance, due to the integrated circuit and the printed circuit, exists between the FAST and CPF pin. When the signal is sent to the FAST pin, a coupling through the parasitic capacitance results in a VCO frequency shift. This problem can be solved by decreasing the slope of the FAST signal with an RC filter.

The loop parameters indicated in Table 10 have been used for following open loop measurements. Fig. 42 shows a frequency drift of less than 800 Hz when the fast charge pump is switched off in a typical DECT application.

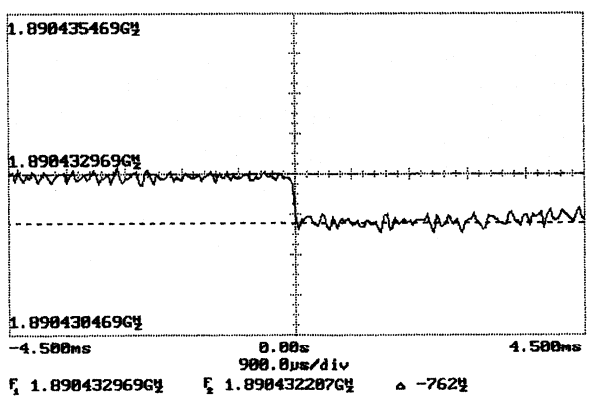


Fig. 42 - Open Loop Modulation: the Fast Charge Pump is Switched Off.

☞ Method 2: The loop is opened by powering down (PON pin) the principal synthesizer directly. The signal sent to the PON is also internally synchronised with the charge pumps to avoid powering down the synthesizer whilst they are still active. This method has additional advantage of reducing the synthesizer current consumption to nearly zero.

Two problems can occur when a synthesizer is powered down.

- The first is known as "Load Pulling". When the synthesizer is switched off, its RF input impedance may change and then an unintended jump in frequency is possible, if the VCO is susceptible to load changes. This problem is negligible with the UMA1021M synthesizer (see Fig. 43).
- The second problem is called "Pushing". The frequency of the VCO moves with changes in its supply voltage. When the principal synthesizer is powered down, it may temporally affect the supply voltage. Proper supply decoupling will attenuate it.

Fig. 43 shows a frequency jump of less than 500 Hz and a frequency drift of less than 600 Hz when the synthesizer is powered down in a DECT application.

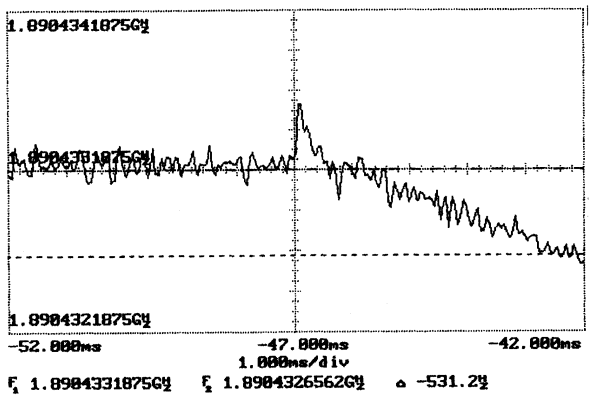


Fig. 43 - Open Loop Modulation: the Synthesizer is Powered Down.

Question 7: Can I anticipate the close in noise with any application?

Answer: Different experiments show that when using the UMA1021M, the main divider follows a 20log(N) (6 dB/octave) slope (i.e. when doubling the RF, you degrade the close in noise by 6 dB), whilst with the reference divider the noise floor is seen to follow a 10log(N) (3 dB/octave) slope.

The expected close in noise of any application can be extrapolated from the results of the GSM application (RF = 902 MHz, F_{CP} = 200 kHz, close in noise = -90 dBc/Hz) with the following rule:

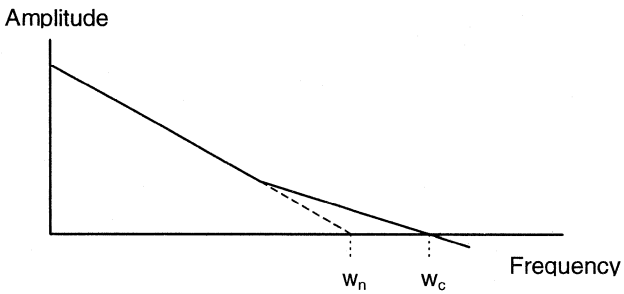
$$\text{Close in Noise (expected)} = -90\text{dBc / Hz} + 20\log\left(\frac{RF}{902\text{MHz}}\right) - 10\log\left(\frac{F_{CP}}{200\text{kHz}}\right)$$

6. Appendixes

6.1 PLL terms

The following is a brief glossary of frequently encountered terms in the PLL literature.

- **Natural frequency w_n**: the natural frequency of the loop. This is the frequency at which the loop would theoretically oscillate if the damping factor was zero.
- **Open loop cross-over frequency w_c**: this is the frequency at which the open loop gain is unity. It is useful in determining the phase margin and hence the stability.



- **Damping coefficient**: ρ can be used as a measure of the stability in second order systems. It is seldom used as a direct measure of stability in higher order designs.
- **Order of the loop**: the order of the loop is the highest power of s (s=jw) in the denominator of the open loop transfer function. The example, below, shows a second order loop.

$$G(s) \times H(s) = (K_{VCO} \times I_{CP}) \times \frac{(s \times \tau_2 + 1)}{(N \times C \times s^2)}$$

- **Type of the loop**: the type of control system formed is defined by the number of perfect integrators in the loop. In the example, above, the loop is a type two system.
- **Phase margin Φm**: the phase margin, in degrees, is expressed as $\Phi m = \Phi(w_c)+180$ where $\Phi(w_c)$ is the open loop phase shift at the frequency w_c.
- **SSB phase noise or close in noise**: it is the noise level within the loop bandwidth relative to carrier at a given frequency offset. It is referred to a 1 Hz bandwidth. It is expressed in dBc/Hz.
- **Integrated phase jitter or residual FM**: this is another measure of the noise performance of a signal source. This measure of integrated noise is usually specified over a particular audio bandwidth, e.g. 10 Hz to 200 kHz. It is expressed in degrees rms. An ideal synthesizer would have zero integrated phase jitter.
- **Spurious**: this defines the spectral purity of the oscillator. Common sources of spurious are the comparison frequency and harmonics. Comparison frequency breakthrough is generated by leakage in the loop filter components, VCO variable capacitor, printed circuit or the charge pump.
- **Settling time or switching time**: this indicates the time for a given frequency jump to be within a specified distance (frequency or phase) from target value.

6.2 Basic PLL transfer function

Fig. 44 shows the block diagram of a basic control loop.

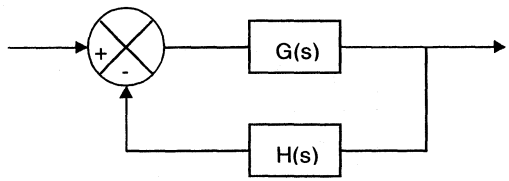


Fig. 44 - Block Diagram of a Loop.

In open loop, the transfer function is $H(s) \times G(s)$ (a)

In closed loop, the transfer function is $\frac{G(s)}{1+(G(s)+H(s))}$ (b)

If we apply these transfer functions to the phase loop in Fig. 45, with equations expressed in Laplace notation.

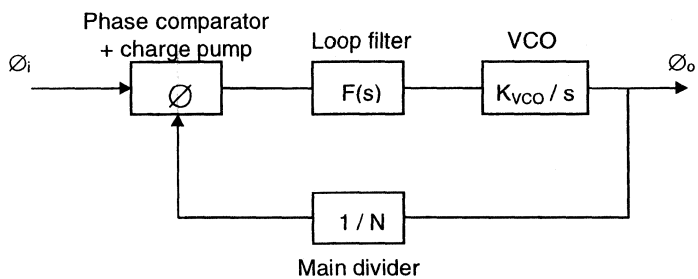


Fig. 45 - Block Diagram of a Phase Locked Loop.

$$G(s) = \frac{I_{CP} \times K_{VCO} \times F(s)}{s} \quad (c)$$

$$H(s) = \frac{1}{N} \quad (d)$$

The PLL open loop transfer function is $\frac{I_{CP} \times K_{VCO} \times F(s)}{s \times N}$ (e)

The PLL closed loop transfer function is

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{K_{VCO} \times I_{CP} \times F(s)/s}{1+\frac{K_{VCO} \times I_{CP} \times F(s)}{s \times N}} = \frac{N \times K_{VCO} \times I_{CP} \times F(s)}{(s \times N)+(K_{VCO} \times I_{CP} \times F(s))} \quad (f)$$

Basic performance of PLL is determined by R_2 and C_2 (see Fig. 27) in the loop filter.

Note: When introducing more components in the loop filter, the expression for the transfer function becomes a lot more complicated. Anyway, this design can serve as a starting point for even more complicated loop filters.

The transfer function of this simple second order loop filter is

$$F(s) = R_2 + \left(\frac{1}{s \times C_2}\right) = \left[\frac{(s \times R_2 \times C_2) + 1}{s \times C_2}\right] \qquad \text{(g)}$$

Then the closed transfer function is

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{N \times K_{VCO} \times I_{CP} \times F(s)}{(s \times N) + (K_{VCO} \times I_{CP} \times F(s))} = \frac{N \times K_{VCO} \times I_{CP} \times \frac{(s \times R_2 \times C_2) + 1}{s \times C_2}}{(s \times N) + (K_{VCO} \times I_{CP} \times \frac{(s \times R_2 \times C_2) + 1}{s \times C_2})}$$

$$= \frac{N \times ((s \times R_2 \times C_2) + 1))}{\frac{s^2 \times C_2 \times N}{K_{VCO} \times I_{CP}} + (s \times R_2 \times C_2) + 1} \qquad \text{(h)}$$

If we compare the denominator of (h) with $\frac{s^2}{w_n^2} + \frac{2 \times \rho \times s}{w_n} + 1$

We find the equations shown below:

$$w_n = \sqrt{\left(\frac{K_{VCO} \times I_{CP}}{C_2 \times N}\right)} \qquad \text{(i)} \Rightarrow \text{(1)}$$

$$\rho = \frac{w_n \times R_2 \times C_2}{2} \qquad \text{(j)}$$

$$R_2 = 2 \times \rho \times \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} \qquad \text{(k)} \Rightarrow \text{(2)}$$

6.3 Demonstration board documentation: Guidance for assembly and operation

The demonstration board is an universal tool to demonstrate and evaluate the UMA1021M under various conditions.

Together, with the Philips 3-Wire bus and the UMA1021M demonstration software, a quick and easy start to evaluation is provided. The enclosed part list corresponds to a GSM application. However, the demoboard may easily be configured for other digital cellular or cordless systems like DCS1800, PHS, etc...

We hope that you will find no problems in realising the evaluation set-up and will come quickly to an application that fits perfectly to your needs.

Assembly

Assembly is done according to the documentation which comes with the demonstration board. Please note that the board may be assembled with VCO's of different style. The existing version of the board can hold surface mount VCO's (e.g. ALPS URAX8, Murata MQE001 type). Since the VCO and the VTCXO use a common on-board supply rail, it is recommended to select both components with the same supply voltage specification.

The loop filter design depends on the system requirements and the VCO's used. A loop filter calculation program has been written for use on IBM PC. It is included with the three wire bus control software diskette (« ToolICalculate filter » menu option). It uses the same cook book method as described on the paragraph 3.1.

The supplied circuit diagram corresponds to a typical GSM system. A VCO sensitivity of about 26 MHz/V and a typical comparison frequency of 200 kHz have been assumed. The charge pump current has been selected to 3.6 mA (CR1 bit set to 0, CR0 bit set to 1). The loop filter is the one calculated in the worked example. The parameters and measurement results are summarised in section 4 (Table 7 and Fig. 30 to Fig. 33).

Board configuration

Two regulators allow the analog supply (V_{CC}) and the digital voltage (V_{DD}) to be supplied independently. The VCO and the VTCXO are supplied by the analog voltage.

The digital input POL allows to select the polarity of power on inputs, POL is grounded for power on to be active low and POL is supplied to V_{DD} for power on to be active high. The demonstration board is configured with the latter.

A VTCXO or an external generator can be used as the reference. On the demonstration board, The VTCXO drives the reference divider via the pin 16. If an external generator is used, the resistor R18 must be removed and the resistor R19 grounded with a 10 kΩ value.

Getting started

1. Connect the Philips 3-wire interface board to the serial printer port (LPT1) of your PC. Copy the two files (BUS3WIRE.WB and BUS3WIRE.EXE) onto your hard disk or run the software from the disk. Type BUS3WIRE to start. Select UMA1021M option in the DEVICE TYPE menu. Verify that the displayed window is well configured as you wish.
2. Connect the interface card with the UMA1021M demonstration board.
3. Connect the board to a 7.5V well regulated and low noise power supply.
4. The UMA1021M demonstration board is operational now and the PLL should be locked.
5. Start your synthesizer evaluation...

If you need assistance or do have any questions or comments don't hesitate to call your local Philips Semiconductors representative.

Ref.	Value/Type	Size	Ref.	Value/Type	Size
R1	100 kΩ	0805 SMD	C1	2.2 nF	0805 SMD
R2	0 Ω	0805 SMD	C2	NNP	0805 SMD
R3	2.2 kΩ	0805 SMD	C3	33 nF	0805 SMD
R4	0 Ω	0805 SMD	C4	NNP	0805 SMD
R5	12 Ω	0805 SMD	C5	4.7µ/10V	Tant. chip cap.
R6	12 Ω	0805 SMD	C6	100 nF	0805 SMD
R7	18 Ω	0805 SMD	C7	100 pF	0805 SMD
R8	18 Ω	0805 SMD	C8	100 nF	0805 SMD
R9	18 Ω	0805 SMD	C9	56 pF	0805 SMD
R10	56 Ω	0805 SMD	C10	56 pF	0805 SMD
R11	100 k Ω	0805 SMD	C11	33 pF	0805 SMD
R12	NNP (*)	0805 SMD	C12	33 pF	0805 SMD
R13	100 k Ω	0805 SMD	C13	33 pF	0805 SMD
R14	12 Ω	0805 SMD	C14	100 pF	0805 SMD
R15	12 Ω	0805 SMD	C15	100 nF	0805 SMD
R16	12 Ω	0805 SMD	C16	1 nF	0805 SMD
R17	12 Ω	0805 SMD	C17	1 nF	0805 SMD
R18	10 k Ω	0805 SMD	C18	4.7 µF / 10 V	Tant. chip cap.
R19	NNP	0805 SMD	C19	100 nF	0805 SMD
R20	1.5 k Ω	0805 SMD	C20	22 pF	0805 SMD
R21	10 k Ω	0805 SMD	C21	100 pF	0805 SMD
R22	10 k Ω	0805 SMD	C22	100 nF	0805 SMD
R23	5.6 k Ω	0805 SMD	C23	100 nF	0805 SMD
R24	100 k Ω	0805 SMD	C24	4.7 µF / 10 V	Tant. chip cap.
R25	4.7 k Ω	0805 SMD	C25	4.7 µF / 10 V	Tant. chip cap
R26	1.5 k Ω	0805 SMD	C26	100 nF	0805 SMD
R27	4.7 k Ω	0805 SMD	C27	4.7 µF / 10 V	Tant. chip cap
R28	1.5 k Ω	0805 SMD	IC1	UMA1021M	SSOP20
R29	12 Ω	0805 SMD	IC2	LM317LZ	TO92
XTAL	13 MHz	TOYOCOM	IC3	LM317LZ	TO92
VCO	URAE8X814A	ALPS			

Table 12 - Part List for UMA1021M Demonstration Board (GSM Application).

(*) NNP: Not Normally Populated

X1: Out of lock detector

X2: RF output 50Ω

X3: 3-Wire Bus Control

X4: External reference input

X5: Supply

J1: activates fast charge pump

J2: controls power down for the synthesizer

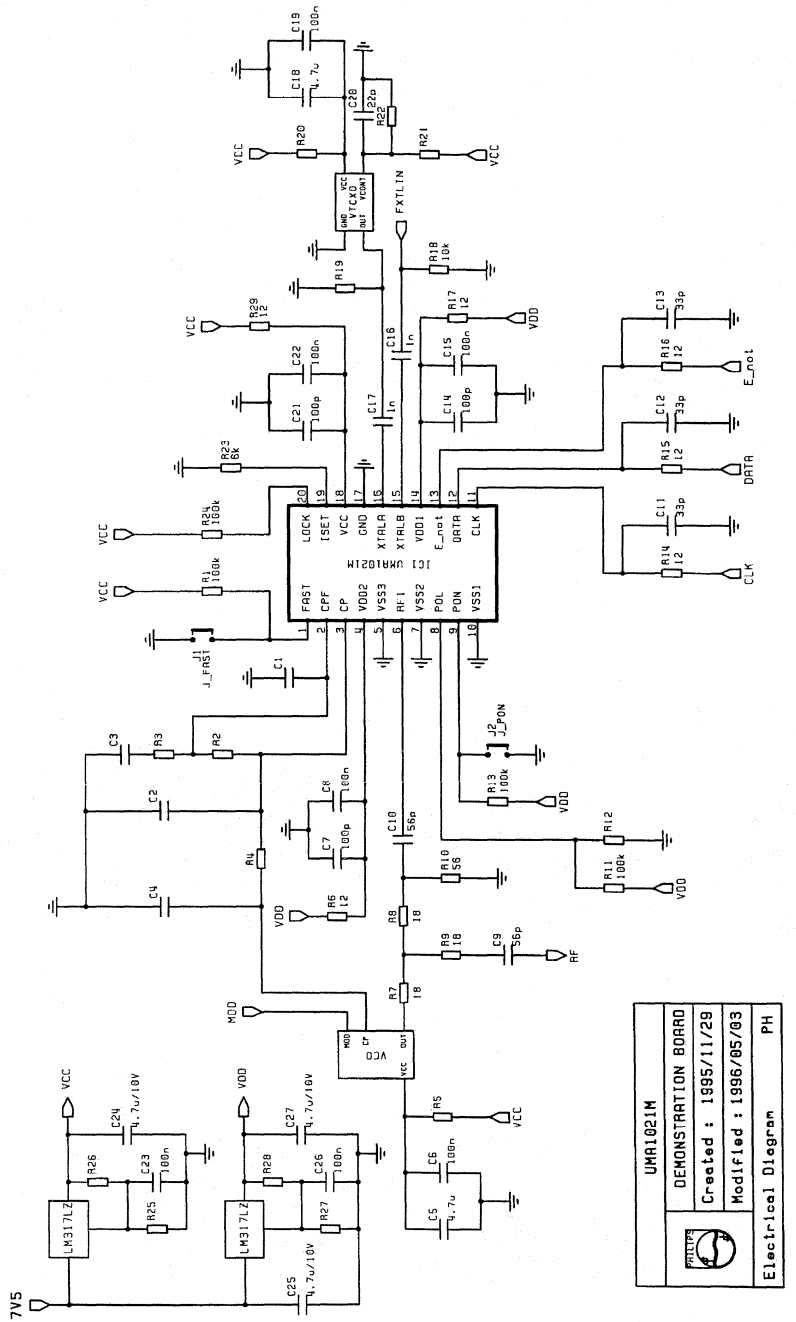


Fig. 46 - Demonstration Board Circuit Diagram.

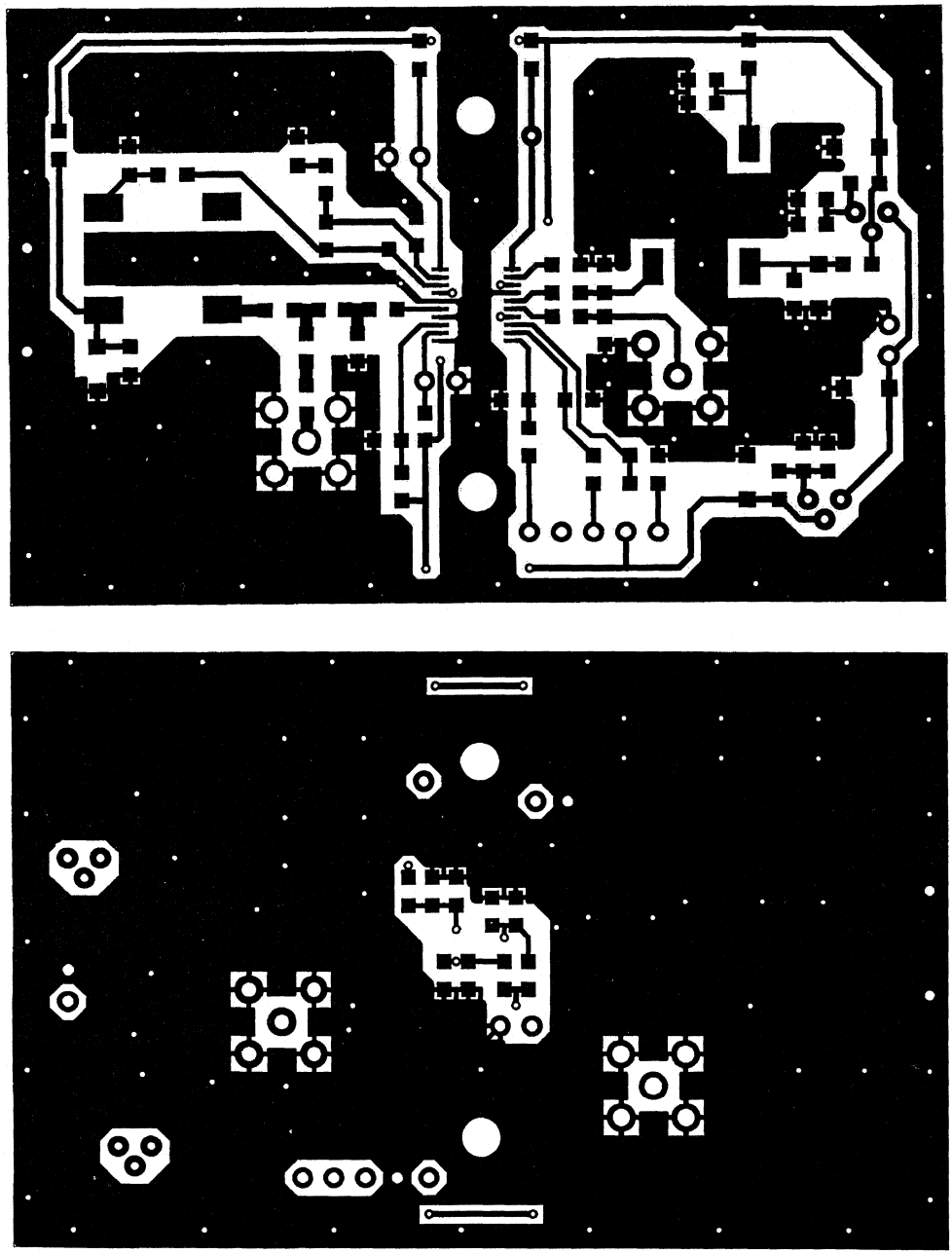


Fig. 47 - Demonstration Board pcb Layout.

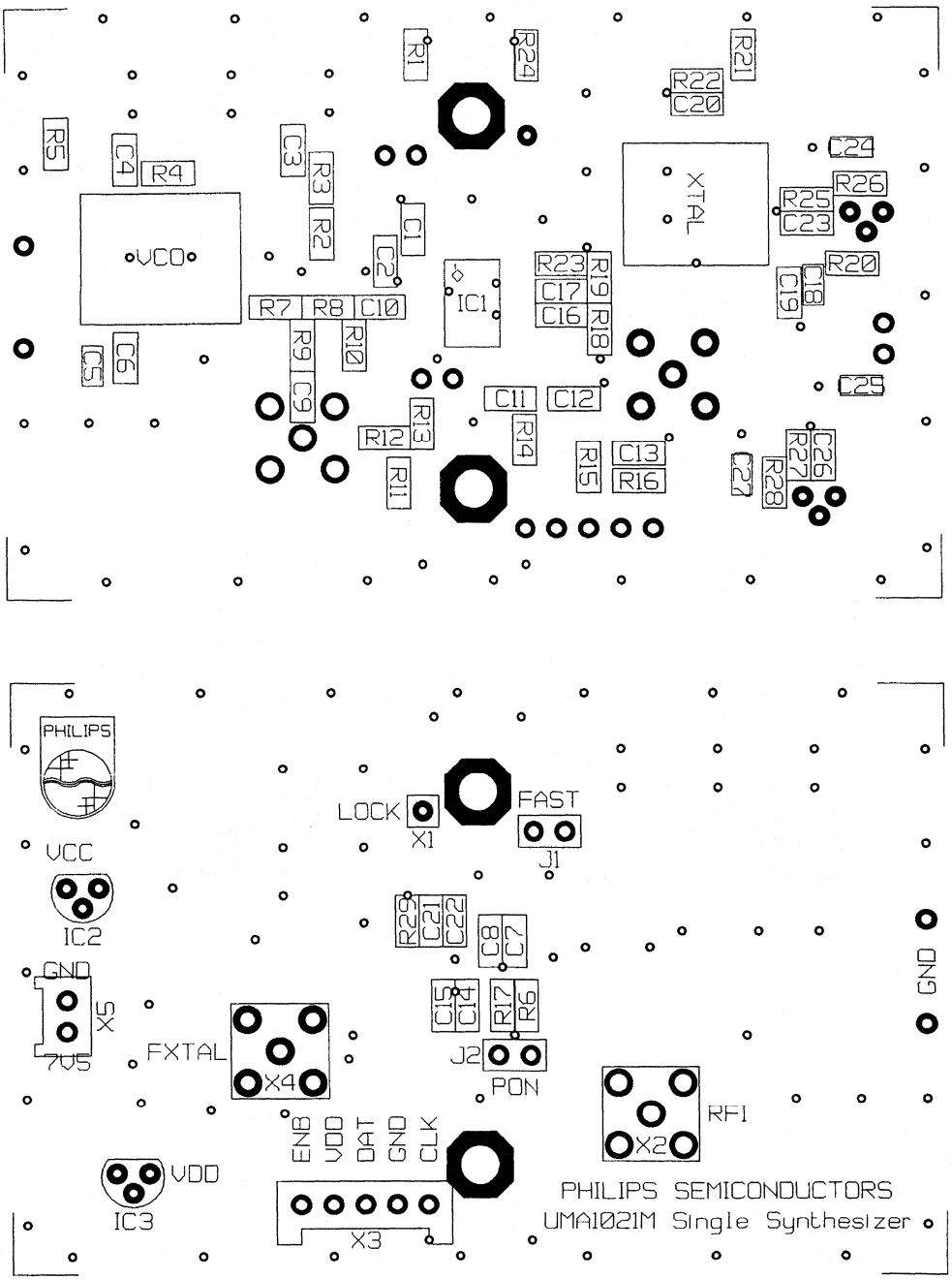


Fig. 48 - Demonstration Board Placement of Components.

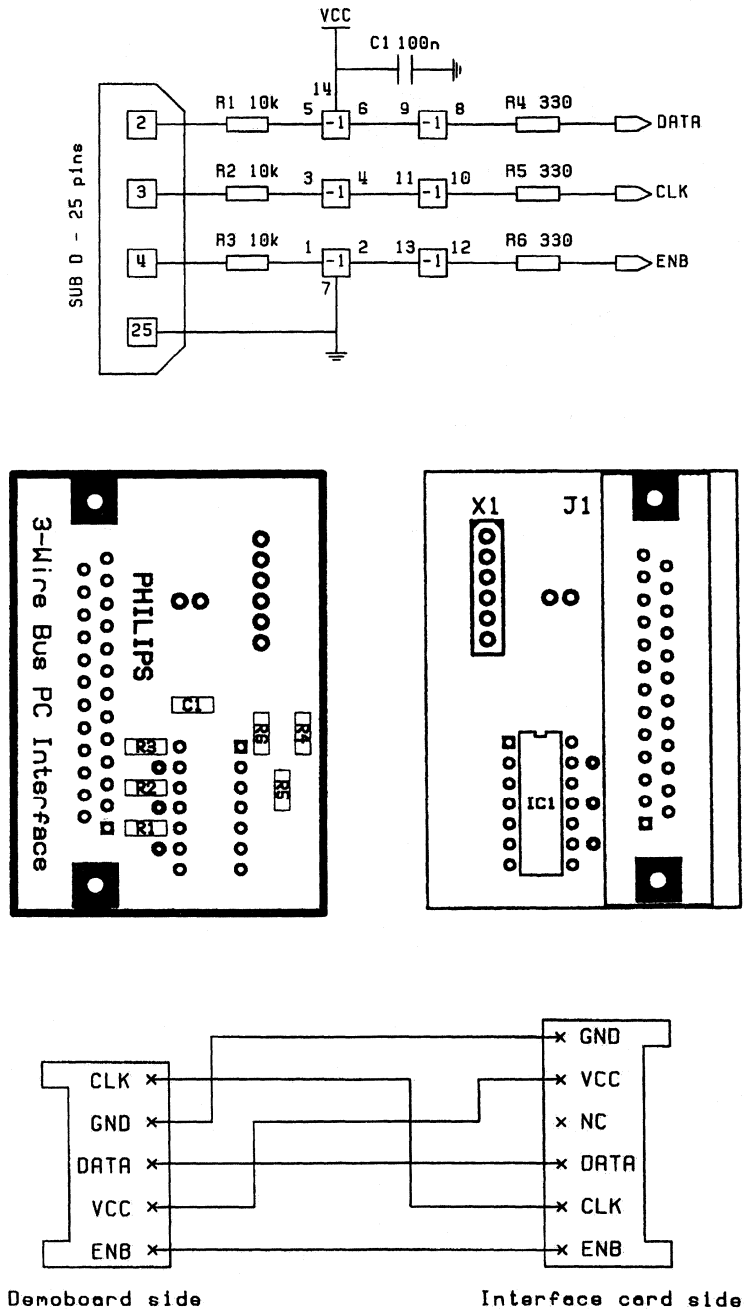


Fig. 49 - Interface Card pcb Layout and Cable Connection.

7. References

[1] Product specification UMA1021M, Philips Semiconductors, 28 August 1996.

[2] Gardner, Floyd M. Phase lock Techniques, 2nd ed, Wiley, New York. 1980.

[3] Rohde, Ulrich, L. Digital PLL Frequency Synthesizers, Theory and Design, Prentice-Hall, Englewood Cliffs, New Jersey 1983.

CGY2030M DECT power amplifier

Application Note

Summary

This report is intended to provide support for designing power amplifier for DECT applications.

It contains a description of the power amplifier as well as a brief overview of interstage and input /output matching .

An application example of the CGY2030M is given by means of board description for testing ,recommendations for use ,measurement results ,and performances.

Some explanations concerning the self biasing specificity of this circuit are also available in the document.

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1. INTRODUCTION

This note describes the application of RF monolithic GaAs device in plastic SMD packages for DECT power amplifier.

Their main features are:

-low cost

-100% SMD

-high performance

-low voltage operation

-possible operation without negative bias for the gates

2. PINNING

The pinning is shown in Fig.1.

SYMBOL	PIN	DESCRIPTION
VGG2	1	fourth stage gate bias input voltage
GND	2 to 4	ground
VDD2	5	drain second stage and supply
GND	6 and 7	ground
VDD1	8	drain first stage and supply voltage 1
RFI	9	PA input
VGG1	10	first second and third stages gate bias input voltages
GND	11 and 12	ground
VDD3	13	drain third stage and supply voltage 3
GND	14 and 15	ground
RFO/ VDD4	16	PA output and supply voltage 4

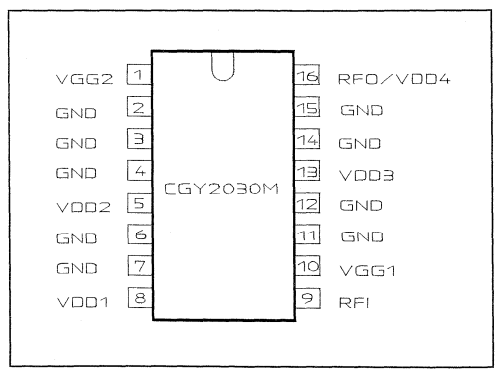

Fig. 1 Pin configuration

3. CIRCUIT DESCRIPTION

3.1 Power amplifier

The amplifier is based on a monolithic integrated four stages device using GaAs FET technology in a plastic package.
This device is able to deliver 27 dBm with 3.2 V drain operation.
As briefly described in Fig.2. this device exhibits inter stage matching circuits implemented simultaneously both on board and in the package on chip.Each matching consists of a series,parallel combination of elements.The series elements are generally capacitive (MIM capacitors on chip) while the parallel ones can be inductive or capacitive.Further more the parallel matching networks include a bias path for the drains of the different stages.
The input and output matching circuits are implemented on board.
When built on a low cost printed circuit board ,the amplifier is associated with a switching circuit for pulsed applications.This one provides the suitable ramping and switching time for DECT applications.

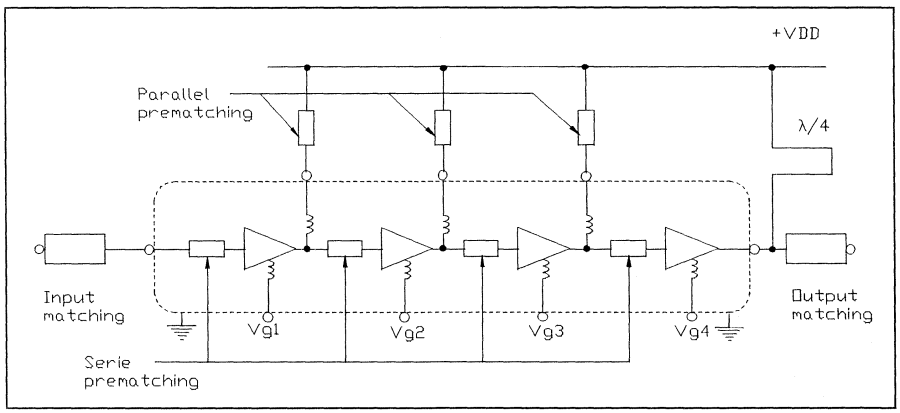

Fig. 2 Power amplifier

3.2 Interstage matchings

The general philosophy used for interstage matching is described when looking at the Fig.3.

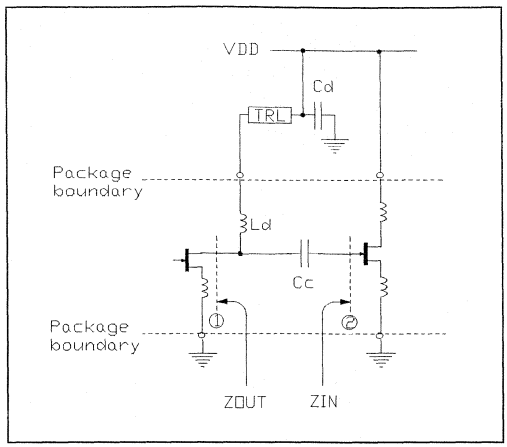

Fig. 3 Interstage matching

The aim is to match the input impedance Zin from a stage in the reference plane 2 to the output impedance Zout of the previous one in the reference plane 1.
This can be accomplished with the interstage coupling capacitor Cc(MIM) on chip ,the bonding wire between the drain and the package lead ,the external transmission line TRL and the decoupling capacitor Cd.
The only parameters that can be tuned are external to the package because Ld (bonding wire) and Cc are fixed values that cannot be adjusted.
As Zin ,Zout are known by simulation with enough accuracy ,it is relatively easy to adjust Cd and TRL (width and length) for a perfect matching between Zin and Zout.

3.3 Drain switching circuit

When used in DECT applications the power amplifier needs to be switched on and off by means of external series bipolar or MOS transistors.
For this purpose we use a double switch as described in Fig.4.

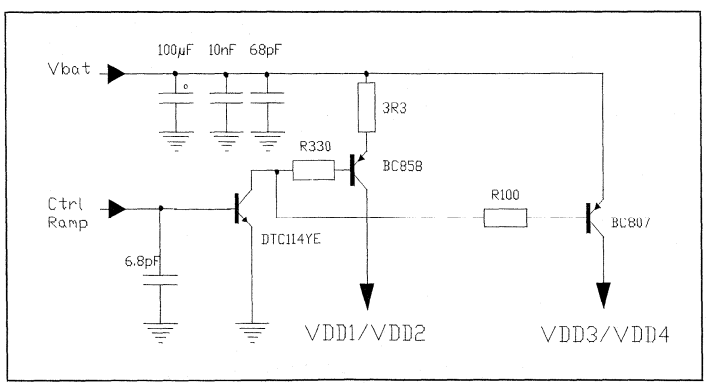

Fig. 4 Drain switching circuit

The reason why we use two PNP bipolar transistors (one for the first two stages and one for the last two ones) is that ,in order to avoid transient high peak current and to insure smooth power ramp-up , the two last stages must be switched on with some delay with respect to the first two ones.
This is accomplished with separated switches and with different time constants for the first and second stages on one hand and for the third and fourth stages on the other hand.
To understand how this delay can be introduced ,let's consider the equivalent circuit of one switch in Fig.5

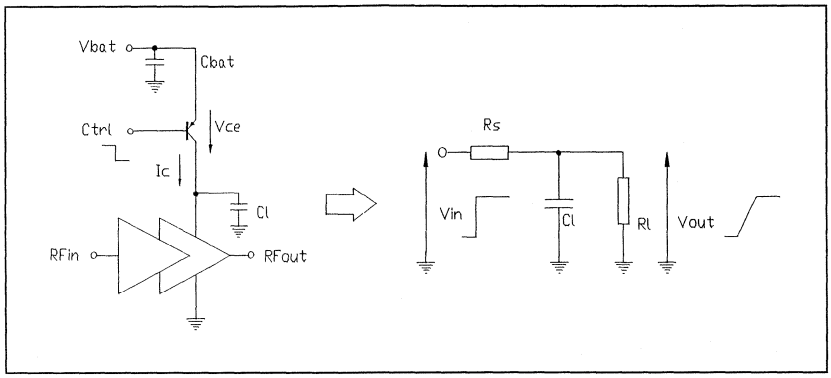

Fig. 5 Drain switching equivalent circuit

-Rl is the non linear load resistance induced by two stages of the power amplifier when these ones are switched on.
The instantaneous value of Rl (versus time) depends on the ratio V/I present on the drains of this stages.
In a first approach we will only consider the final values of V and I for calculations.
-Rs is also a non linear source resistance introduced by the switch and is approximately the ratio between Vce and I.
We will also consider the final values Vcesat and I for calculations.
-Cl is the integrating capacitor introducing the different time constants between the two last stages and the first ones.
As Rl is much larger than Rs ,we can consider that td≅(tr2-tr1)≅2.2(Cl2-Cl1) where td is the time delay to establish the drain voltage ;tr1 ,tr2 are the rise times and Cl1 ,Cl2 the integrating capacitors of the two parts of the amplifier.In that way td is approximately 22 nS.
This time delay is high enough to get the last stages already self biased before their supply voltage has reached its steady state value and in turn no extra peak current or any power overshoot can take place within the ramp-up.
A simpler drain switching circuit can be used if the amplifier is operated with negative bias at pins VGG1 and VGG2.

4. MODE OF OPERATION

Two operation modes are possible depending on the nature of the power control.

4.1 Mode 1:without negative bias

In this mode the four stages of the power amplifier are self biased with the incoming RF signal (see Fig.6).

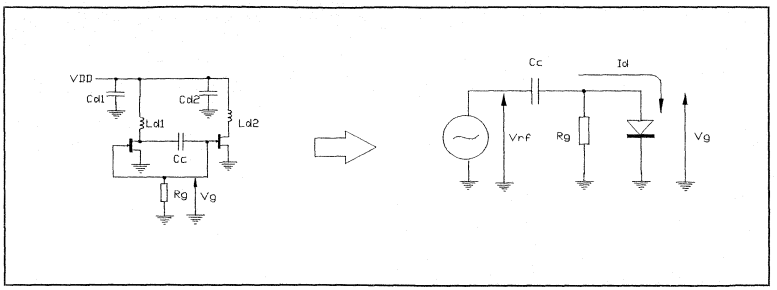

Fig. 6 Self biasing equivalent circuit

As the gates are return to ground via resistors ,when a RF signal is applied ,and if the level of this one is high enough ,a DC detected current takes place in the gate source junction.This current charges the interstage coupling capacitor Cc and in turn a DC average voltage will appear gradually across the gate source junction ,starting from zero to a negative value within the few first periods of the RF signal.When the absolute maximum value of the signal (RF+DC) is less than 0.7V (Vgson) a steady state is established because ,as the detected signal is no longer existing ,the coupling capacitor stops charging.
Once the steady state is reached ,the DC component of the signal at the gate terminal will bias negatively this one and his value will depend on the time constant Rg*Cc and the RF level.
As the power control cannot be achieved by any supply variations ,this mode of operation is only suitable for applications where power control is not required such as DECT.

4.2 Mode 2:with negative bias

This mode of operation is possible when a negative bias is available.
In that case ,adequate negative bias are applied to gates via pins VGG1 and VGG2.
Generally VGG1 biases the first three stages more in class A while VGG2 bias the last one more in class AB for a better compromise between power gain and efficiency.
This mode of operation is necessary when higher level of linearity is required.
As the internal bias no longer depends on the incoming RF level the power control is now possible by variation of the supply voltage.

5. GENERAL CHARACTERISTICS

CONDITIONS:

VDD=3.2V-F=1900MHz-Tamb=25°C-Pulse width=2.5mS-Duty cycle=25%-Pin=0dBm

CHARACTERISTICS	MIN	TYP	MAX	CONDITIONS	UNITS
Measured in mode 1 ;without negative bias-VGG1 and VGG2 connected to ground					
Supply current		400	500		mA
Rf output power	26	27	28.5		dBm
DC to RF efficiency		40			%
Output RF leakage in off state		-40		VDD=0V	dBm
Harmonic level		-35			dBc
Spurious level		-60		Load VSWR=6:1 through all phases	dBc
Load mismatch	No degradation			Pload=27dBm VSWR=6:1	
Measured in mode 2 ;with negative bias at pins VGG1 and VGG2 ;VGG1=-1.2V-VGG2=-2V					
RF output power	25.5	26	28		dBm
DC to RF efficiency		35			%
Output Rf leakage in off state		-50		VDD=0V	dBm
Total gate current	-1		1		mA

6. CIRCUIT DIAGRAM AND RECOMMENDATIONS FOR USE

6.1 Circuit diagram

The circuit diagram used for testing is described in Fig.7

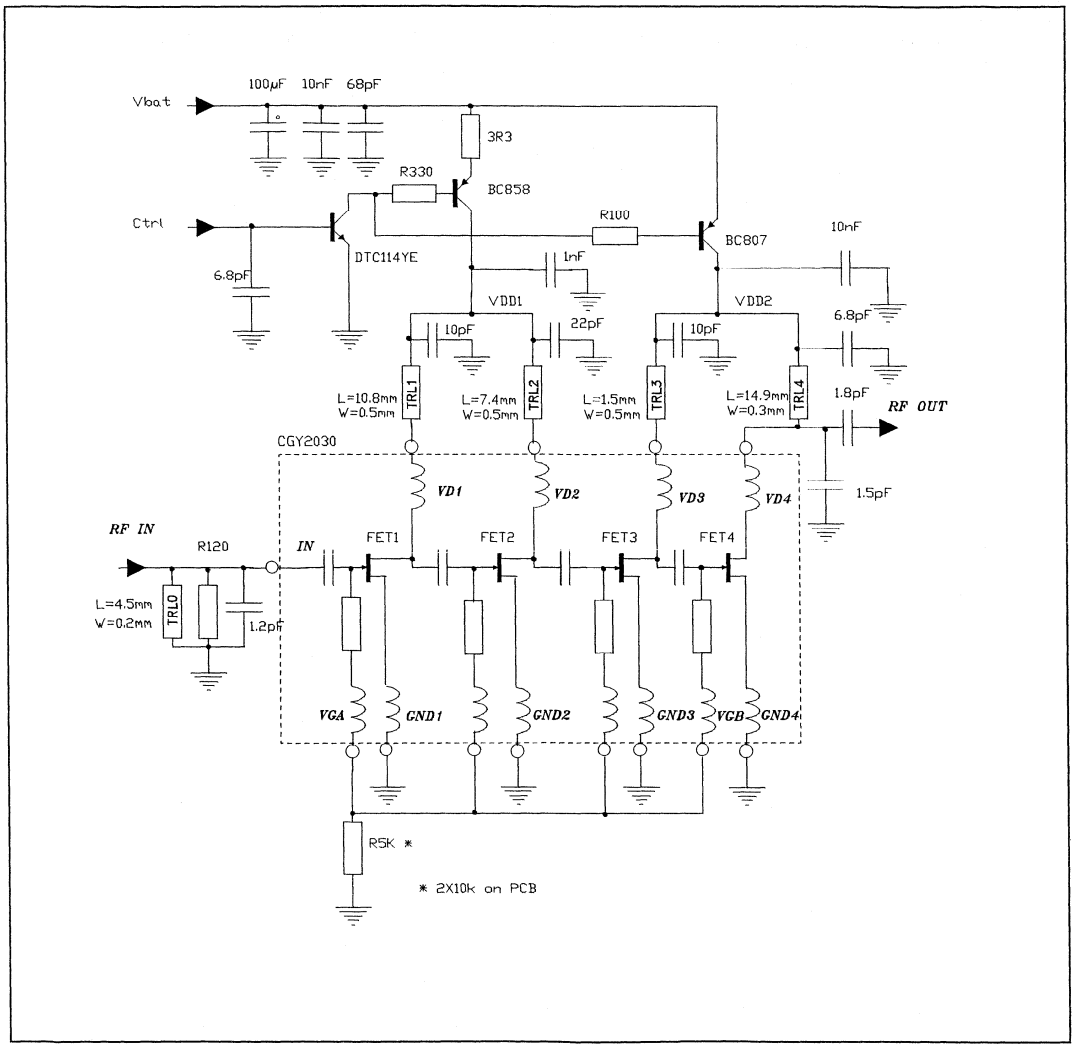

Fig. 7 Circuit diagram

6.2 Recommendations for use

Mode1 operation:
When used without negative biasing voltage applied on pin VGG1 and VGG2 ,the power amplifier is self biased with the incoming signal.
In order to prevent the device from destruction ,apply first the RF signal to pin Rfin ,then apply the switching signal to pin Ramp once Vbattery is present.

Mode2 operation:
When negative biasing is used ,apply first the negative voltages to VGG1 (typically -1.2V) and to VGG2 (typically -2V) prior the drain voltage.

7. PRINTED CIRCUIT BOARD LAYOUT-LIST OF COMPONENTS

7.1 Circuit layout.

The demoboard layout is given in Fig.8.
The characteristics of the substrate in use for the PCB are as following:
-substrate type:FR4 triple clad (the central layer is used as the reference ground plane).
-Relative permetivity:εr=4.7
-Thickness:H=2x0.8mm
-Size:40x45mm

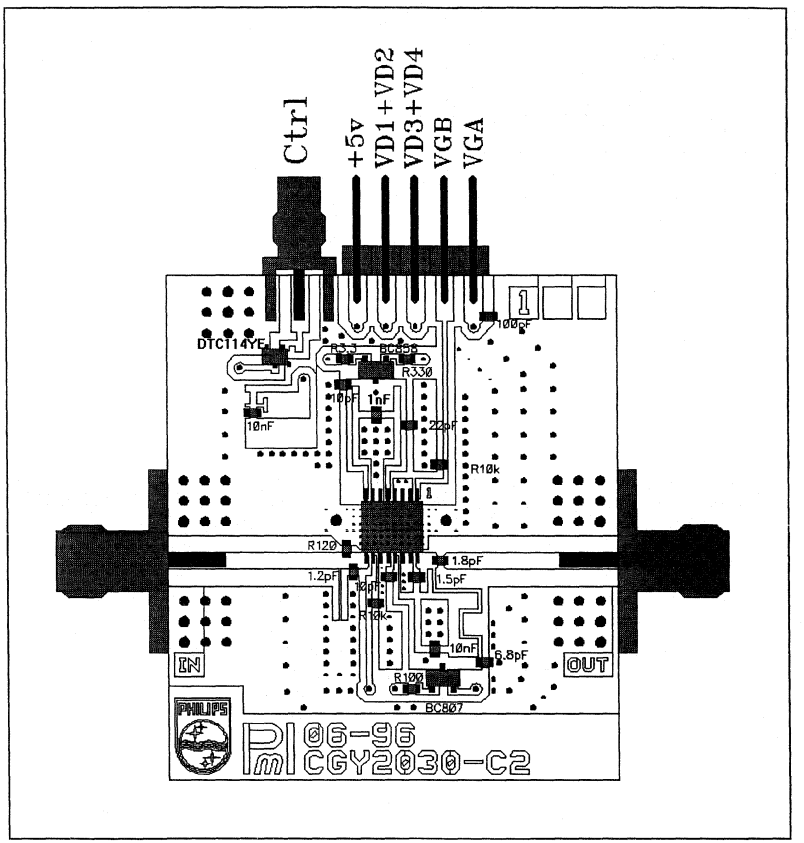

Fig. 8 Circuit layout

7.2 Part list DECT power amplifier.

CAPACITORS (Size:0603)	
VALUE	NUMBER
1.5 pF	1
1.2pF	1
1.8 pF	1
6.8 pF	3
10 pF	2
22 pF	1
68 pF	1
1nF	1
10 nF	2
100 µF	1

RESISTORS (Size:0603)	
VALUE	NUMBER
3.3 Ω	1
100Ω	1
120	1
330Ω	1
10kΩ	2

TRANSISTORS	
TYPE	NUMBER
DTC114YE	1
BC807	1
BC858	1

TRANSMISSION LINES (PCB)		
NAME	WIDTH(µm)	LENGTH(µm)
TRL0	200	4500
TRL1	500	10800
TRL2	500	7400
TRL3	500	1500
TRL4	300	14900

8. THERMAL CHARACTERISTICS/POWER DISSIPATION CONSIDERATIONS

8.1 Thermal Characteristics

The device is capable of a maximum average power dissipation of Ptot= 400 mW up to a channel temperature not exceeding Tch= 150°C
The thermal resistance from channel to ambient in free air is typically Rth j-a= 145 K/W.
In consequence ,as the formula to calculate the channel temperature is Tch= (Pl/Eff-Pl) x δ x Rth j-a + Tamb we can determine the channel temperature Tch, knowing all other parameters

8.2 Channel temperature calculation /Maximum duty cycle

If we want to calculate Tch with the following parameters:
Ptot = 400 mW
Eff = 40%
Pl = 500 mW
δ = 10%
Rtlj-amb= 145 kW
Tamb= 50°C
With formula we get:
Tch= (0.5/0.4 -0.5) X 0.1 X 145 + 50
Tch= 60.88 C°
In a same way, using the formula, we can determine what is the maximum duty cycle allowed for not exceeding the maximum channel temperature of 150°C for a given ambient temperature.

8.3 Power derating curve

For safety and reliability reason we can draw a derating curve concerning the power dissipation versus ambient temperature (See Fig 9).

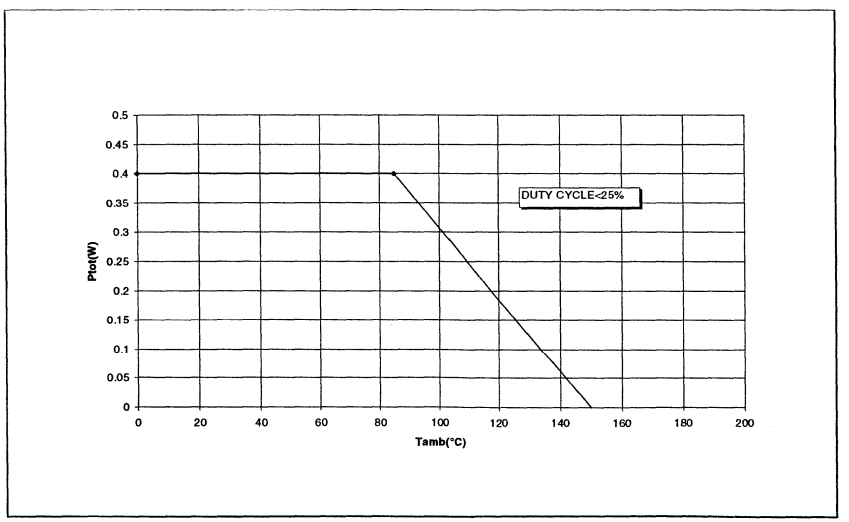

Fig. 9 Power derating

9. ELECTRICAL CHARACTERISTICS

9.1 Output power and efficiency as a function of drain voltage

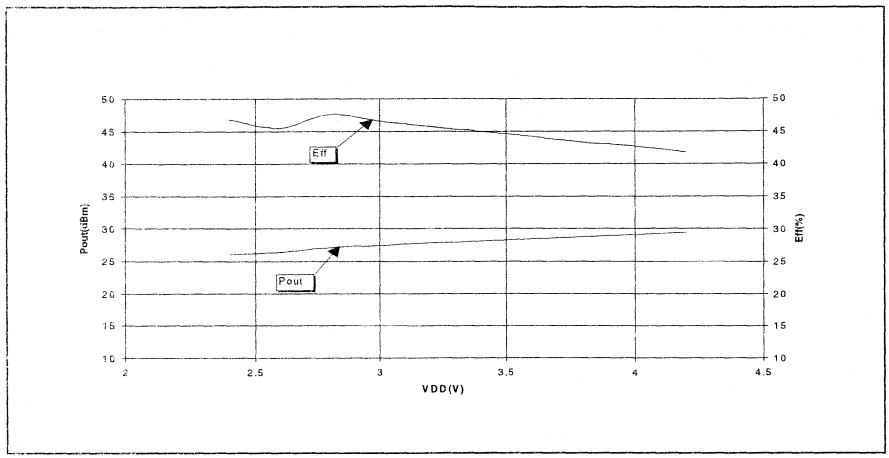

Fig. 10 Output power/efficiency versus drain voltage

9.2 Output power and efficiency as a function of frequency

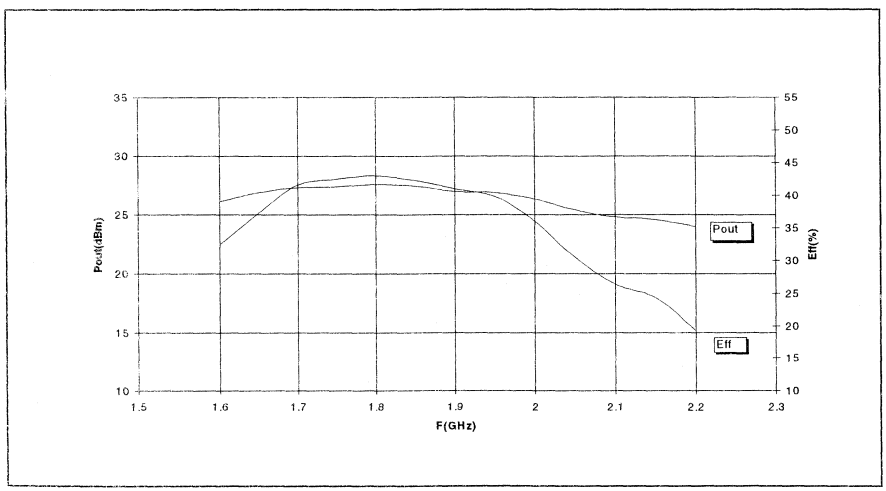

Fig. 11 Output power/efficiency versus frequency

9.3 Harmonics

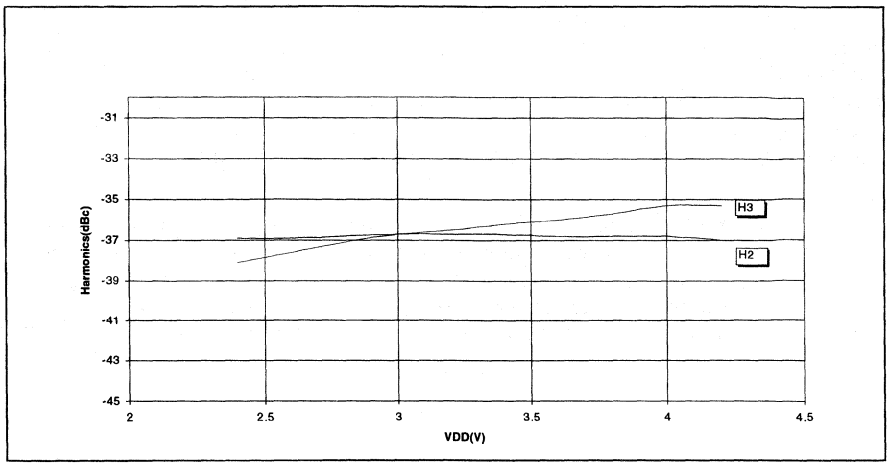

Fig. 12 Harmonics versus drain voltage

9.4 Temperature dependency

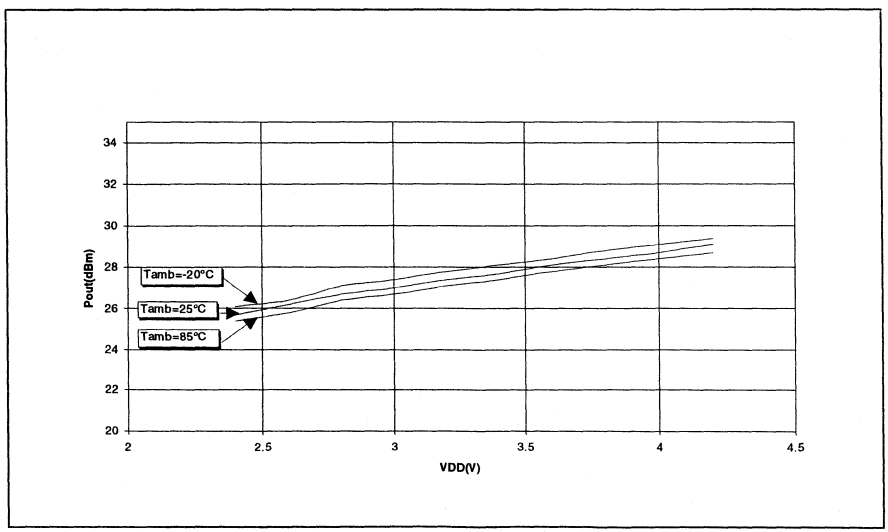

Fig. 13 Temperature dependency

Summary

This report is intended to provide application support for designing image rejecting front-ends with the UAA2072M, UAA2073M, UAA2073AM, UAA2077AM, UAA2077BM and UAA2077CM integrated circuits from Philips Semiconductors.The first of the line, the UAA2072M, has been developed for GSM applications. The UAA2073M and UAA2073AM are derivatives from the UAA2072M and hence closely related. The UAA2077AM, UAA2077BM and UAA2077CM are based on the same structure but are intended for use in 2 GHz applications. They permit low power applications and eliminate the need for an external bulky ceramic filter required for image rejection.They contain a receiver front-end and a high frequency transmit mixer (not on the UAA2077AM).

Chapter 1 covers complete theoretical background of image rejection. Chapters 2 and 3 contain a general and functional description of these ICs. Chapter 4 gives useful equations, which have been utilized for impedance matching. A worked-out application example, based on the UAA2077BM is given in Chapter 5. The related schematics, layout and assembly drawings can be found in Chapter 7. Matching results, image rejection, IP3 and all relevant RF characteristics of the circuits are included in Chapter 6, to aid in proper circuit design.

Since it was not possible to give, for each topic, the features of the all 6 ICs, it was decided to take into account only one circuit at a time as an example.

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1. BASIC THEORY OF IMAGE REJECTION

In a conventional heterodyne receiver, the incoming signal is amplified with a single stage of tuned RF amplifier and mixed with an adjustable local oscillator (LO) to produce a signal at a fixed intermediate frequency (IF). A selective RF filter is then needed to attenuate all frequencies outside the band of interest.

Let's consider the case of the following reception : the LO frequency is lower than the RF wanted frequency.

A simple application for the 935 to 960 MHz GSM band is shown below. Assuming that the IF frequency is chosen equal to 70 MHz, this leads to the values of 865 to 890 MHz for the LO frequency. The image frequency band, placed at 140 MHz away from the desired band is at 795 to 820 MHz. The signal at LO-IF frequency, presented at the RF input has to be rejected while the signal at LO+IF must go through the reception chain. On the same way, the lower side band can be also rejected.

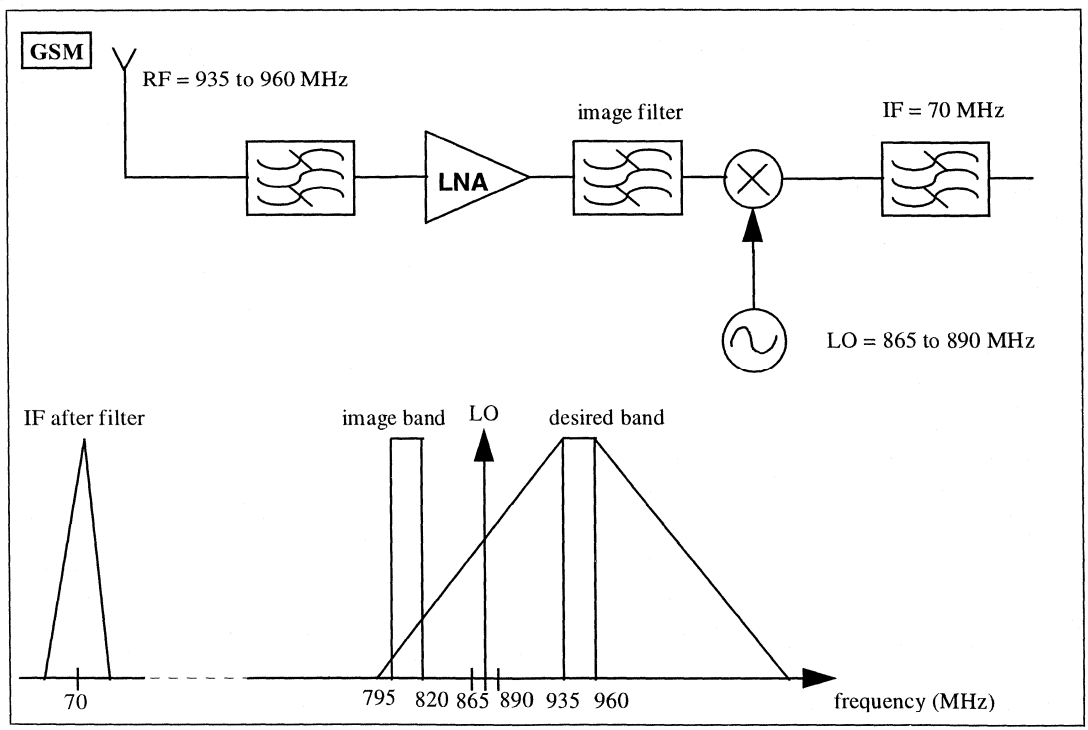


Fig. 1 Heterodyne radio receiver and frequency plan

Another way to suppress response at the image frequency is to use an image reject mixer. The basic principle is to use phase cancellation instead of frequency selective attenuation. The basic circuit consists of a pair of mixers, driven from a quadrature LO source, a 90° phase shifter and a power combiner, as shown below :

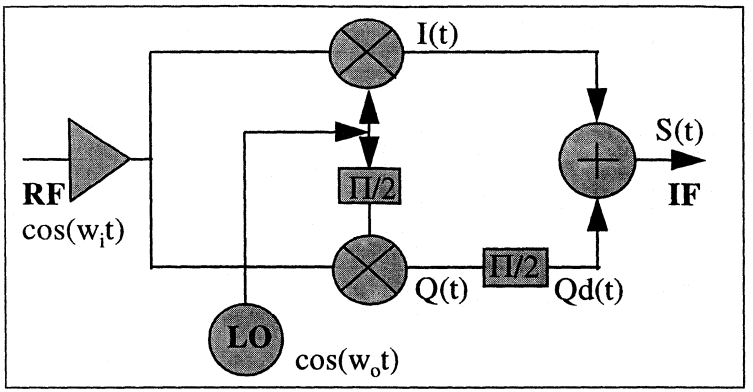


Fig. 2 Image reject mixers

To understand how the process of image rejection with this circuit is done, let's follow the mathematics equations behind that :

The signal **I(t)**, corresponding to the in-phase mixer product is equal to :

$I(t) = \cos(\omega_i t) * \cos(\omega_o t) = 1/2\ (\cos(\omega_i - \omega_o)t + \text{sum frequency}) = 1/2 \cos(\omega_d t)$

with $\omega_d = \omega_i - \omega_o > 0$, considering the case of the RF wanted signal above the LO signal.

The signal **Q(t)**, related to the quadrature mixer product is :

$Q(t) = \cos(\omega_i t) * \cos(\omega_o t - 90°) = 1/2 \cos(\omega_d t + 90°) = -1/2 \sin(\omega_d t)$

The quadrature shifter, introduced in one path, produces a signal $\mathbf{Q_d(t)}$ such as :

$Q_d(t) = -1/2 \sin(\omega_d t - 90°) = 1/2 \cos(\omega_d t)$

The signal **S(t)** , after summing the in-phase and quadrature signals is :

$S(t) = Q_d(t) + I(t) = \cos \omega_d t$, provided that ω_i is the RF frequency and $\omega_d = \omega_i - \omega_o > 0$

Now, assume that $\omega_d = \omega_i - \omega_o < 0$ ω_i is the image frequency

$I(t) = 1/2 \cos(-\omega_d t) = 1/2 \cos(\omega_d t)$

$Q(t) = 1/2 \cos(-\omega_d t + 90°) = 1/2 \sin(\omega_d t)$

$Q_d(t) = 1/2 \sin(\omega_d t - 90°) = -1/2 \cos(\omega_d t)$

Sum I(t) and $Q_d(t)$: $S(t) = 1/2 \cos(\omega_d t) - 1/2 \cos(\omega_d t) = 0$

2. INTRODUCTION TO THE IMAGE REJECTING FRONT ENDS

This chapter provides an overview of this IC family and follows with detailed description, specific to each circuit.

The UAA2072M was the first IC in the image rejection family. To satisfy the need of the emerging digital mobile communications equipment, a family of image rejecting front-end IC's based around the UAA2072M has been developed : the UAA2073M and UAA2073AM dedicated for GSM and the UAA2077AM, UAA2077BM and UAA2077CM dedicated for 2 GHz applications. A simplified block-diagram, representing the main common functionalities of these circuits is shown in Fig. 3. The IC is divided into three main blocks : the receive, transmit and local oscillator sections. The transmit block is not integrated in the UAA2077AM.

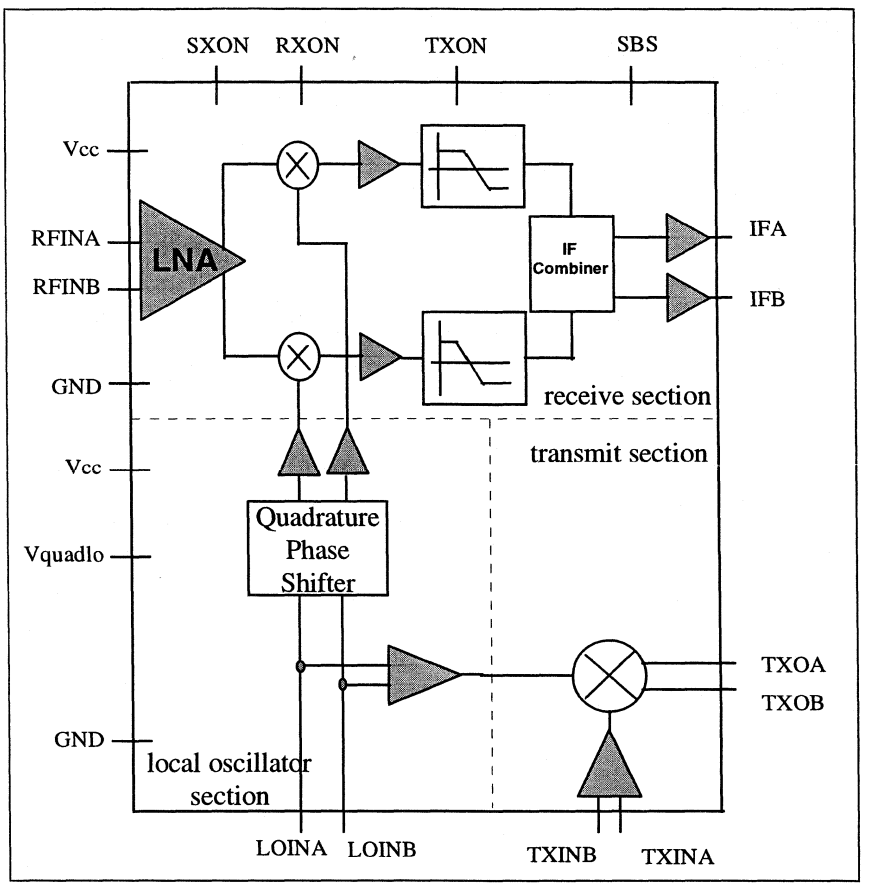


Fig. 3 Block-diagram

The circuits present the following common features :

2.1 Common Features

- low-noise, wide dynamic range amplifier
- double balanced image reject mixing
- integrated Rx and Tx blocks
- IF I/Q combiner
- on-chip quadrature network
- low-power consumption
- very low-noise figure
- small package SSOP20
- very small application (no image filter)

All relevant parameters are summed up in the following table :

Table 1 Quick reference data
Typical values are indicated

	UAA2072M	UAA2073M	UAA2073AM	UAA2077AM	UAA2077BM	UAA2077CM
Vcc (V)	4.5 to 5.3	3.6 to 5.5	3.6 to 5.3	3.15 to 5.3	3.6 to 5.3	3.6 to 5.3
Iccrx (mA)	31.5	26	26	27	27	36
RX Noise Figure (dB)	4	3.25	3.6	4.3	4.3	4.0
Gain (dB)	26	23	22	20	20	23
IP3 (dBm)	-15	-15	-15	-17	-17	-17
CP1 (dBm)	-24.5	-23	-23	-23	-23	-24
Image Rejection (dB)	35	37	45	32	32	38
IF frequency (MHz)	program.	71 (nominal)	175 (nominal)	110 (nominal)	188 (nominal)	188 (nominal)
Application	GSM	GSM	GSM	DECT	DCS1800	DCS1800/ PCS1900

All these circuits comprise an LNA and an image reject mixer. In the previous equipment designs generation, this RF part was composed of discrete LNA, mixer and image filter. This higher integration level reduces variation of RF performance in production. Therefore, high frequency radio manufacturability is eased so that reliability and reproducibility are thus improved.

The image reject mixer gives typically over 30 dB of image rejection (see Table 1). This means little RF input filtering is necessary, enabling the use of only one low-cost RF input filter. Moreover, the removal of the bulky expensive ceramic image filter enables smaller phone designs.

The performance is such that all critical RF parameters are stable over the entire temperature and voltage ranges.

Particularities of each circuit are described below.

2.2 the UAA2072M

Its supply voltage ranges from 4.5 to 5.3 V ; it is intended to be used in the GSM cellular telephones. To adjust for maximum image rejection performance at a given IF, a control logic programmable via the 3-wire serial bus interface is provided. This permits indeed compensation for process spreads and trimming for the chosen IF frequency and the LO band center frequency. The power-up of the transmit, receive and LO buffers as well as the selection of sideband rejection are also programmable by the 3-wire serial bus.

2.3 the UAA2073M and UAA2073AM

The UAA2073M is the second generation front-end for 900 MHz applications. It offers better performance than the UAA2072M.

The supply voltage range is lower, from 3.6 to 5.3 V with a typical 3.75 V supply. The power consumption has been improved to 26 mA typically in receive mode. The whole control block for tuning image rejection has been suppressed. The image rejection is optimum when the IF frequency is equal to 71 MHz.

The UAA2073AM is a derivative of the UAA2073M, with an IF frequency equal to 175 MHz. The image frequency rejection has been improved to 45 dB but at the expense of a reduced range of possible IF frequencies.

2.4 the UAA2077AM, UAA2077BM and UAA2077CM

In order to meet the rapidly increasing demand for mobile radio 1800 MHz equipment, the UAA2077AM, the UAA2077BM and UAA2077CM have been developed and have become the new generation of image rejection ICs.

The UAA2077AM is intended for use in the digital cordless system DECT, the UAA2077BM and UAA2077CM in the digital cellular systems DCS1800 and PCS1900. One particularity of the UAA2077AM is that it doesn't include a transmit block. One the other hand, the voltage supply can be reduced up to 3.15 V for temperature from 0 to 70 °C. This offers the possibility to connect directly the chip to an unregulated 3-cell battery supply. The UAA2077BM has been designed for DCS1800 applications. The UAA2077CM, a derivative of that IC, was designed initially to address the stringent requirements of PCS1900 applications but is also suitable for DCS1800 applications.

3. FUNCTIONAL DESCRIPTION

3.1 Power-down modes

The UAA2072M is the only one of this ICs' family to feature software power-down modes. For the five other circuits, several power-down modes are exclusively controlled by hardware input pins. Let's take the example of the UAA2073M. According to the block-diagram, 3 different functional areas are defined:

- the receive section
- the transmit section
- the local-oscillator section

For minimizing the pulling effect on the external VCO when entering in the receive or transmit modes, a special mode of operation has been created : the synthesizer-ON (synthon) mode . This mode is used to power-up the buffering on the LO inputs. The whole local oscillator section is thus turned **on**; this includes the quadrature phase shifter and buffers.

When the transmit mode is active, the down conversion mixer and the low-noise amplifier, including in the transmit section are turned **on**. The LO buffer (from the LO section) is also needed to drive the transmit IF down conversion mixer and has to be powered-on.

For the receive mode, the whole receive section is turned **on**, just as the quadrature phase shifter and the LO buffer on the path.

For example, a typical cellular transceiver would first assert SXON, to power-up LO buffers and allow VCO to stabilize, followed some time later by RXON being asserted just before the wanted signal arrives. At the end of the receive burst, RXON only is de-activated to power-down the receiver. The circuit is left in SX mode, as following slots will be used for example for transmitting. The circuit will enter TX mode when TXON is asserted. When the complete transceiver re-enters IDLE mode (no active call), the IC is returned to power down mode by de-activating SXON, RXON and TXON.

The different modes of operation are then defined as follows:

- the RX mode : the receive section and LO buffers to RX are **on**
- the TX mode : the transmit section and LO buffers to TX are **on**
- the Synthon mode : the complete LO section is **on**
- the SRX mode : the receive section is **on** and the Synthon mode active
- the STX mode : the transmit section is **on** and the Synthon mode active

The control of these different power status is done by hardware, with the pins TXON, RXON and SYNTHON.

Different logical combinations allow a selection of all the modes defined above (see Table 2).

Table 2 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SYNTHON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	RX mode
HIGH	LOW	LOW	TX mode
LOW	LOW	HIGH	Synthon mode
LOW	HIGH	HIGH	SRX mode
HIGH	LOW	HIGH	STX mode
HIGH	HIGH	LOW	receive and transmit sections on; specification not guaranteed
HIGH	HIGH	HIGH	receive and transmit sections on; specification not guaranteed

Figure 4 shows these modes of operation.

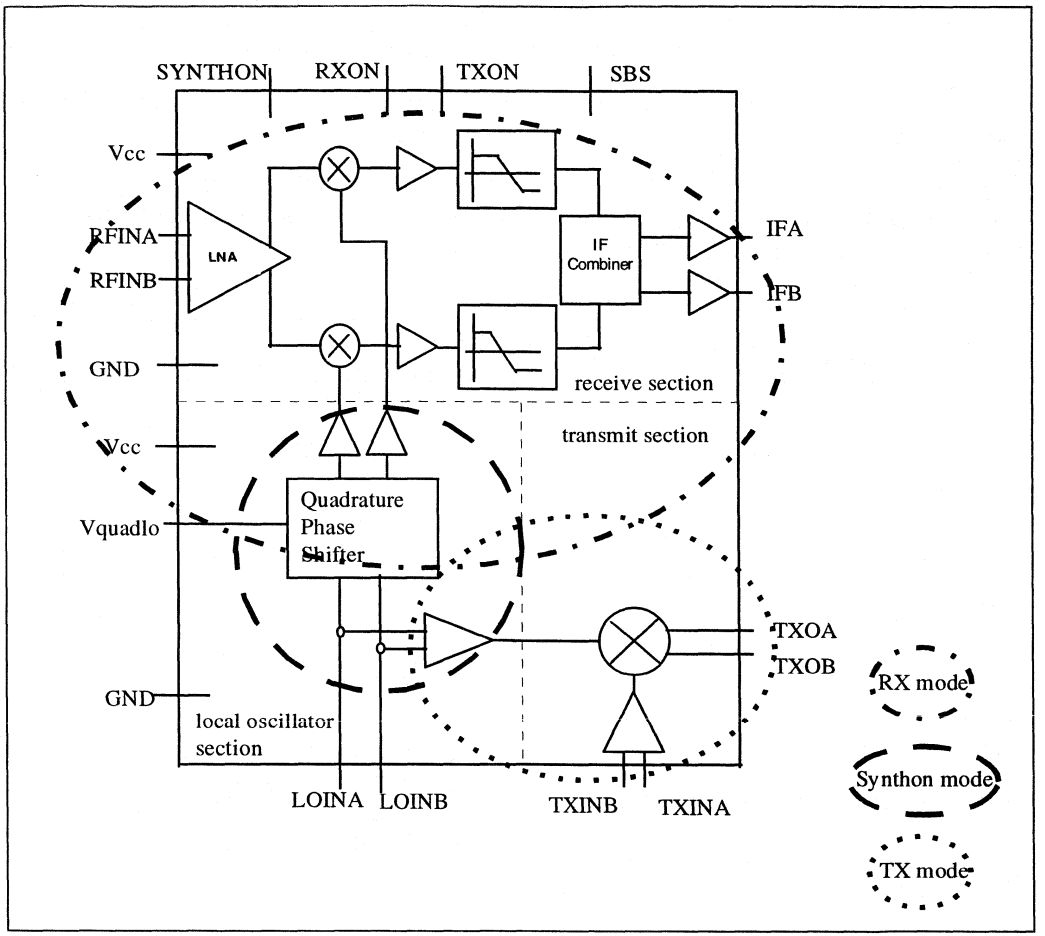


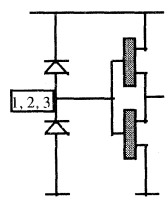
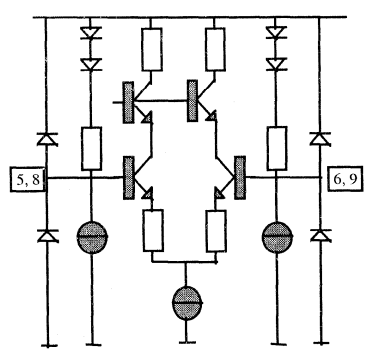
Fig. 4 Power-down modes

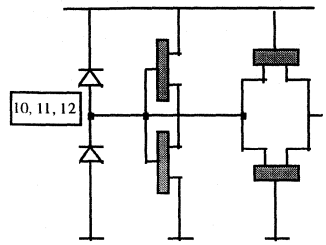
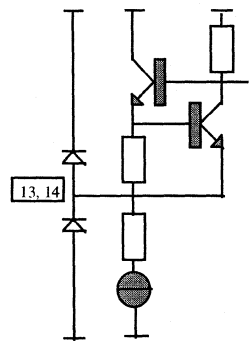
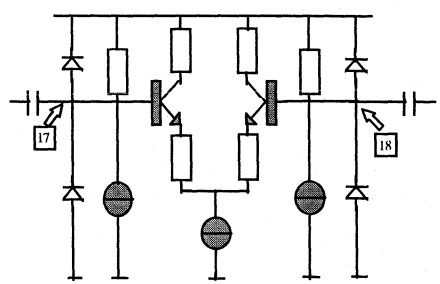
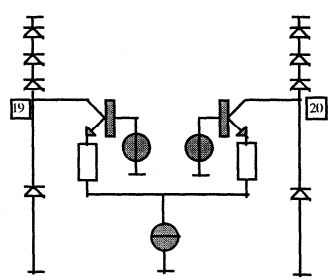
Power-down modes for the UAA2077AM/BM/CM operate in the same way. The SYNTHON pin is named in that case the SXON pin and refers to the SX mode (instead of Synthon).

3.2 Pin function diagram

The following table shows the equivalent circuit per pin for the UAA2072M. An analogy can be made for the pins functions diagrams of the UAA2073M/AM and UAA2077AM/BM/CM.

- the equivalent circuits related to the LO, RF, TX inputs and IF outputs are common for all ICs.
- the TX output on the UAA2077BM/CM is identical to the IF output on the UAA2072M.
- the TX output of the UAA2073M/AM is identical to the TX output of the UAA2072M.
- the TXON, RXON and SXON pin diagrams on UAA2073M/AM and UAA2077AM/BM/CM are similar to the CLK, DATA and $\overline{E}$ ones on the UAA2072M.

PIN N°	PIN MNEMOMIC	DCV	EQUIVALENT CIRCUIT
1	CLK		
2	DATA		
3	$\overline{E}$		
5	RFINA	+ 2.1	
6	RFINB	+ 2.1	
8	TXINA	+ 2.2	
9	TXINB	+ 2.2	

PIN N°	PIN MNEMOMIC	DCV	EQUIVALENT CIRCUIT
10	TEST		
11	RXON		
12	TXON		
13	TXOIFB	+ 2.9	
14	TXOIFA	+ 2.9	
17	LOINB	+ 4.8	
18	LOINA	+ 4.8	
19	IFB	+ 2.5	
20	IFA	+ 2.5	

3.3 Phase shifter

The principle of phase shifting, implemented in the image rejecting front-ends is based on all-pass filters.

The basic cell is then as follows :

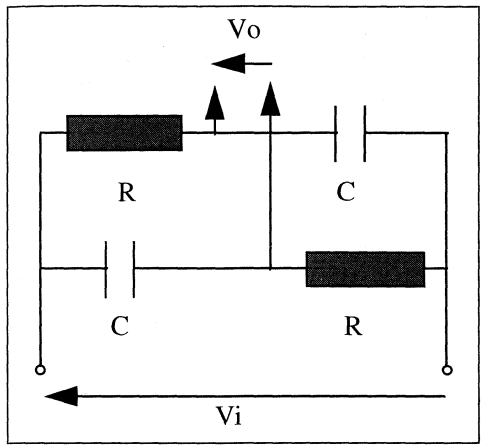


Fig. 5 All-pass filter

From the equations associated with the circuit, it can be easily deduced that :

$$|Vo| = |Vi|$$

$$\Delta\phi = -2\arctan(RC\omega)$$

For the LO quadrature phase shifter, two cells of such type are used, one set to 45 ° and the other to 135 ° and work in their linearity zone. Graphs of simulated LO phase shift are given so that exact quadrature phase can be obtained for a given LO frequency (see Fig. 6 and Fig. 7).

The design procedure for phase-shifting on the I and Q channels is similar.

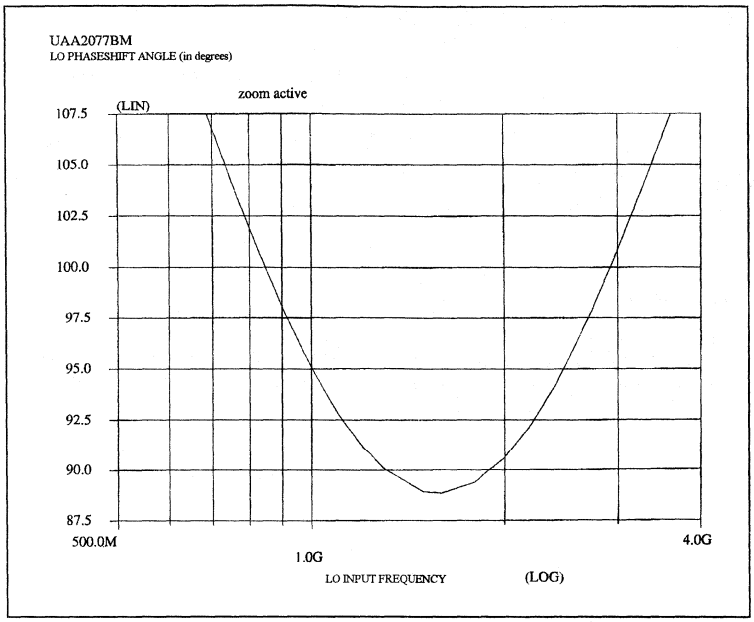


Fig. 6 Simulated LO phase shift versus LO input frequency

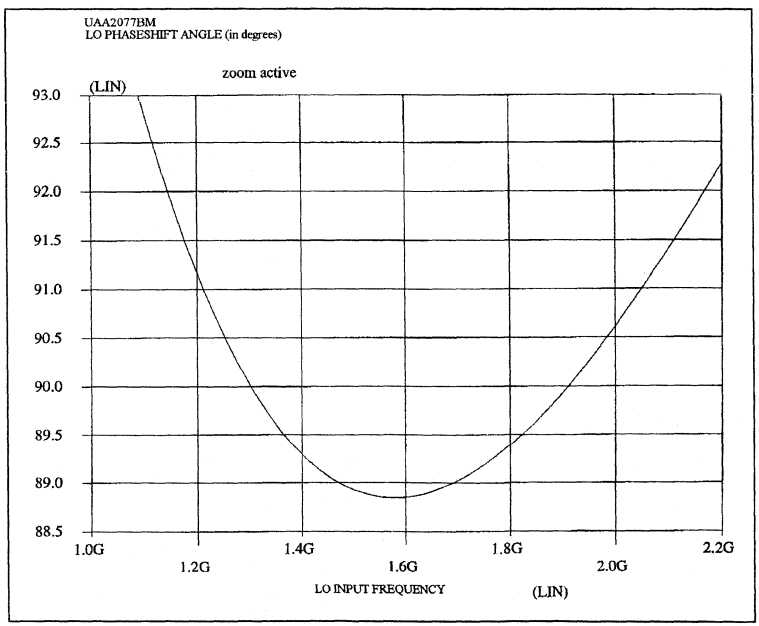


Fig. 7 Simulated LO phase shift versus LO input frequency (magnified around 1.6 GHz)

4. IMPEDANCE MATCHING CONSIDERATIONS

4.1 Introduction

Transfer of power between a source and its load must be done with a minimum of loss, particulary if the originated signal is already very low. Therefore, special care must be taken for impedance matching when designing a RF circuit. The aim is indeed to enable a maximum of power transfer.

4.2 Impedance Matching

Let's assume first that the source and load impedances are purely resistive equal to R_S and R_L. A matching can be easily done with a L-network design, shown below . It is the simplest and most widely used circuit as a matching circuit :

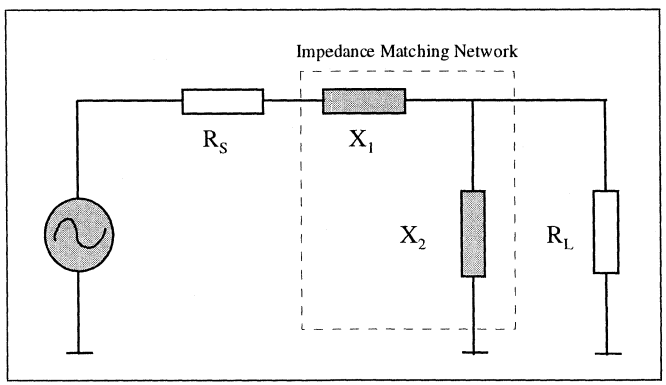


Fig. 8 L-network circuit

R_S : source resistance

R_L : load resistance

X_1 : series reactance

X_2 : parallel reactance

Let's now introduce the equations, which can be used to design this network.

Dealing with the quality factor Q, the following equations provide a simple and quick solution.

Determine the Q factors from

$$Q_1 = Q_2 = \sqrt{\frac{R_L}{R_S} - 1}$$

Determine X_1 and X_2 from

$Q_1 = X_1 / R_S \qquad Q_2 = R_L / X_2$

Since there are 2 possible arrangements of the L and C components, X_1 and X_2 can be either capacitive or inductive reactance; it depends on the configuration required, low-pass or high-pass.

In most cases, the impedance is rarely purely resistive. Source and load impedances are almost always complex, i.e. they contain both resistive and reactive components. Therefore, it is also necessary to handle these stray reactances.

Two basic approaches can be used : the stray reactances present in the source and load can be absorbed in the matching network when the stray element values are smaller than the calculated element values. If not, they can be resonated with an equal and opposite reactance. This is the basic of any matching design, to make the source drive its complex conjugate as a load impedance The reactive parts thus cancel each other and leave only R_S and R_L . If R_S and R_L are equal, maximum power transfer is achieved.

4.3 Balun Design

A balun is a device for matching an unbalanced line (e.g. a coax) to a balanced load (e.g. an antenna).

The standard configuration of all baluns utilized in our application is depicted in Fig. 9.

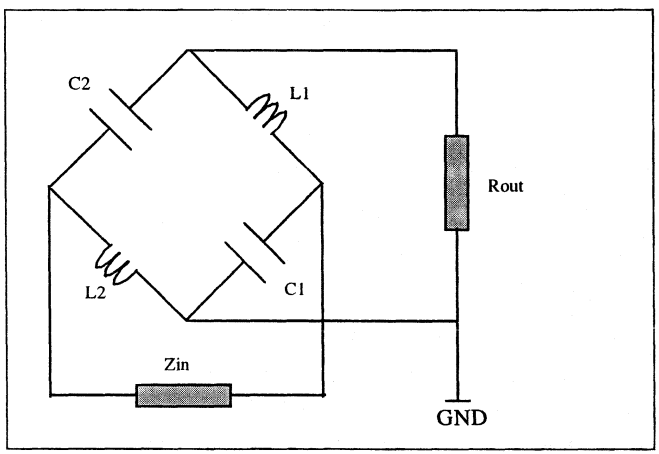


Fig. 9 Balun circuit

Since Rout represents the output impedance of the generator, it is always resistive (e.g. 50 Ω). Zin represents the differential input impedance of the circuit. In order to simplify the balun design, let's assume that Zin is also resistive, equal to Rin.

Therefore, L1 = L2

C1 = C2

The mathematics associated with the circuit give the following results; the balun parameters, depending on the input / output resistances and frequency are :

$$L = \frac{\sqrt{Rin * Rout}}{\omega} \qquad \text{and } C = \frac{1}{\omega * \sqrt{Rin * Rout}}$$

To get more information on printed balun design, please refer to the "OM5045 Dect radio design" application note (see references).

5. TYPICAL APPLICATION CIRCUITS

5.1 Worked Examples

In this chapter, a design example, based around the UAA2077BM for DCS1800 applications is given. The circuit is typically connected as shown in Fig. 26. All values related to input / output impedances are mentioned in the product datasheet (dated from 9 Jan 96). The input impedance parameters are always specified in parallel configuration.

Multilayer ceramic capacitors with NPO dielectric have been used for general coupling/decoupling aspects :

- a value of 8.2 pF for decoupling 2 GHz frequencies (C1, C3, C17, C18, C19, C29 for AC-coupling; C6 to C9, C27, C30 for supply voltage decoupling).

- a value of 100 pF for decoupling 100-200 MHz frequencies (C11, C23 for AC-coupling; C5, C31 for supply voltage decoupling)

This choice results in a compromise between a high capacitive value needed for decoupling and the effect of parasitic inductance (self resonance frequency) appearing when dealing with high frequencies.

5.1.1 RF input

R_p, the real part of the parallel impedance is equal to 60 Ω

C_p, the imaginary part of the parallel impedance is equal to 1 pF

f_i , the RF input frequency is equal to 1850 MHz

The balun component values are then calculated at 1850 MHz with Rin = 60 Ω and Rout = 50 Ω

L = 4.7 nH On the demo board, L6 = L1 = 5.6 nH

C = 1.6 pF On the demo board, C2 = C14 = 1.2 pF

The difference found between calculated and real values are due to PCB parasitic effects. An optimization has also been done in order to get a noise figure as small as possible.

Now, let's resonate C_p with an equal and opposite reactance at 1850 MHz :

$LC_p\omega^2 = 1$ hence L = 7.4 nH On the demoboard, L15= 6.8 nH.

5.1.2 TX input

R_p, the real part of the parallel impedance is equal to 65 Ω

C_p, the imaginary part of the parallel impedance is equal to 1 pF

f_i , the RF input frequency is equal to 1750 MHz

This yields to the following values :

L = 5.2 nH L7 = L8 = 4.7 nH

C = 1.6 pF C15 = C16 = 1.8 pF

5.1.3 IF output

According to the pin function diagram, the IF output is of the open-collector type. It can also be deduced that the voltage output can not be greater than $V_{cc}+3V_{be}$.

It is decided to proceed in 2 stages :

- a first matching from 1.2 kΩ to 50 Ω in single-ended mode that means on each IF output

- a second matching using a balun in order to provide from both IF ouputs, IF_A and IF_B (100 Ω differential) one terminal single ended output IF_o at 50 Ω.

Matching

The need for a DC path between V_{CC} and the output pin dictates the need for an inductor in the shunt leg of the matching network.

Z_{LRX}, the typical application IF output load impedance is equal to 1kΩ in balanced configuration. C_{IF}, the typical internal capacitance, measured on the demo board is equal to 4 pF

The application is then for 1 kΩ load in differential mode i.e. 1 kΩ on each single-ended IF output.

For our application, C_L is equal to 4 pF

R_L is chosen equal to 1.2 kΩ

$R_S = 50\ \Omega$

$f_{IF} = 188$ MHz

Following the basic design procedure from paragraph 4.2 yields :

$$Q_1 = Q_2 = \sqrt{\frac{1200}{50} - 1} = 4.8$$

$X_1 = Q_1 * R_S = 50*4.8 = 240$

$X_2 = R_L / Q2 = 1200 / 4.8 = 250$

$X_1 = 1 / C\omega \quad \Rightarrow C = 1 / X_1\omega = 1 / (240*2\pi*188.10^6) = 3.5$ pF

On the schematic, C22 = C24 = 3.9 pF

$X_2 = L\omega \quad \Rightarrow L = X_2 / \omega = 250 / (2\pi*188.10^6) = 212$ nH

The matching for the reactive part of the load, $C_L = 4$ pF, leads to the following value for L' :

$L'C\omega^2 = 1 \quad \Rightarrow L' = 1 / (4.10^{-12}*(2\pi*188.10^6)^2) = 1.79.10^{-7}$

The resultant inductance is :

$L // L' = 97*10^{-9} = 97$ nH

On the schematic, L11 = L12 = 100 nH

Balun

Rin = 100 Ω

Rout = 50 Ω

$L = \sqrt{100 * 50}$ / (2π*188*10^6)= 59.8 nF L13 = L14 = 56 nH

C = 1 / ($\sqrt{100 * 50}$ *2π*188.10^6) = 11.9 pF C25 = C26 = 12 pF

6. MEASUREMENTS and RESULTS

6.1 Matching results

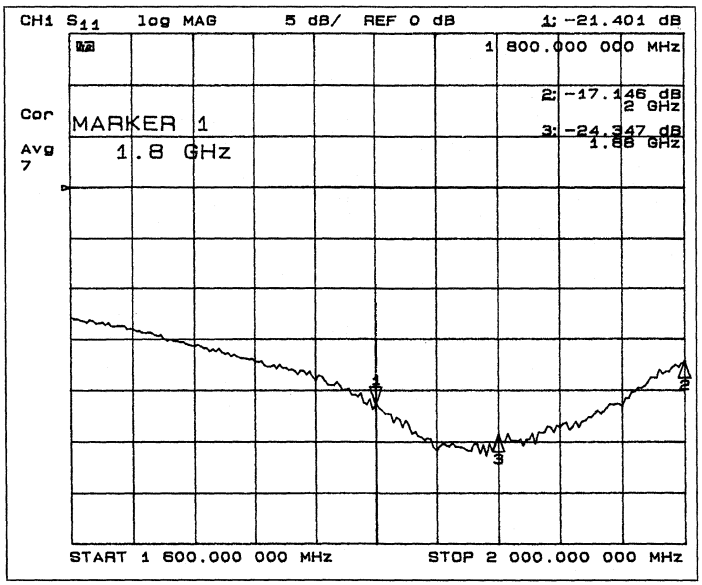


Fig. 10 Matching at RF input

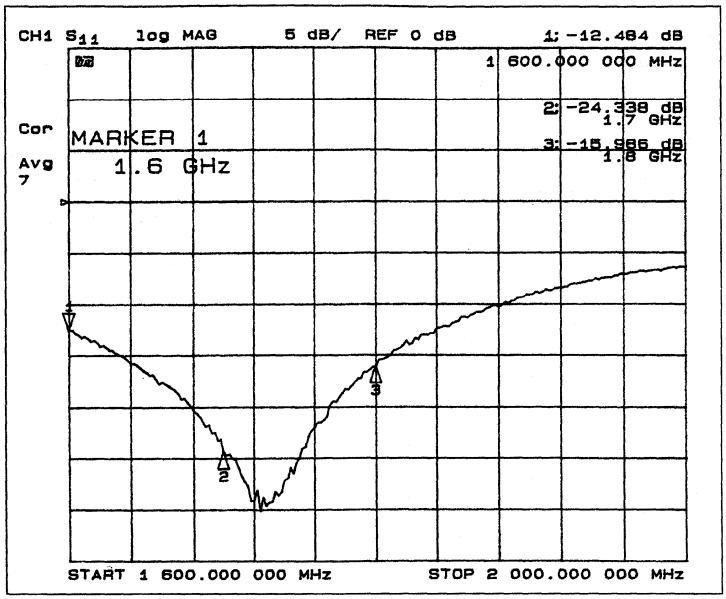


Fig. 11 Matching at TX input

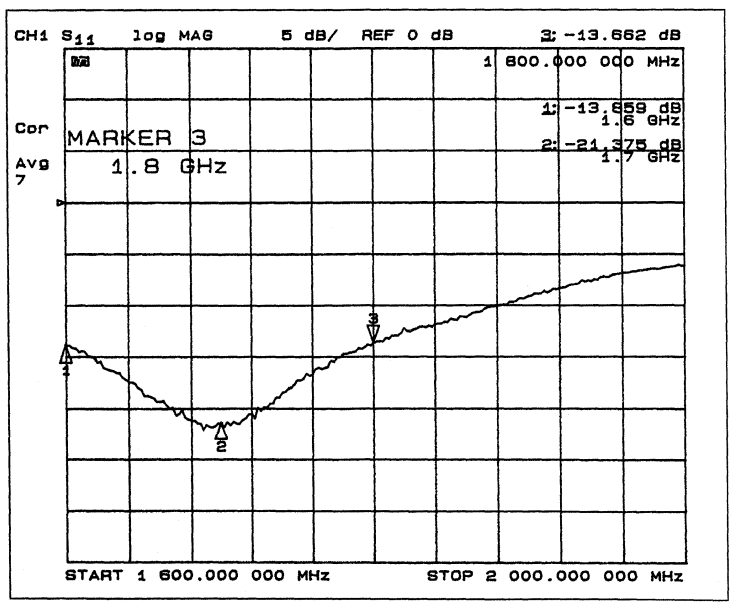


Fig. 12 Matching at LO input

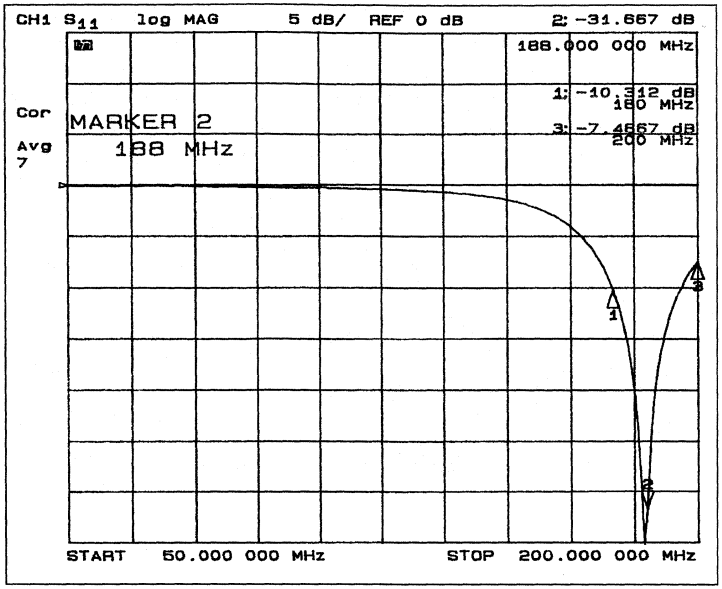


Fig. 13 Matching at IF output

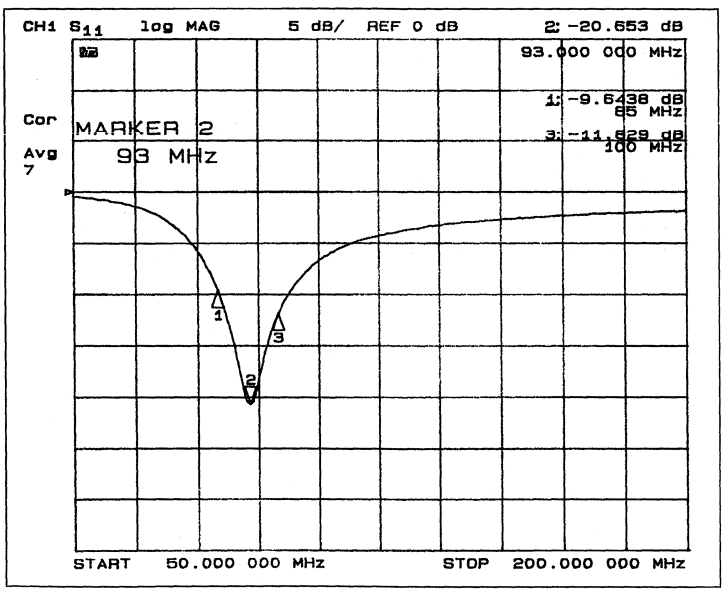


Fig. 14 Matching at TX output

6.2 Linearity / spurious response

In Fig. 15 is depicted the setup used for measuring the spurious response . Two separate measurements have been done :

- the RF frequency sweeps from RF - 4IF to RF + IF with a variable step of IF/(3*4*5) in order to reach the 2nd, 3rd, 4th and 5th harmonics.

- the RF frequency sweeps from IF to 22 IF with a fixed step equal to IF/5

In both cases, the LO frequency is fixed and the network analyzer always looks at a fixed IF frequency.

The results are shown on Fig. 16 and Fig. 17.

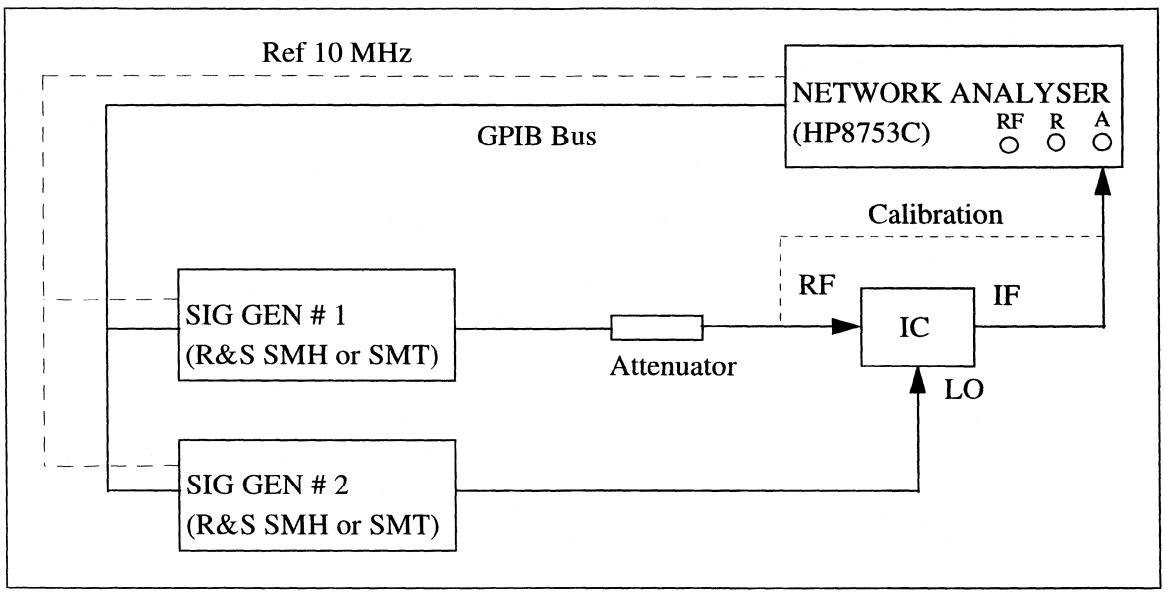


Fig. 15 Spurious response measurement setup

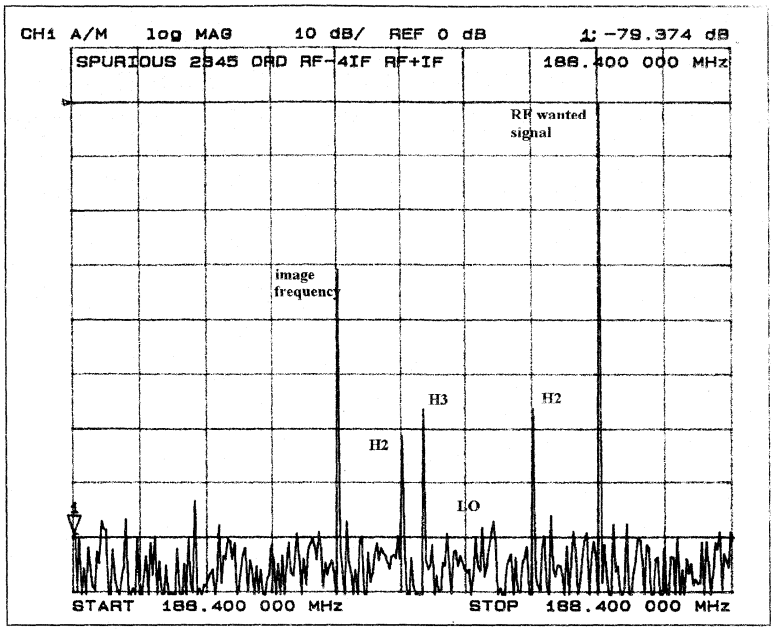


Fig. 16 UAA2077BM spurious response

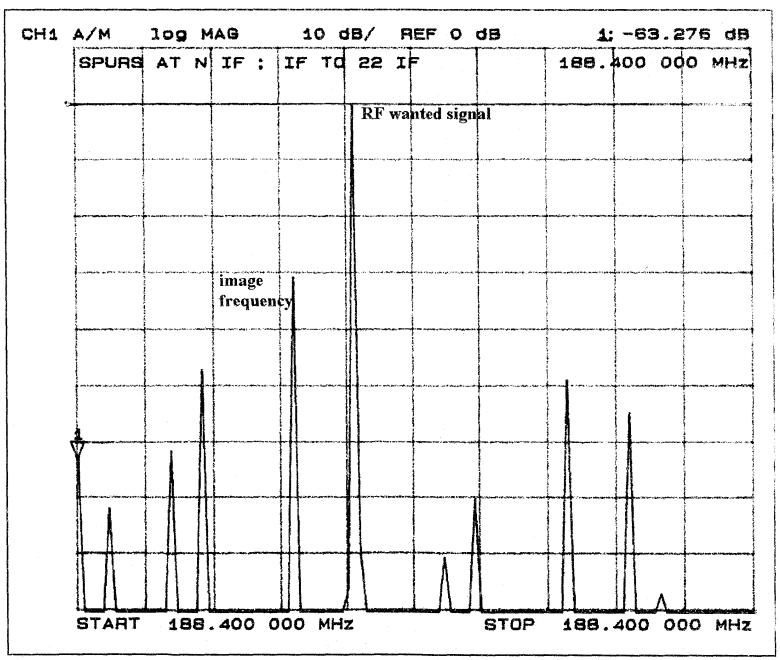


Fig. 17 UAA2077BM spurious response

6.3 Image rejection

Image rejection measurements have been proceeded in varying 2 different parameters :

- the image rejection is given versus the IF frequency with a fixed LO . The RF signal is swept. The appropriate set-up is depicted on Fig. 18. Results are shown on Fig. 19 and 20.

- the image rejection is given versus the RF frequency with a fixed IF. Both RF and LO input signals are swept. The set-up, in that case, is identical to the one used for spurious response measurement (see Fig. 15). The results are shown on Fig. 21.

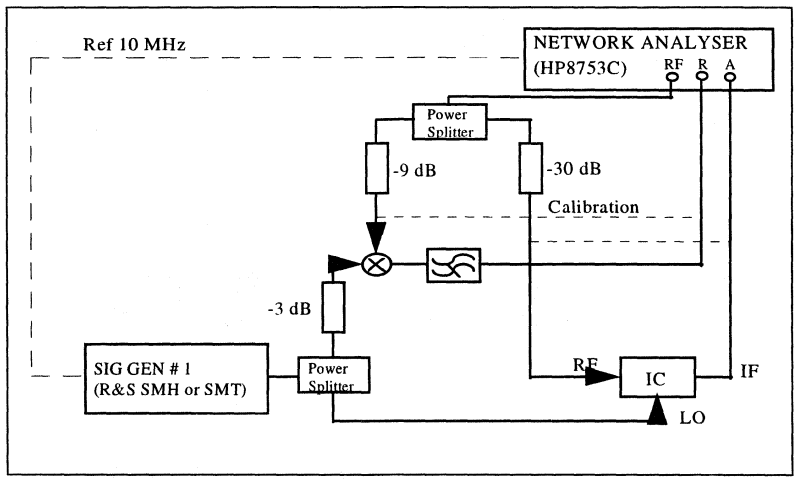


Fig. 18 Image rejection measurement setup with a fixed LO frequency

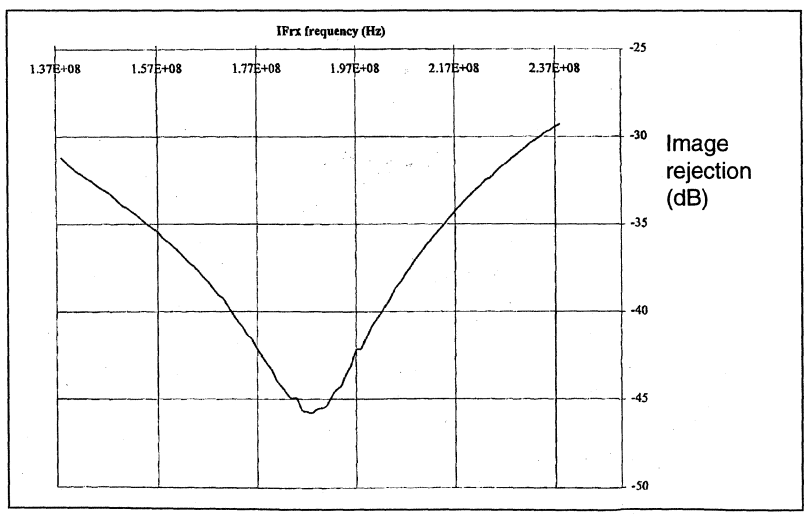


Fig. 19 UAA2077CM Image rejection versus IF frequency for f_{RF} wanted > f_{LO}

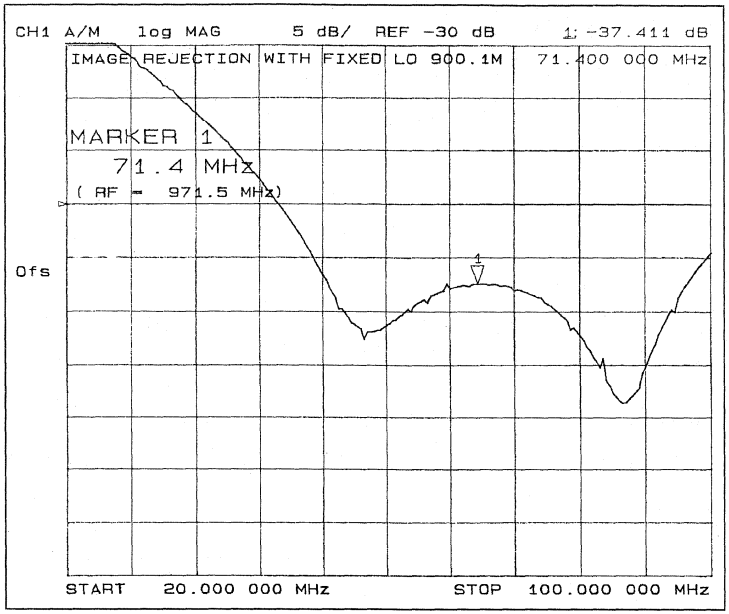


Fig. 20 UAA2073M Image rejection versus IF frequency

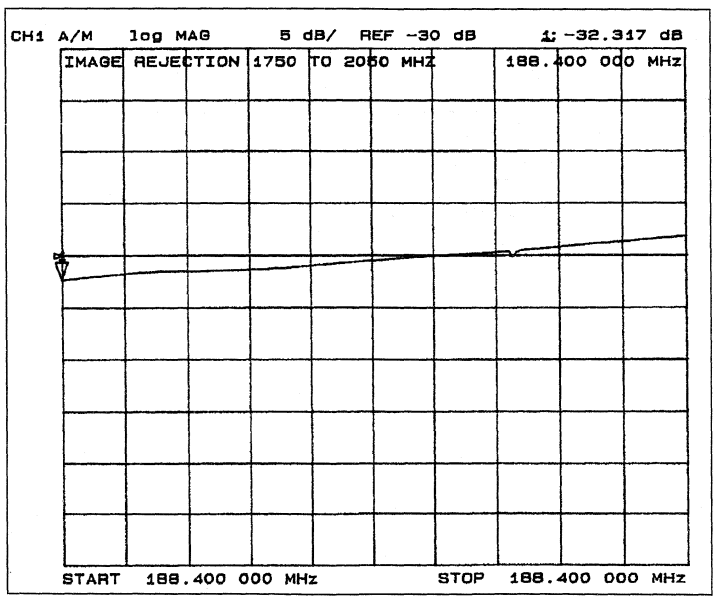


Fig. 21 UAA2077BM Image rejection versus LO frequency

6.4 Gain, compression point and IP3

The gain presented on Fig. 23 has been measured for a fixed IF frequency with a RF swept from 1.75 to 2.05 GHz. The set-up utilized in that case is the same as the one shown on Fig. 15.

The 1 dB compression point has been measured following the test set-up depicted on Fig. 20.

The set-up shown on the following figure enables a measurement of the 3rd order intercept point parameter.

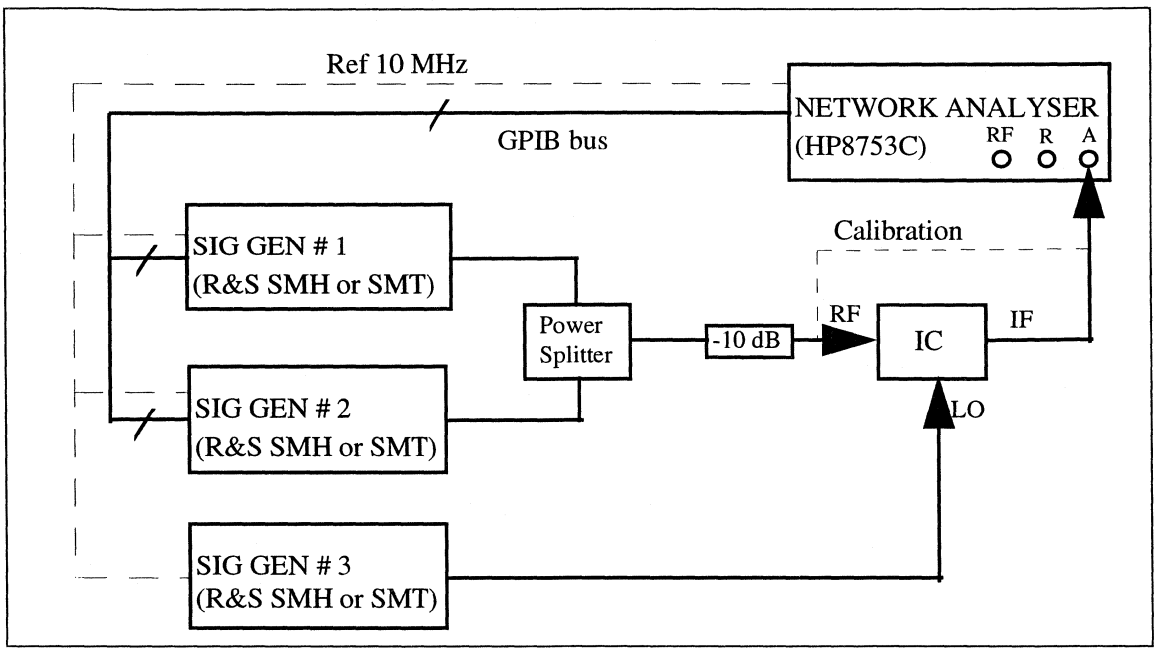


Fig. 22 Third order Intercept Point set-up

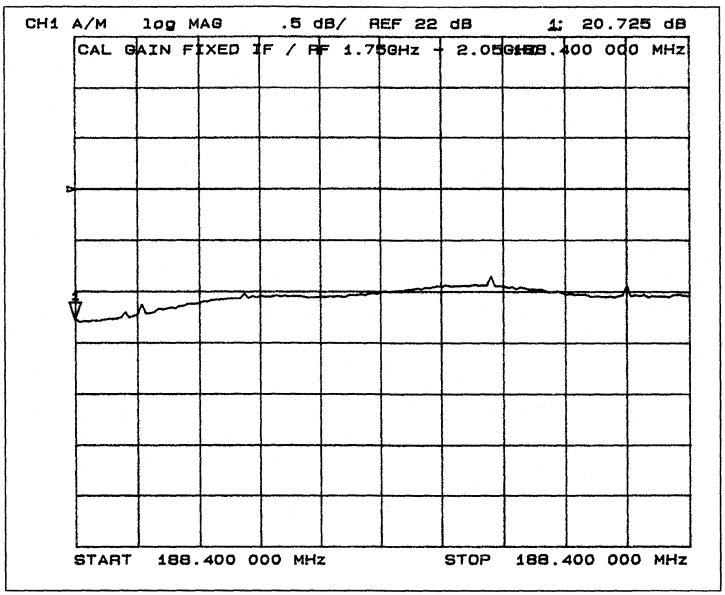
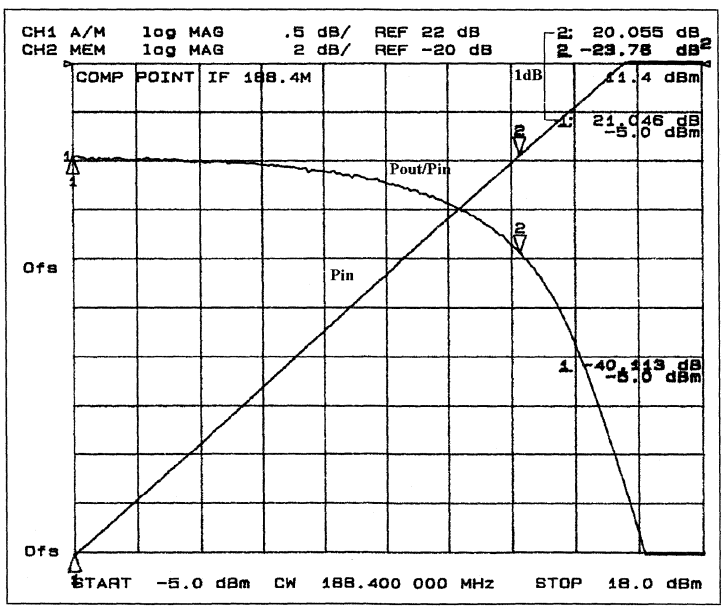


Fig. 23 UAA2077BM gain versus input frequency (from 1.75 to 2.05 GHz)



CPin = -23.75 dBm

Fig. 24 UAA2077BM 1 dB Compression Point

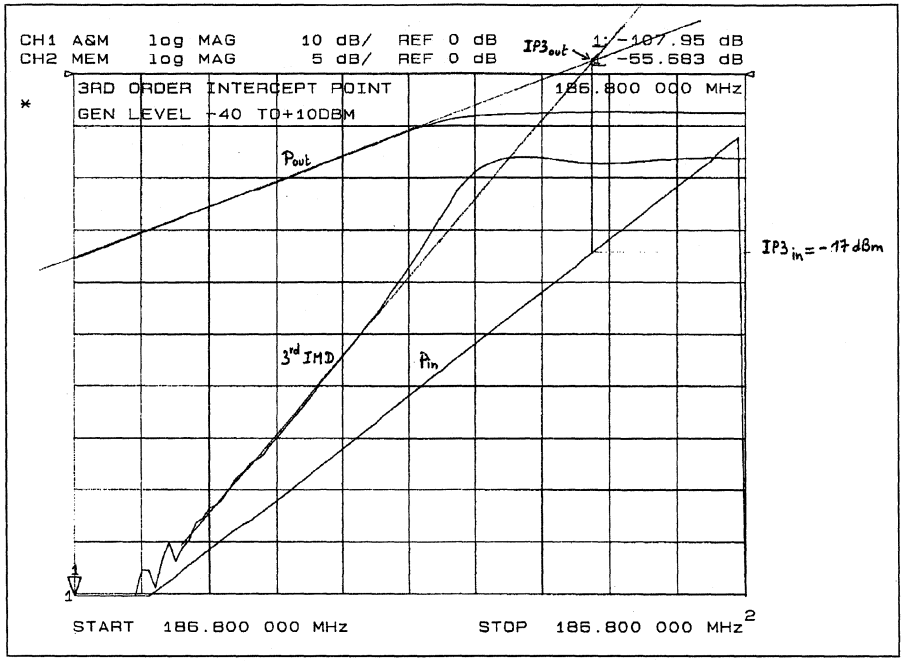


Fig. 25 UAA2077BM 3rd order Intercept Point

7. DEMONSTRATION BOARD

Two different kinds of board have been designed, one related to the UAA2073XM ICs, the other one to the UAA2077XM ICs.The UAA2077BM and the UAA2073M have been taken as an example for both families.

7.1 Schematic drawings

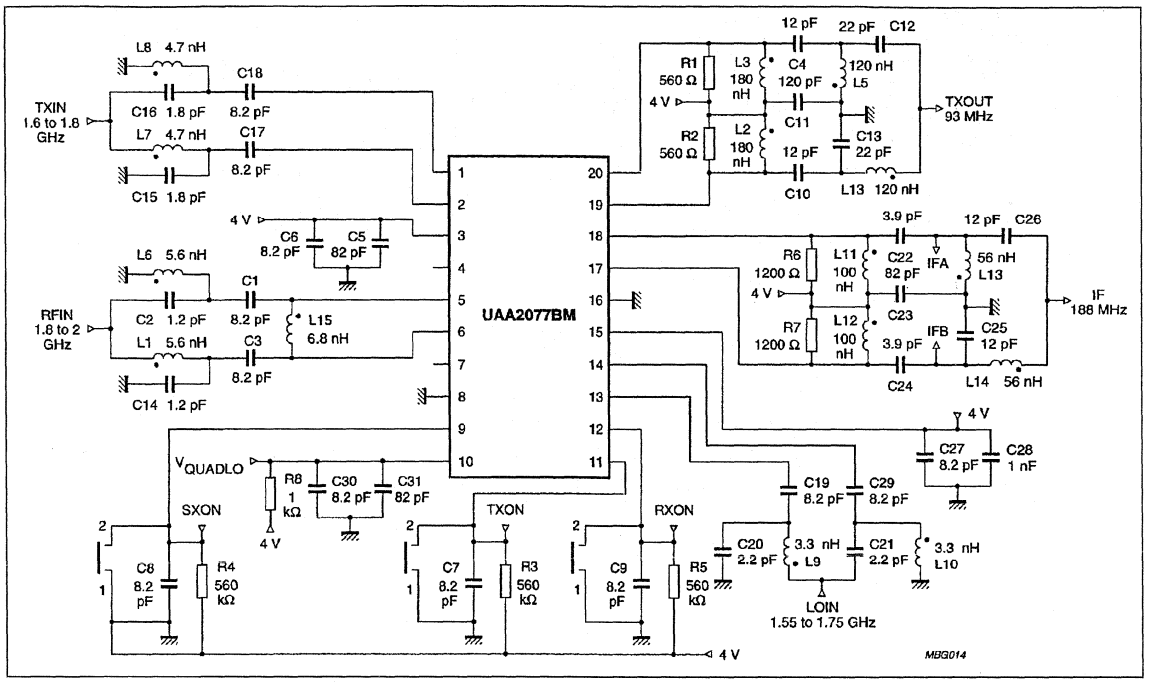


Fig. 26 UAA2077BM application diagram

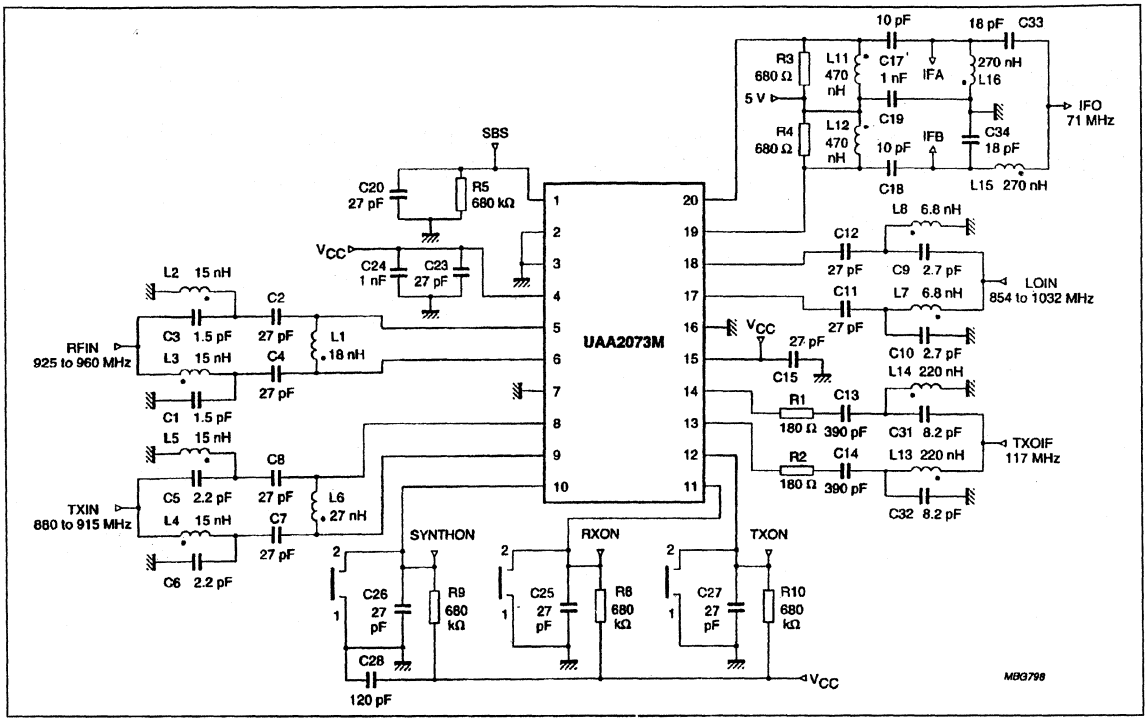


Fig. 27 UAA2073M application diagram

7.2 Component lists

Component values for the UAA2077BM demoboard are indicated below.

Table 3 Demo board Component List

Reference	Value	Type / Size	Reference	Value	Type / Size
L1	5.6 nH	0603 SMD	C13	22 pF	0805 SMD
L2	180 nH	0805 SMD	C14	1.2 pF	0603 SMD
L3	180 nH	0805 SMD	C15	1.8 pF	0603 SMD
L4	120 nH	0805 SMD	C16	1.8 pF	0603 SMD
L5	120 nH	0805 SMD	C17	8.2 pF	0603 SMD
L6	5.6 nH	0603 SMD	C18	8.2 pF	0603 SMD
L7	4.7 nH	0603 SMD	C19	8.2 pF	0603 SMD
L8	4.7 nH	0603 SMD	C20	2.2 pF	0603 SMD
L9	3.3 nH	0603 SMD	C21	2.2 pF	0603 SMD
L10	3.3 nH	0603 SMD	C22	3.9 pF	0805 SMD
L11	100 nH	0805 SMD	C23	82 pF	0805 SMD
L12	100 nH	0805 SMD	C24	3.9 pF	0805 SMD
L13	56 nH	0805 SMD	C25	12 pF	0805 SMD
L14	56 nH	0805 SMD	C26	12 pF	0805 SMD
L15	6.8 nH	0603 SMD	C27	8.2 pF	0805 SMD
C1	8.2 pF	0603 SMD	C28	1 nF	1206 SMD
C2	1.2 pF	0603 SMD	C29	8.2 pF	0603 SMD
C3	8.2 pF	0603 SMD	C30	8.2 pF	0805 SMD
C4	12 pF	0805 SMD	C31	82 pF	0805 SMD
C5	82 pF	0805 SMD	R1	560 Ω	0805 SMD
C6	8.2 pF	0805 SMD	R2	560 Ω	0805 SMD
C7	8.2 pF	0805 SMD	R3	560 k Ω	0805 SMD
C8	8.2 pF	0805 SMD	R4	560 k Ω	0805 SMD
C9	8.2 pF	0805 SMD	R5	560 k Ω	0805 SMD
C10	12 pF	0805 SMD	R6	1.2 k Ω	0805 SMD
C11	120 pF	0805 SMD	R7	1.2 k Ω	0805 SMD
C12	22 pF	0805 SMD	R8	1 k Ω	0805 SMD

Component values for the UAA2073M demoboard are indicated below.

Table 4 Demo board Component List

Reference	Value	Type / Size
R1	180 Ω	0805 SMD
R2	180 Ω	0805 SMD
R3	680 Ω	0805 SMD
R4	680 Ω	0805 SMD
R5	680 kΩ	0805 SMD
R8	680 kΩ	0805 SMD
R9	680 kΩ	0805 SMD
R10	680 kΩ	0805 SMD
C1	1.5 pF	0805 SMD
C2	27 pF	0805 SMD
C3	1.5 pF	0805 SMD
C4	27 pF	0805 SMD
C5	2.2 pF	0805 SMD
C6	2.2 pF	0805 SMD
C7	27 pF	0805 SMD
C8	27 pF	0805 SMD
C9	2.7 pF	0805 SMD
C10	2.7 pF	0805 SMD
C11	27 pF	0805 SMD
C12	27 pF	0805 SMD
C13	390 pF	0805 SMD
C14	390 pF	0805 SMD
C15	27 pF	0805 SMD
C17	10 pF	0805 SMD
C18	10 pF	0805 SMD
C19	1 nF	0805 SMD
C20	27 pF	0805 SMD
C23	27 pF	0805 SMD
C24	1 nF	0805 SMD
C25	27 pF	0805 SMD
C26	27 pF	0805 SMD
C27	27 pF	0805 SMD
C28	120 pF	0805 SMD
C31	8.2 pF	0805 SMD
C32	8.2 pF	0805 SMD
C33	18 pF	0805 SMD
C34	18 pF	0805 SMD
L1	18 nH	0805 SMD
L2	15 nH	0805 SMD
L3	15 nH	0805 SMD
L4	15 nH	0805 SMD
L5	15 nH	0805 SMD
L6	27 nH	0805 SMD
L7	6.8 nH	0805 SMD
L8	6.8 nH	0805 SMD
L11	470 nH	1008 SMD
L12	470 nH	1008 SMD
L13	220 nH	0805 SMD
L14	220 nH	0805 SMD
L15	270 nH	1008 SMD
L16	270 nH	1008 SMD

7.3 Layout and assembly drawings

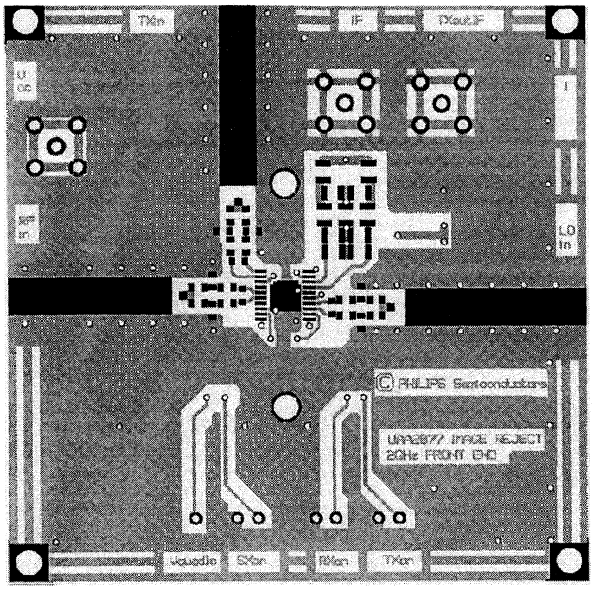


Fig. 28 UAA2077XM Demo board - Layer 1

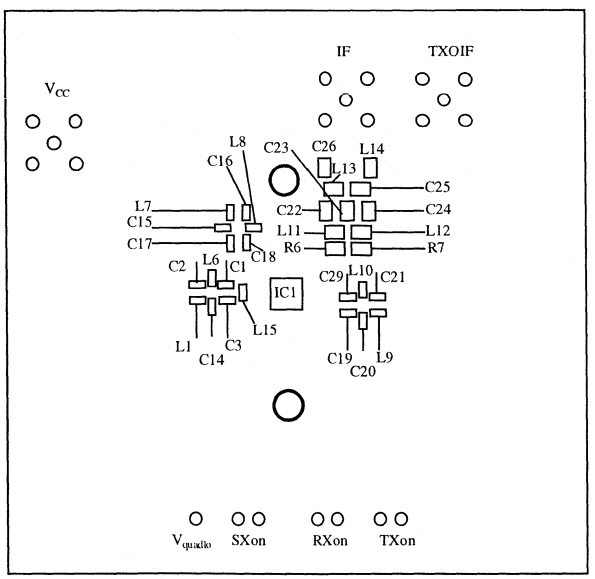


Fig. 29 UAA2077XM Demo board - Layer 1 Assembly

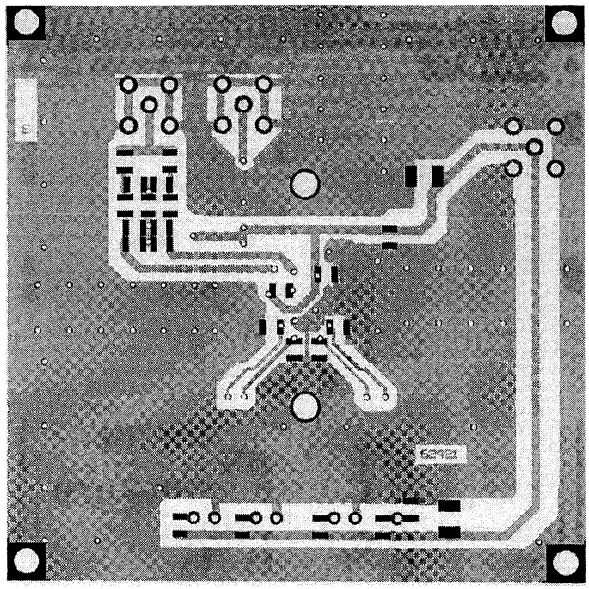


Fig. 30 UAA2077XM Demo Board - Layer 2 Layout

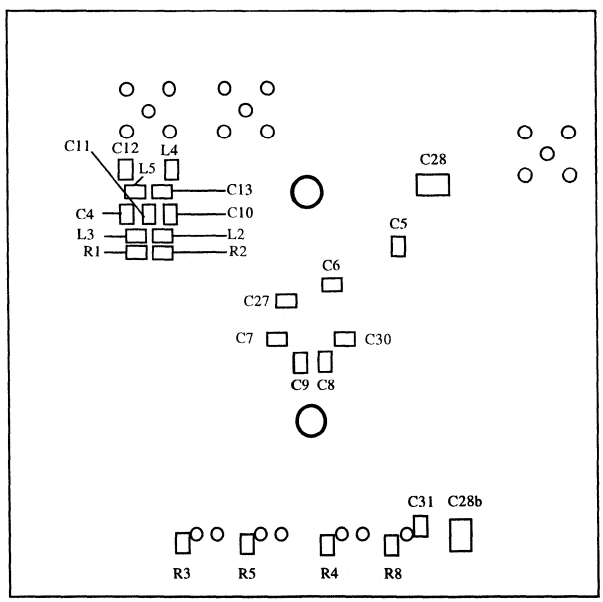


Fig. 31 UAA2077XM Demo Board - Layer 2 Assembly

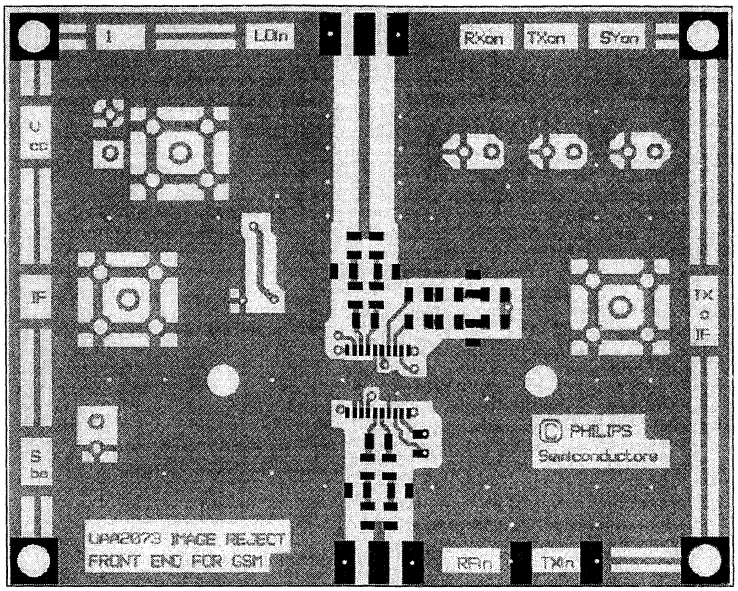


Fig. 32 UAA2073XM Demo Board - Layer 1 Layout

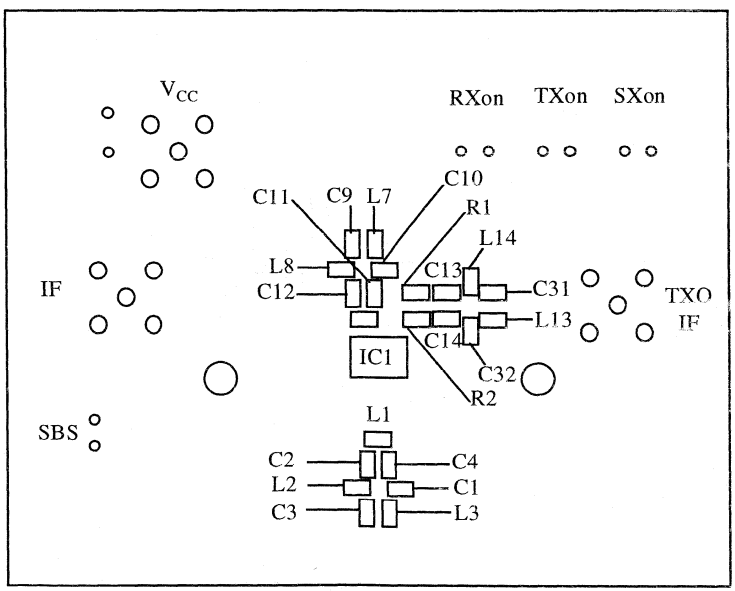


Fig. 33 UAA2073XM Demo board - Layer 1 Assembly

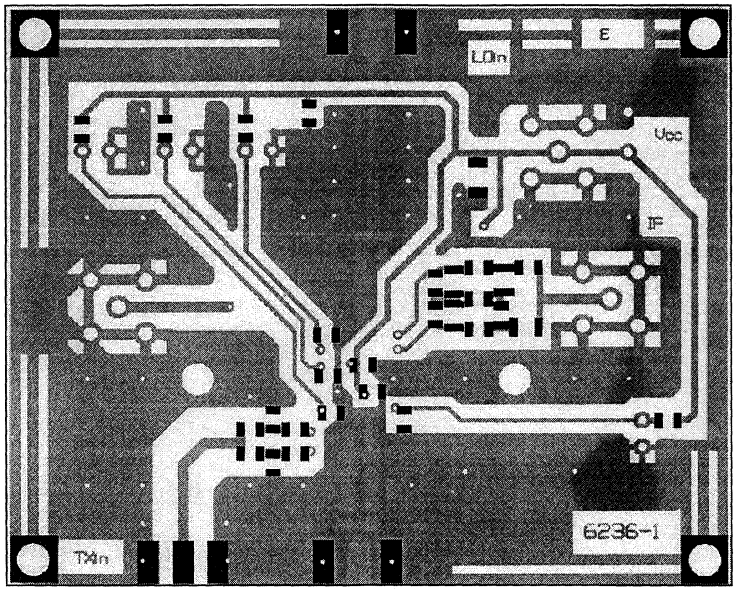


Fig. 34 UAA2073XM Demo Board - Layer 2 Layout

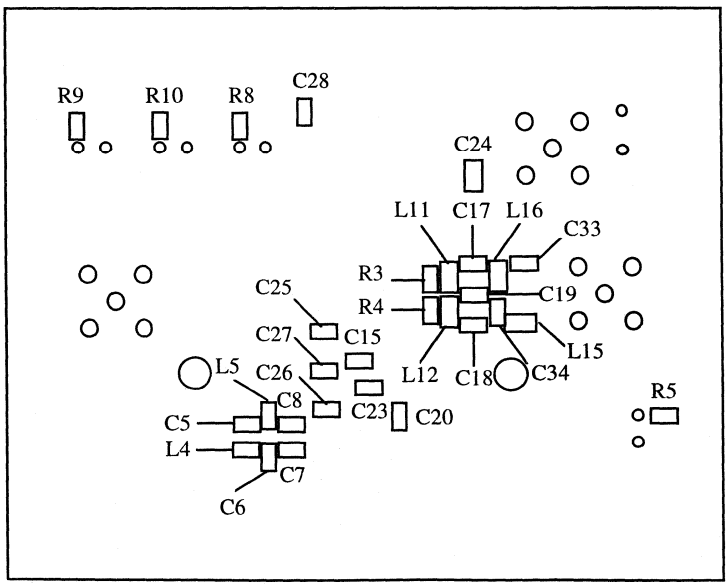


Fig. 35 UAA2073XM Demo Board - Layer 2 Assembly

8. REFERENCES

[1] UAA2072M Image rejecting front-end for GSM applications
Datasheet - November 94

[2] UAA2073M Image rejecting front-end for GSM applications
Datasheet - 07 December 95

[3] UAA2073AM Image rejecting front-end for GSM applications
Datasheet

[4] UAA2077AM Image rejecting front-end for DECT applications
Datasheet -04 July 96

[5] UAA2077BM 2 GHz Image rejecting front-end
Datasheet - 09 January 96

[6] UAA2077CM 2 GHz Image rejecting front-end
Datasheet

[7] OM5045 DECT Radio Design
Application note (report n°AN95096) - 31 October 1995

Summary

This report is intended to provide support for designing power amplifier for DCS/PCS applications.

It contains a description of the power amplifier as well as a brief overview of interstage and input /output matching .

An application example of the CGY2021G is given by means of board description for testing ,recommendations for use ,measurement results ,and performances.

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1. INTRODUCTION

This note describes the application of RF monolithic GaAs devices in plastic SMD packages for DCS/PCS power amplifiers.

Their main features are:

-low cost

-100% SMD

-high performance

-low voltage operation

-high efficiency

2. PINNING

The pinning is shown in Fig.1.

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/VDD4	6 to8	PA output and supply voltage
GND	9 to 17	ground
DETO	18	detector output
VGG1	19	first and second stages gate bias input voltages
GND	20 to 26	ground
RFI	27	PA input
GND	28	ground
VDD1	29	drain first stage and supply
GND	30	ground
VGG2	31	third and fourth stages gate bias input voltages
GND	32	ground
VDD2	33	drain second stage and supplt
GND	34 to 41	ground
VDD3	42	drain third stage and supply
GND	43 to 48	ground

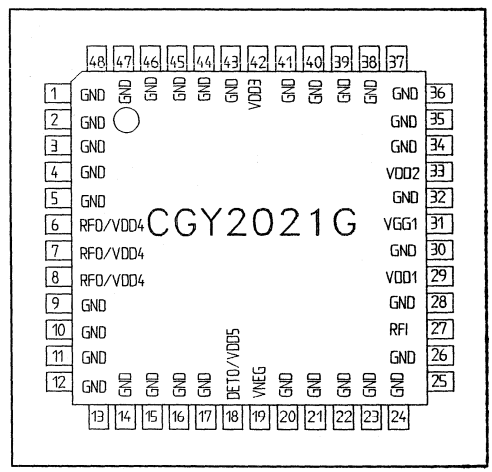

Fig. 1 Pin configuration

3. CIRCUIT DESCRIPTION

3.1 Power amplifier

The amplifier is based on a monolithic integrated four stages device using GaAs FET technology in a plastic package.
This device is able to deliver 33 dBm and up to 35 dBm with 4.4 V drain operation.
As described in Fig.2. this device exhibits inter stage matching circuits implemented both on the board and on the chip.Each matching consists of a serie,parallel combination of inductors and capacitors.The serie elements are generally capacitive (MIM capacitors on chip) while the parallel ones can be inductive or capacitive.The parallel matching includes bias pathes and isolation networks for the drains of the different stages.
The input and output matching circuits are implemented on board.
The power amplifier is built on a low cost printed circuit board in association with a switching circuit for pusled applications.This one is able to provide a suitable switching time for DCS and PCS applications.

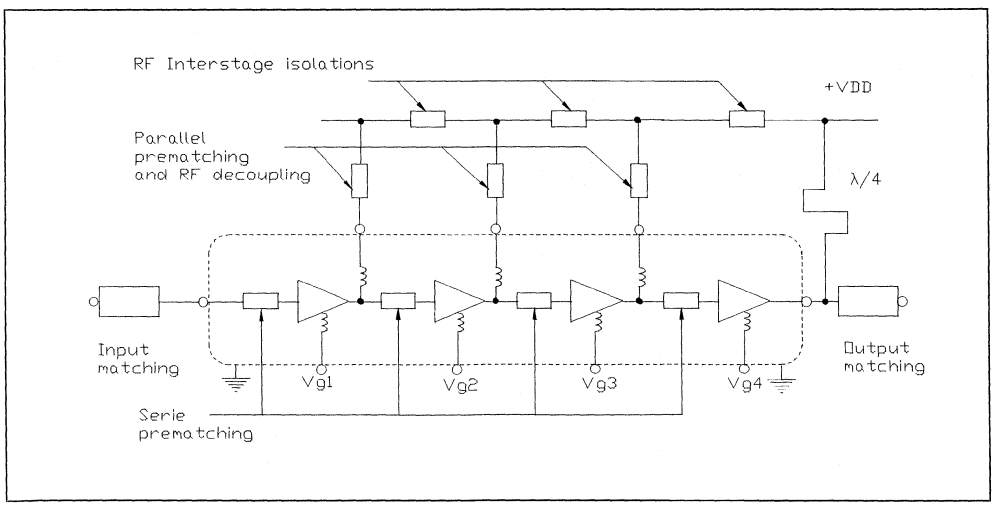

Fig. 2 Power amplifier

3.2 Interstage matchings

The general philosophy used for interstage matching is described when looking at Fig.3.

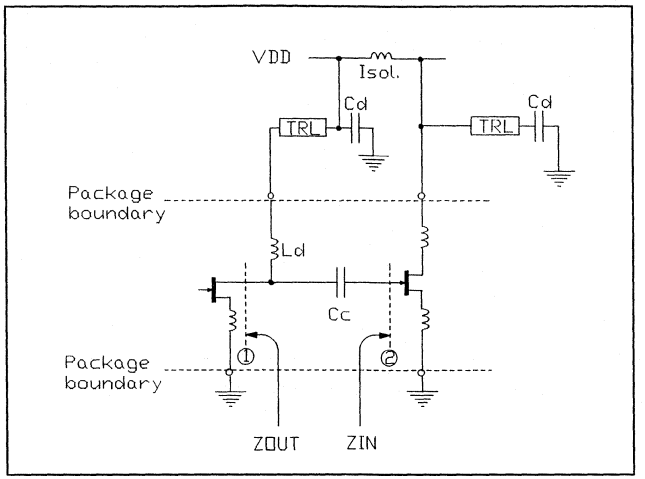

Fig. 3 Interstage matching

The aim is to match the input impedance Zin from a stage in the reference plane 2 to the output impedance Zout of the previous one in the reference plane 1.
This can be accomplished with the interstage coupling capacitor Cc(MIM) on chip ,the bonding wire between the drain and the package lead ,the external transmission line TRL printed on the board and the decoupling capacitor Cd.
As Ld and Cc cannot be adjusted (fixed values),the interstage matching optimisation is carried out by tuning TRL and Cd .

3.3 Drain control and switching circuits

When used in DCS/PCS applications the power amplifier needs to be switched on and off by means of serie element .
For this purpose we use a circuit as described in Fig.4.

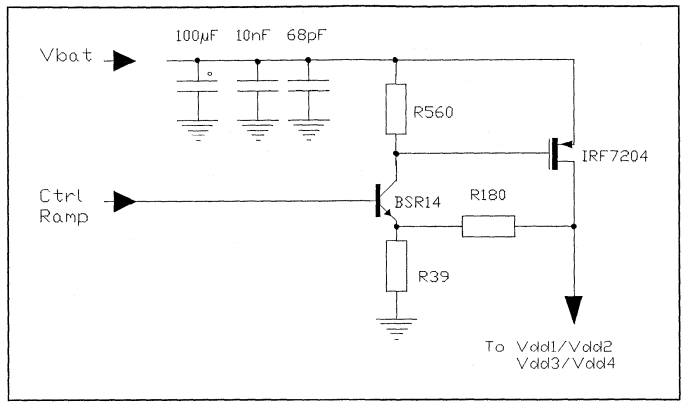

Fig. 4 Drain control and switching circuit

An other way to switch and control the power amplifier is to make use of a specific modulator (UBA1710) intended for these applications with a banbwidth which is around 5 Mhz.
The simplified block diagram is represented in fig .5.
This circuit has the following features :
-Low Rdson N MOS for the switchings
-Voltage tripler for the N MOS control
-Adjustable negative bias for the PA
-Power management disabling the PA when the negative bias is not present
-Stand by gate to switch off the circuit when this one is not in use

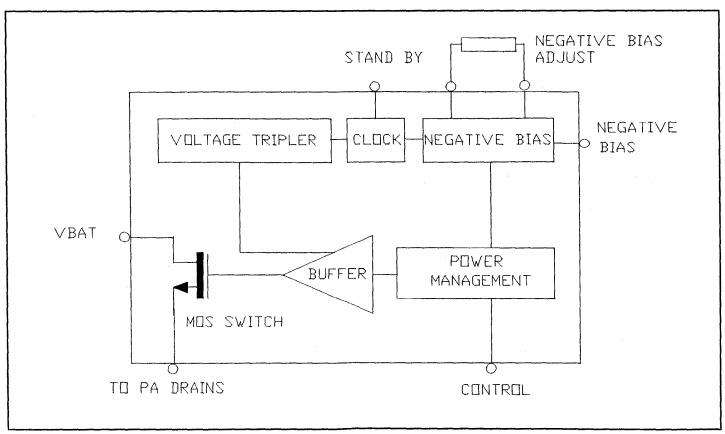

Fig. 5 Modulator

4. MODE OF OPERATION

The device must be operated under pulsed conditions .
The commonly mode of operation in use is class A.
The amplifier must be biased with a negative voltage on the gates in the range of -1V to -2V .
A typical value for the best operation is :-1.6V .
For the drain , the pulsed voltage applied is comprised between 0V and 4.8V ,depending on the powel level we need at the output .
If used with a PMOS as drain control and switch , a negative bias has to be built on the board .
With the use of a UBA1710 modulator , no additionnal negative bias is needed as this one is available in the modulator .
For the RF signal applied to the input port a typical value is 0 dBm continue wave in the DCS/PCS frequency range .

5. GENERAL CHARACTERISTICS

DC CHARACTERISTICS:

VDD=4.5V;Tamb=25°C;peak current values during burst; general operating conditions applied; unless otherwise specified .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Pins RFO/V_{DD4},V_{DD3},V_{DD2},V_{DD1},and DETO/V_{DD5}						
V_{DD}	positive supply voltage		-	4.5	-	V
I_{DD}	positive peak supply current		-	1.4	-	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	-	-1.6	-	V
V_{GG2}	negative supply voltage	note 1	-	-1.6	-	V
I_{GG1} + I_{GG2}	negative peak supply voltage		-	-	2	mA

Note
1- The negative bias V_{GG} must be applied 10µS before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off .

AC-CHARACTERISTICS:

VDD=4.5V; Tamb=25°C; general operating conditions applied; unless otherwise specified .
Measured and guaranteed on CGY2021G evaluation board .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power amplifier						
Pi	input power		-2	-	+2	dBm
S11	input return loss	50 Ω source;note1	-	-	-10	dB

fRF	RF frequency range	DCS	1710	-	1785	MHz
fRF	RF frequency range	PCS	1850	-	1910	MHz
Po(max)	maximum output power	Tamb=25°C; V_{DD}=4.5V	33	34	-	dBm
Po(max)	maximum output power	Tamb=-20 to +85°C;V_{DD}=4.2V	31		-	dBm
η	efficiency	DCS; at Po(max)	40	50	-	%
η	efficiency	PCS; at Po(max)	-	47	-	%
Rs	optimum serie load impedance		-	6	-	Ω
Cs	optimum serie load capacitance		-	11	-	pF
Po(off)	isolation	PA off; Pi=0dBm	-	-50	-	dBm
N_{RX}	output noise in RX band		-	-	-121	dBm/Hz
H2	2nd harmonic level		-	-40	-	dBc
H3	3rd harmonic level		-	-35	-	dBc
Stab	stability	note 2	-	-	-50	dBc
Power sensor driver						
$P_{O(DET)}$			-	-25	-	dBc

Notes

1. Including the 82Ω resistor connected in parallel at the power amplifier input on the evaluation board .
2. The device is adjusted to provide nominal value of load power into a 50 Ω load .The device is switched off and a 6:1 360 electrical degrees during a 60 seconds test period .

6. CIRCUIT DIAGRAM AND RECOMMENDATIONS FOR USE

6.1 Circuit diagram

The circuit diagram used for testing and described in Fig.6 is the one making use of a CGY2021G in association with the UBA1710 .

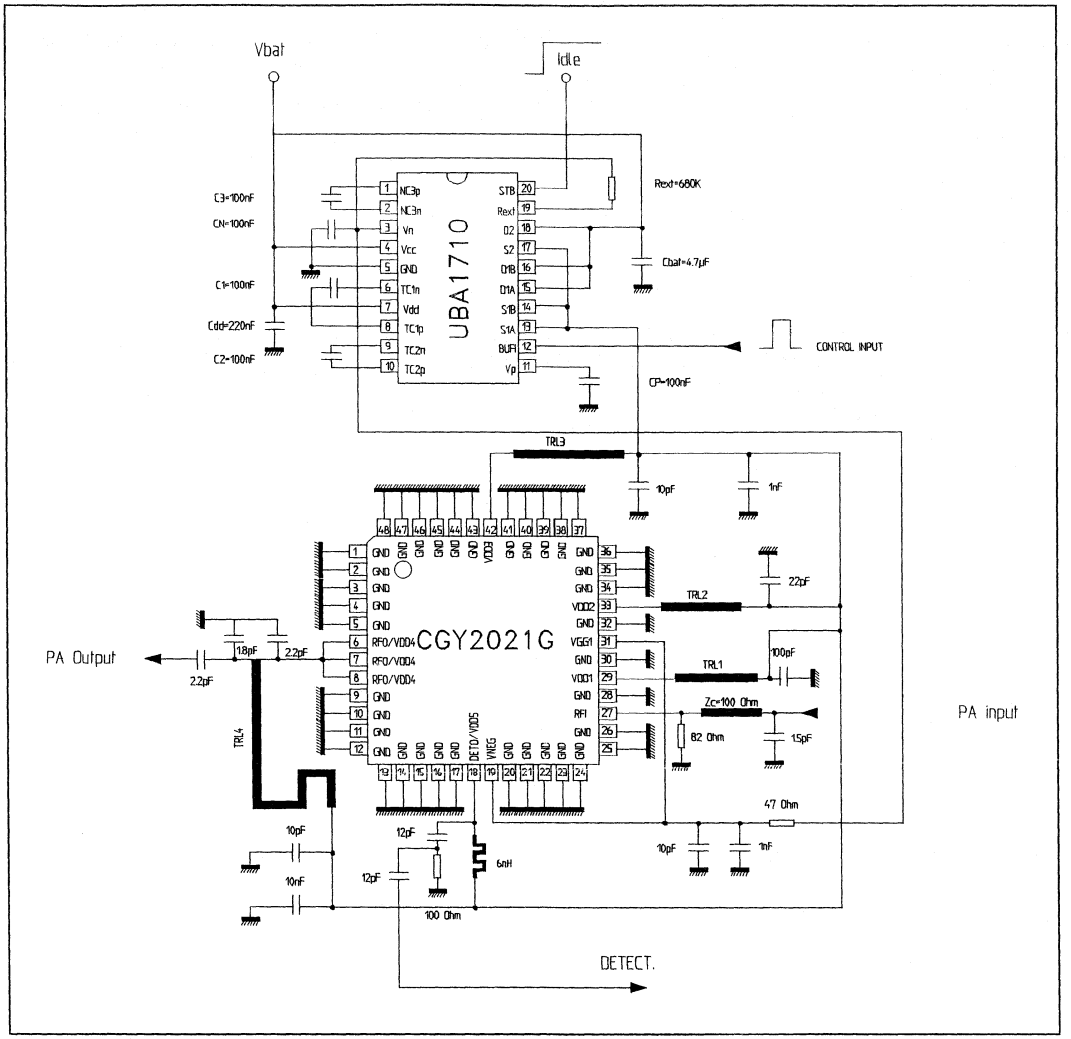

Fig. 6 Circuit diagram

6.2 Recommendations for use

6.2.1 Without UBA1710

As the device makes use of the normally on MESFET technology , a negative biasing applied to the gates must be set prior the drain voltage in order to avoid any power dissipation exess .

6.2.2 With UBA1710

When used with a power modulator (UBA1710) no particular precaution is necessary as long as the power amplifier is connected to the UBA1710 .

The power modulator has a built in power management that disables the drain voltage as long as the negative bias applied to the gates is higher than -1V .

7. PRINTED CIRCUIT BOARD LAYOUT-LIST OF COMPONENTS

7.1 Circuit layout.

The demoboard layout making use of a CGY2021G and a UBA1710 is given in fig. 7 .
The characteristics of the substrate in use for the PCB are as following:
-substrate type:FR4 double clad
-Relative permetivity:εr=4.7
-Thickness:H=0.8mm
-Size:35x42mm

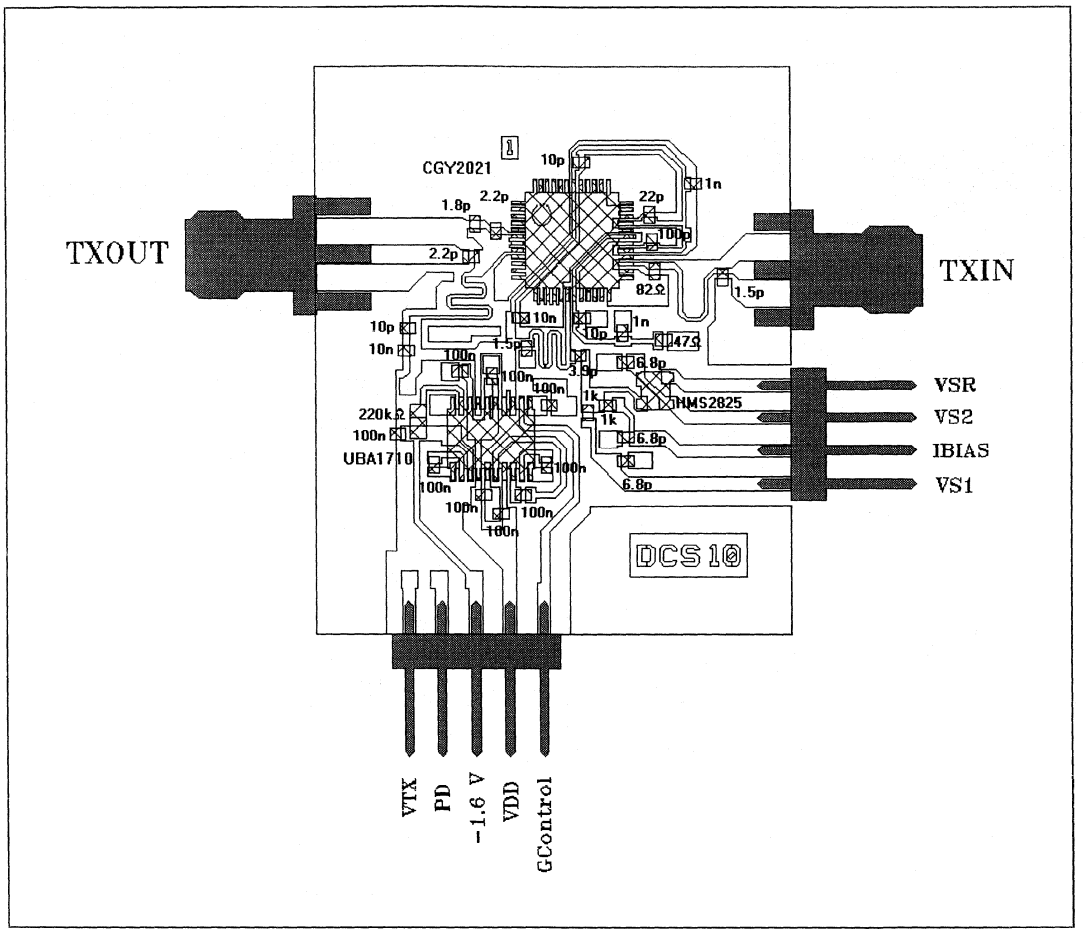

Fig. 7 Circuit layout

7.2 Part list DCS power amplifier with UBA1710

CAPACITORS (Size:0603)	
VALUE	**NUMBER**
1.5 pF	2
1.8	1
2.2	2
3.9 pF	1
6.8 pF	3
10 pF	3
22 pF	1
100 pF	1
1 nF	2
10 nF	2
100 nF	9

RESISTORS (Size:0603)	
VALUE	**NUMBER**
47 Ω	1
82 Ω	1
1kΩ	2
220kΩ	1

ACTIVE COMPONENTS	
CGY2021G	1
UBA1710	1
HMS2825	1

8. THERMAL CHARACTERISTICS

8.1 Thermal Characteristics

The maximum average dissipation is 1.3 W for a channel temperature not exeeding Tch=150 °C .

The thermal impedance from channel to ambient is typically Rthjc=45 K/W .This impedance is measured under nominal DCS/PCS pulse conditions .

8.2 Power derating curve

For safety and reliability reasons a power derating curve relative to the power dissipation is introduced and given in Fig 8.

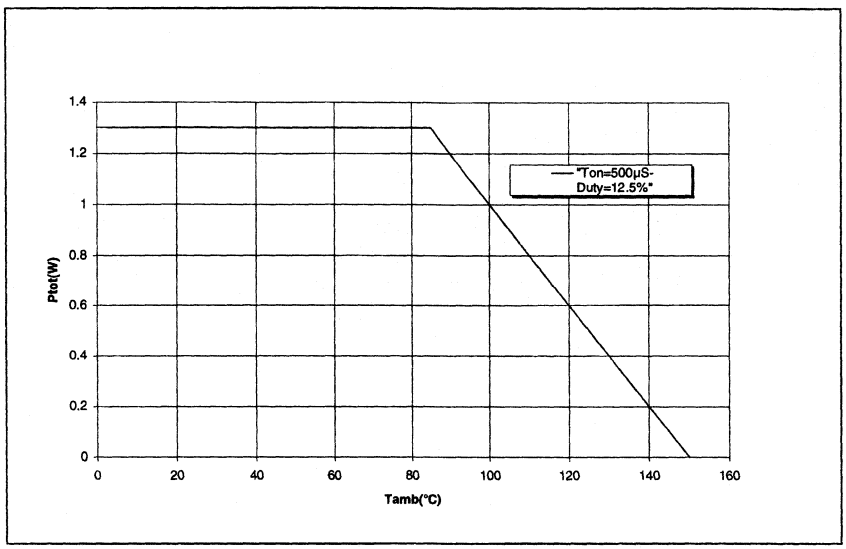

Fig. 8 Power derating

9. ELECTRICAL CHARACTERISTICS

9.1 Output power and efficiency as a function of drain voltage

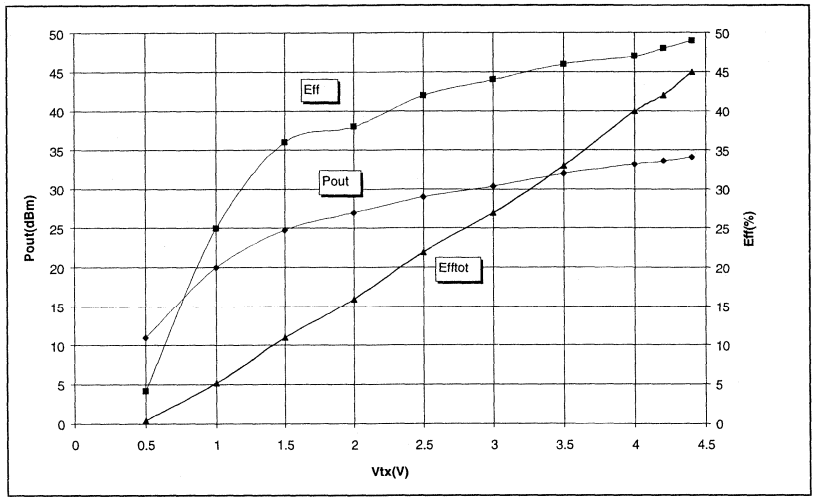

Fig. 9 Output power and efficiency versus drain voltage

9.2 Output power and return losses as a function of frequency

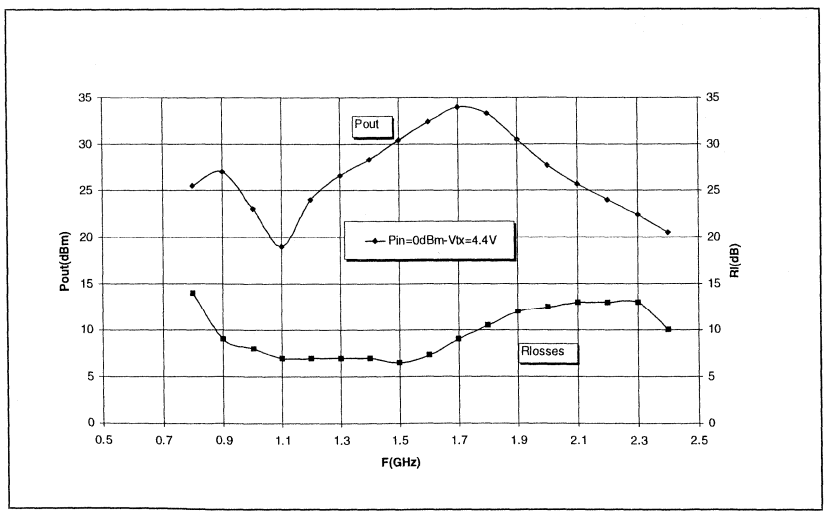

Fig. 10 Output power and input return losses versus frequency

9.3 Small signal gain and input/ouput return losses

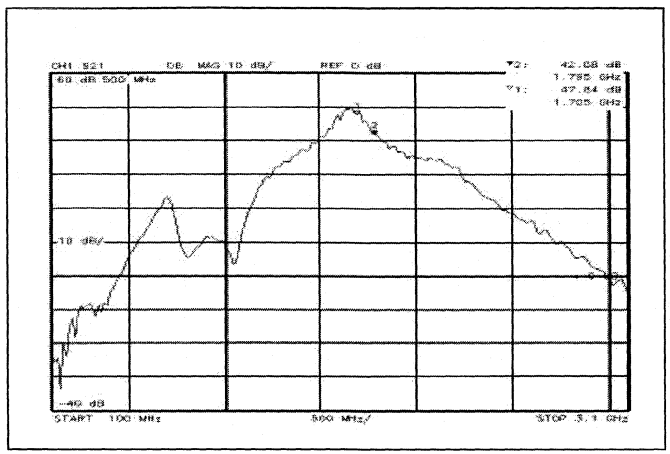

Fig. 11 Small signal gain versus frequency

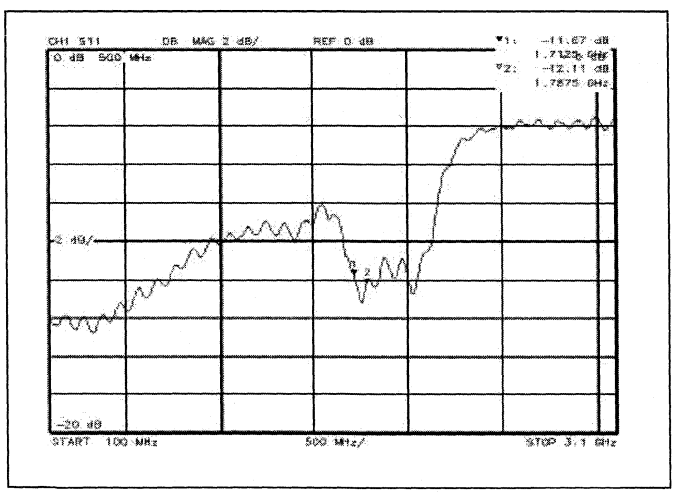

Fig. 12 Small signal input return losses

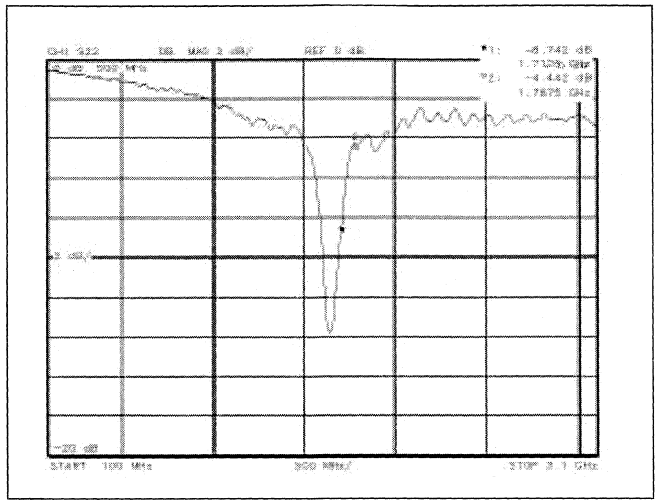

Fig. 13 Small signal output return losses

9.4 Output power as a function of input power

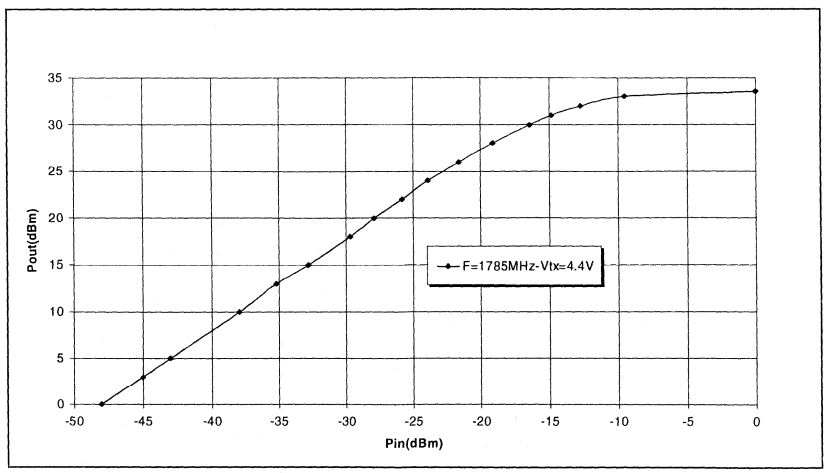

Fig. 14 Output power versus input power

9.5 Spurious gain as a function of frequency

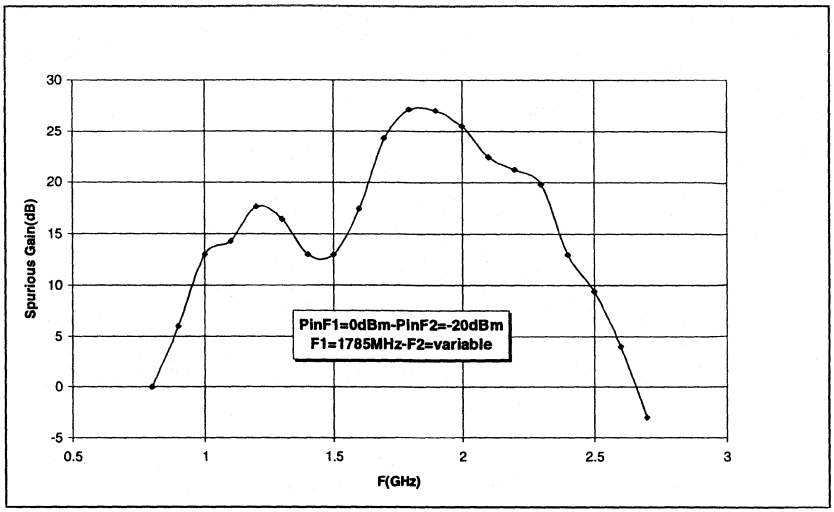

Fig. 15 Spurious gain versus frequency

9.6 Intermodulation gain as a function of output power

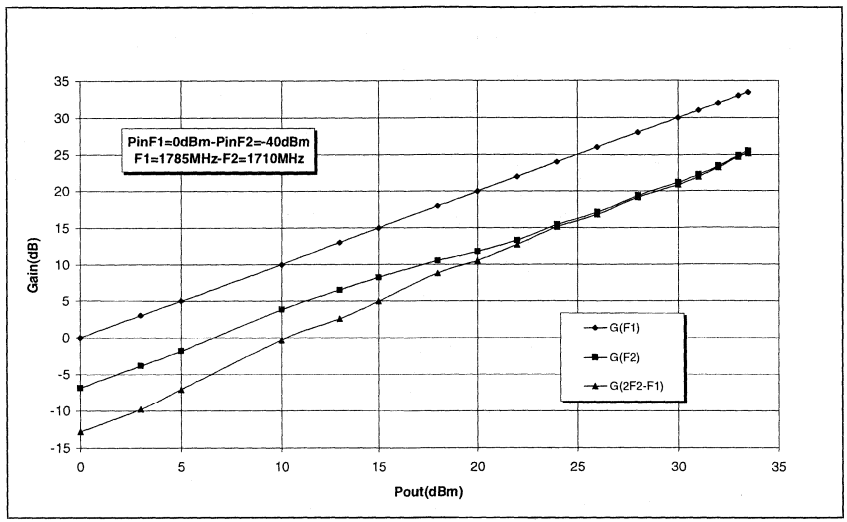

Fig. 16 Intermodulation gain versus output power

9.7 AM/PM conversion as a function of output power

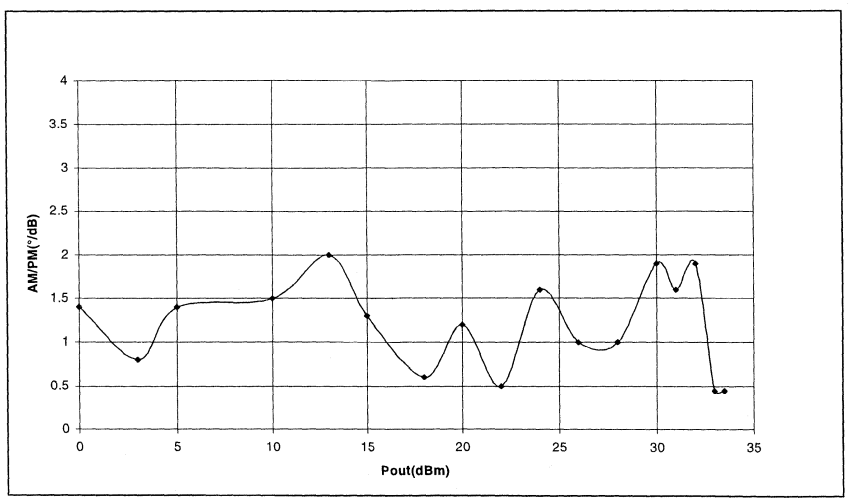

Fig. 17 AM/PM conversion versus output power

9.8 AM/AM conversion as a function of output power

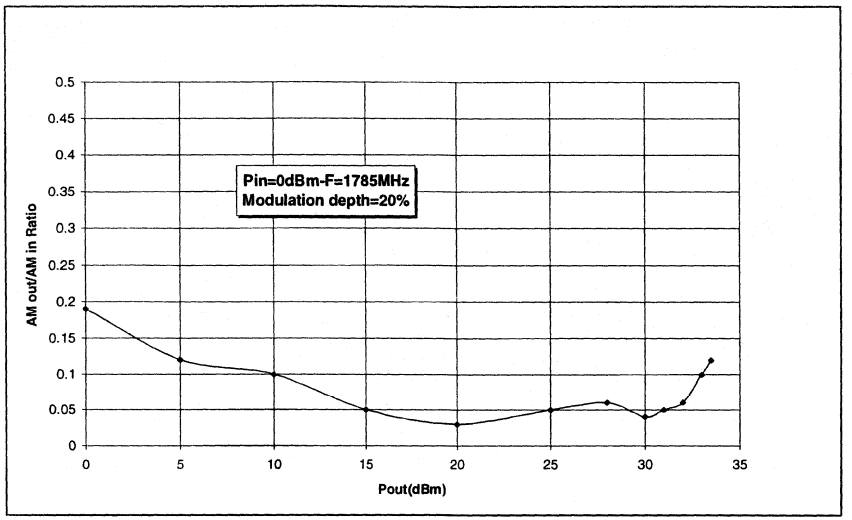

Fig. 18 AM/AM conversion versus output power

9.9 Noise conversion as a function of frequency

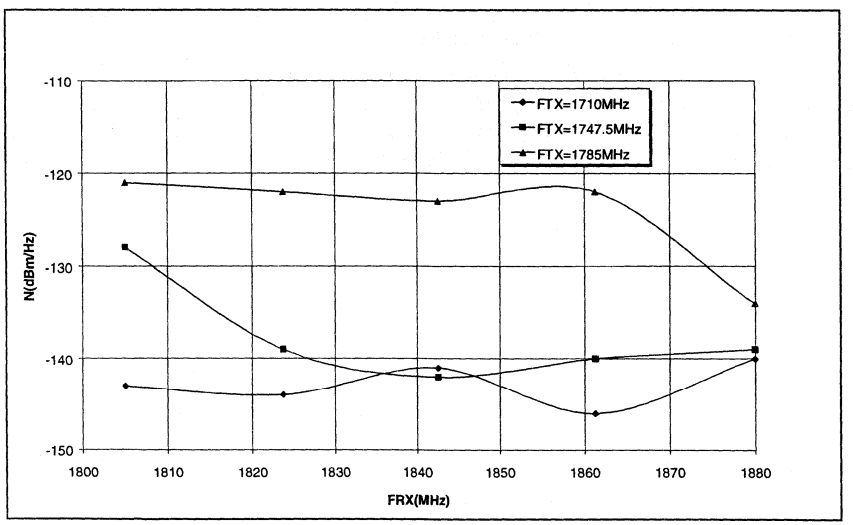

Fig. 19 Noise conversion versus frequency

9.10 Settling time in association with UBA1710

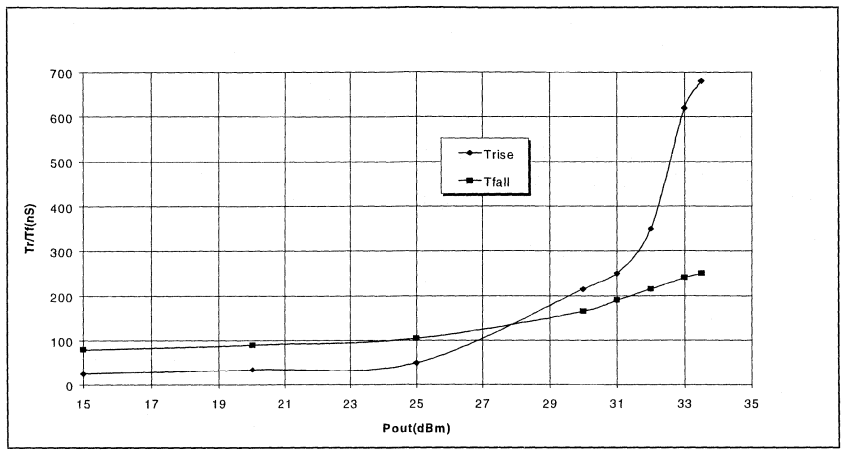

Fig. 20 Settling time versus output power

10. MODELIZATION AND SIMULATION

As the non linear models of the MESFET in use for the CGY2021G are known with a good accuracy , we can predict the dynamic performances of the power amplifier .

A relevant simulation concerning the output power and efficiencies versus the voltage exhibit a close correlation to the nominal measurements performed on the demoboard .See fig. 21
The CGY2021G models including the package parasitics are available on request for simulations and power amplifier designs in other frequency ranges like PCS for example .

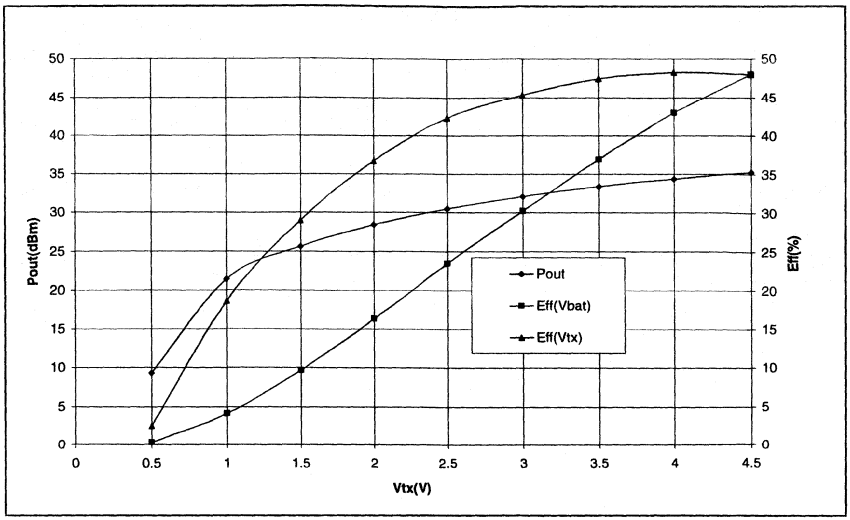

Fig. 21 Power control simulation

Summary

This report is intended to provide support for designing the power control in use for GSM/DCS/PCS applications with GaAs power amplifier.

It contains a general description of the circuit as well as a more in-depth analyse of the different blocks implemented in the controller .

An application example of the UBA1710M is given by means of the board description for testing the performances.

Some additional informations concerning the optimisation of the modulator when this one is used under GSM/DCS/PCS standards are also available in this document .

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1. INTRODUCTION

This note describes the application of monolithic silicon devices in plastic SMD packages for DCS/PCS power control of GaAs amplifiers.

Their main features are:

-low cost

-100% SMD

-high performance

-low Rdson for the MOS switches

-Negative voltage on board

-Power management and idle mode

-Wide bandwidth for the feedback loop amplifier

-4.8 V operation

2. PINNING

The pinning is shown in Fig.1.

SYMBOL	PIN	DESCRIPTION
NC3P	1	charge pump tank capacitor
NC3N	2	charge pump tank capacitor
VN	3	negative bias voltage
Vcc	4	analog. supply voltage
GND	5	ground
TC1N	6	charge pump tank capacitor
Vdd	7	digital supply voltage
TC1P	8	charge pump tank capacitor
TC2N	9	charge pump tank capacitor
TC2P	10	charge pump tank capacitor
Vp	11	positive tripler voltage
BUFI	12	buffer input
S1A	13	power MOS 1 source A
S1B	14	power MOS 1 source B
D1A	15	power MOS 1 drain A
D1B	16	power MOS 1 drain B
S2	17	power MOS 2 source
D2	18	power MOS 2 drain
Rext	19	external resistor for VN
STB	20	stand by input (active high)

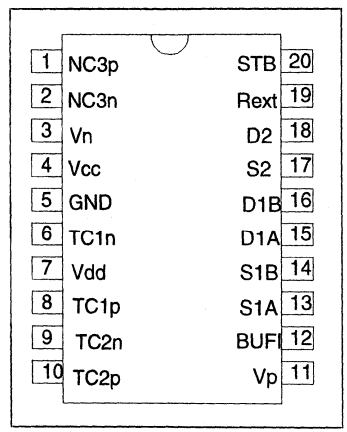

Fig. 1 Pin configuration

3. CIRCUIT DESCRIPTION

3.1 General block diagram

As described in fig.2. the controller has a built in double power MOS to switch on and off the drain voltages applied to the power amplifier in order to control the power level of the transmit path .

These MOS power devices can be connected in parallel or separately to the power amplifier output and driver stages drain circuits .

As we use N MOS transistors for switching , a buffer is used to drive these ones . The buffer output voltage capability is much higher than the battery voltage in order to saturate and turn on the power MOS at the rated maximum output power level with minimum insertion losses .

A voltage tripler is used to supply the buffer . This voltage converter is necessary to allow high positive voltage swing at the buffer output to drive the power MOS devices .

A negative voltage is also built in to bias the gates of the GaAs power amplifier . This negative voltage can be adjust externally with a resistor . As the tripler voltage and the negative bias use charge pump circuits , an internal clock/oscillator drives simultaneously these two blocks .

The power management block disables the input control ramp applied to the buffer as long as the negative bias is not available .

Finally a stand by circuit can set the circuit in an idle mode when activated .

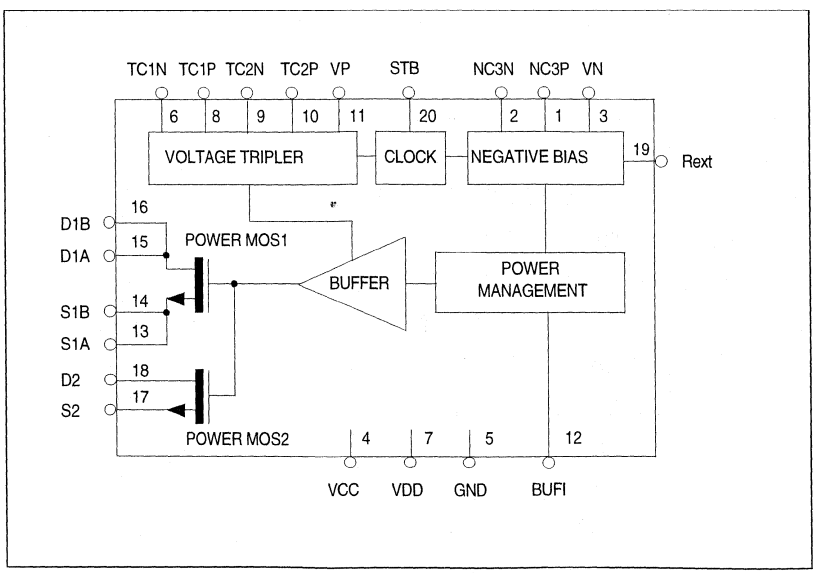

Fig. 2 General block diagram

3.2 Voltage tripler circuit

The voltage tripler is described in fig.3.

The circuit works on the basis of charge pump circuits with transferred charges from a capacitor to an other one .

In a first step , the switches S1 to S4 are closed (while S5 to S7 are opened) ,C1 is charged to Vbat .Then switches S5 to S7 are closed (S1 to S4 opened) and C1 is discharged in C2 with an additional voltage Vbat applied .The peak voltage across this capacitor is then 2*Vbat .

In a third step ,S1 to S4 are closed once more (with S5 to S7 opened) and now C2 discharges in C3 with an additional V bat applied to the previous peak voltage present across C2 (2*Vbat). This new voltage appearing across C3 is now 3*Vbat .

The group of switches are operated alternately through a switches control block as long as the Vtriple has not reached the value given by the ratio : [(R1+R2)/R2]*Vbg .

Vbg is the band gap voltage applied to the non inverting port of the comparator .

When this voltage value is reached the output level of the comparator goes to zero ,disabling the switches control and in turn stopping the capacitors charging/discharging process .

Theorically Vtriple is 3*Vbat , but practically the voltage is regulated at a constant level of 11.8V .

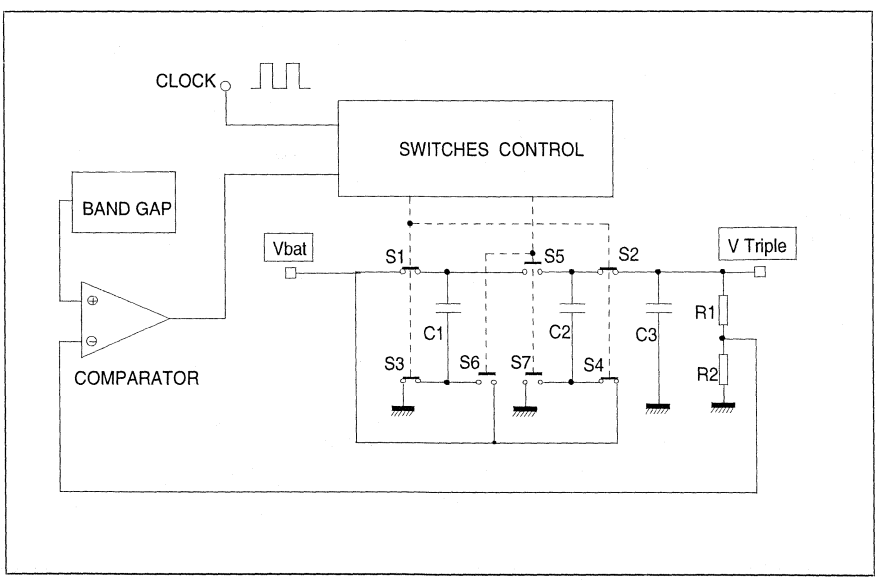

Fig. 3 Voltage tripler

3.3 Negative voltage

The negative voltage block diagram is given in fig.4.

As for the voltage tripler , the process in use is a charge pump circuit using diodes as switches .

At the starting point the negative voltage is zero and the voltage output level of the comparator is high ,

enabling the clock pulses to charge the capacitors C1 and C2 .

The voltage at the inverting port of the comparator is gradually pulled down as Vneg is decreasing toward negative values .When the voltage become zero ,the output of the comparator goes to zero , and in turn the pulses from the clock no longer charge the capacitors of the charge pump circuit and Vneg stabilises to a value determined by the band gap voltage and the resistors bridge .

The value of Vneg is given by the formula : Vneg = -[R2*Rext/R1(R2+Rext)]Vbg with R2 = 60kΩ ,R1 = 38.4kΩ and Vbg = 1.28 V .

As we can see the negative voltage can be adjust by mean of the external resistor Rext , and the range lies between -2 V for Rext = ∞ and 0 V for Rext = 0Ω .

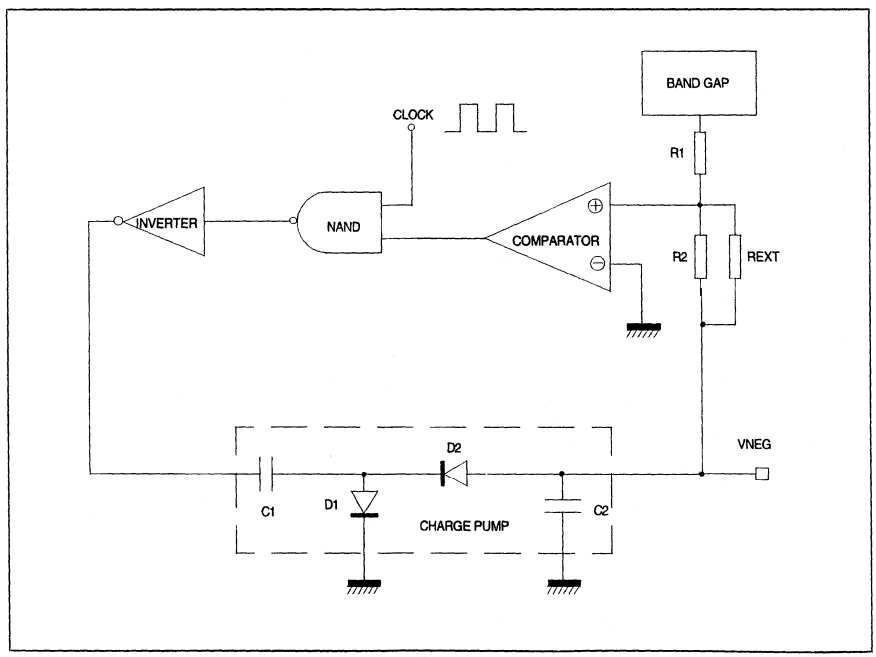

Fig. 4 Negative voltage circuit

3.4 Power management

The schematic of the power management circuit is given in fig.5.

The aim of this circuit is to prevent any signal from being applied to the buffer as long as the negative voltage is not at least -1 V .

In fact this does not allow any drain voltage to be applied to the power amplifier if the negative voltage is not low enough to prevent this one from excess of drain current .

For this purpose , a comparator in association with two MOS switches is used .

When the UBA1710M is turn on , Vneg is close to zero and a positive voltage is applied to the non inverting port of the comparator .The output voltage level of this one is high and the MOS switches SW1 /SW2 are respectively in off and on states .This situation prevent any control signal to be present at the buffer input .

When Vneg goes negative , the voltage at the comparator is pulled down and when this voltage is zero or less, SW1 /SW2 are on and off ,enabling the control signal to switch on the drain voltage .

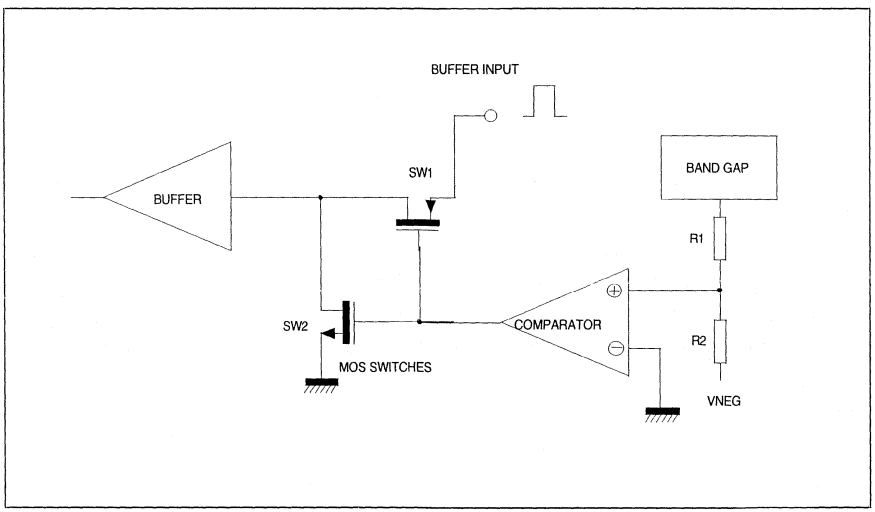

Fig. 5 Power management

3.5 Shut down circuit

When the UBA1710M modulator is not operating (within the bursts for example), and to avoid any unnecessary consumption ,the circuit can be set in an idle mode .

The circuit described in fig.6 ,comprises a MOS switch inserted between the battery and the rest of the modulator .

When a positive voltage (+Vbat) is applied to the stand by pin ,the modulator is in an idle state while this one is active with zero volt applied .

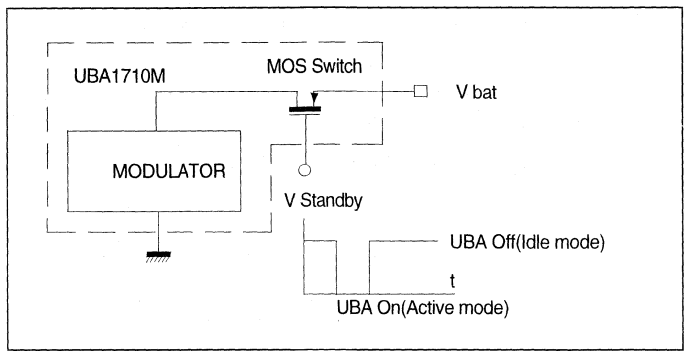

Fig. 6 Shut down circuit

3.6 Power MOS switch and buffer

In order to improve the bandwidth and the dynamic range of the association power MOS and buffer , a negative feedback is introduced by means of two resistors .The block diagram is given in fig.7.

The feedback ratio ,equal to R2/(R1+R2) is sufficient to insure a 2 MHz bandwidth minimum with an input signal ranging from 1.2 to 3.4 V .These values are important if the modulator has to be used in a control loop .

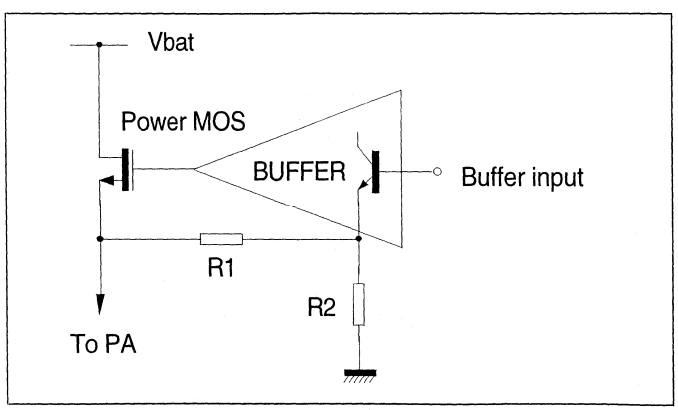

Fig. 7 Power switch and buffer

3.7 Oscillator

The oscillator (clock) in use in the UBA1710M is a source coupled CMOS multivibrator. The schematic is given in fig.8.

The oscillation frequency is 600 kHz and this one is given by the formula : F=I/(4*C*Vc) ,where I is the current source value ,C the coupling capacitor value and Vc is the voltage across the capacitor .

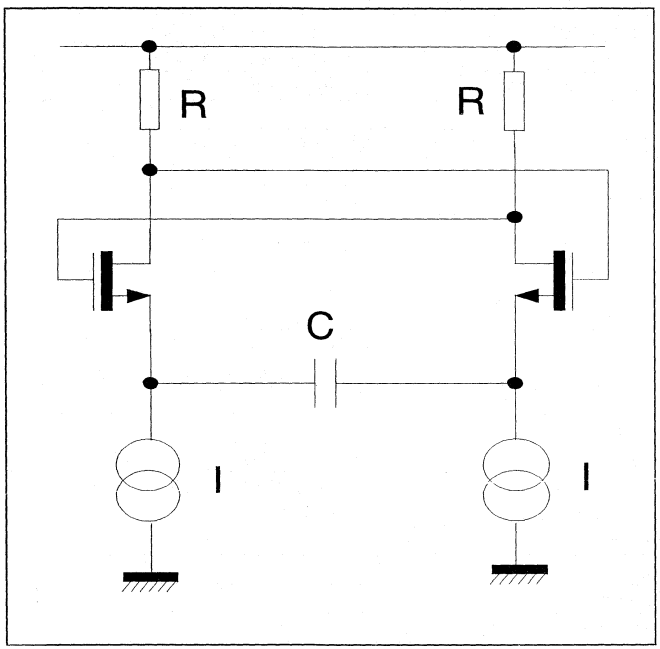

Fig. 8 Oscillator

4. MODE OF OPERATION

The device must be operated under pulse conditions with a power MOS driving current capability not exceeding 2.5 A peak (MOS1 and MOS2 connected in parallel) with a maximum duty cycle of 10% and a pulse width of 1 mS .

5. GENERAL CHARACTERISTICS

VDD=4.8V;Tamb=25°C; unless otherwise specified .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
Icc=Idd	peak supply current	power-up mode; PA on	-	12	-	mA
		power-down mode; PA off	-	5	-	mA
Istb	standby current	standby mode	-	0.1	1	µA
Power MOS1						
Rdson1	on resistance	Ids=1.3A	-	0.18	-	Ω
Power MOS2						
Rdson2	on resistance	Ids=0.4A	-	0.5	-	Ω
Clock circuit						
fclk	clock frequency		-	600	-	kHz
Voltage tripler						
Vpo	output voltage	with Ipo=2 mA	11.4	11.8	12.3	V
Vr(p-p)	amplitude ripple (peak-to-peak value)	with Ipo=2 mA C1=C2=100 nF; Cp=100 nF	-	20	-	mV
ton	turn-on-time		-	100	-	µS
Negative DC/DC converter						
Vno	output voltage	with Ino=250 µA; Rext=470kΩ	-1.5	-1.8	-2.0	V
Vr(p-p)	amplitude ripple (peak-to-peak value)	with Ino=250 µA, C3=100 nF; Cn=100 nF	-	2	-	mV
ton	turn-on-time		-	280	-	µS
MOS buffer amplifier						
Vil	LOW level input voltage		-	1.2	-	V
Vih	HIGH level input voltage		-	3.4	-	V
tsw	switching time from 0 to 4.5 V		-	1	-	µS

6. CIRCUIT DIAGRAM AND RECOMMENDATIONS FOR USE

6.1 Circuit diagram

With the circuit diagram given in fig.9 , we make use of a GaAs power amplifier for DCS/PCS applications as active device to be controlled by the modulator UBA1710M .

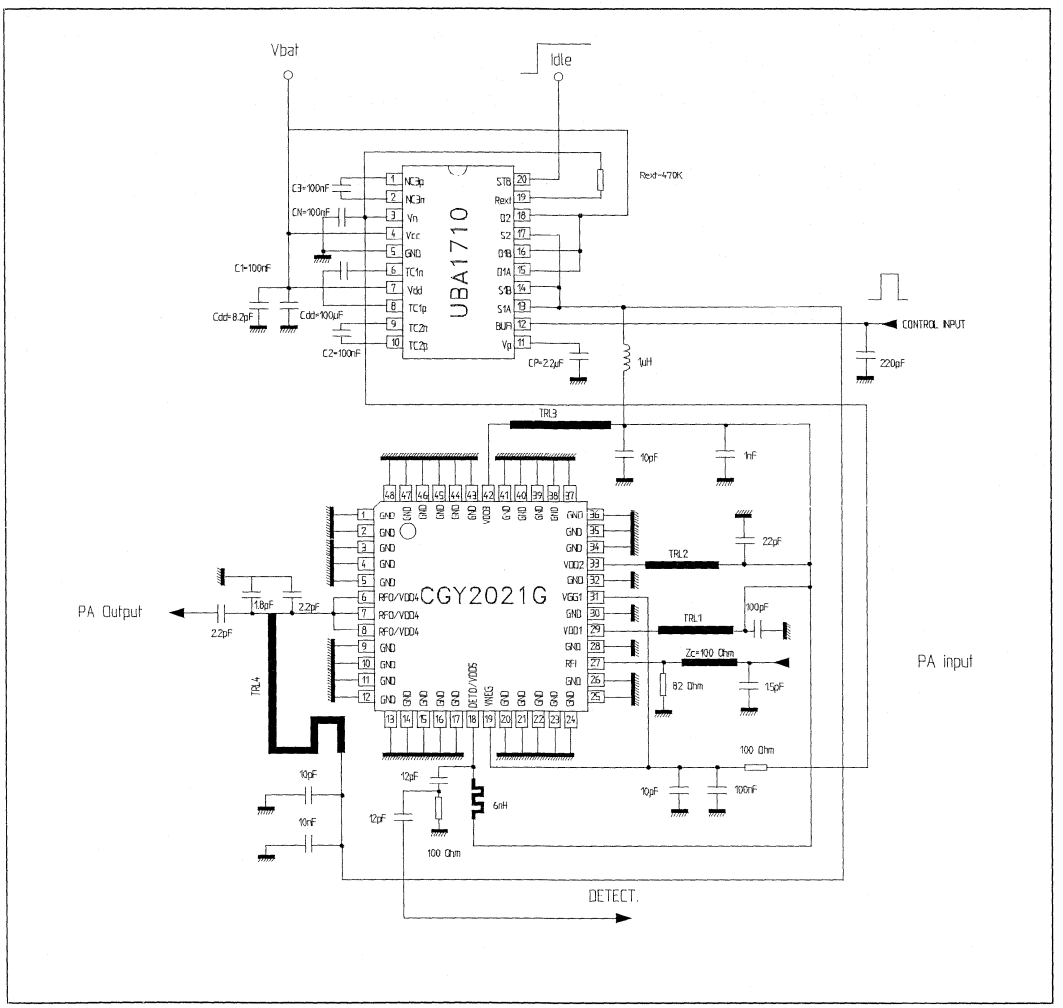

Fig. 9 Circuit diagram

6.2 Recommendations for use

When the modulator is associated with power amplifier for DCS/PCS applications , we know that the standards in use are rather difficult to fulfil ; this is particularly critical for the time and frequency masks .

Some attention must be paid with the decoupling and filtering around the UBA1710M to avoid any unwanted spurious , or noise to be amplified by the transmit path . For that reason , when looking at the circuit diagram in fig.9 ,low and high frequency decouplings are used at Vgs and Vcc (pin 7 and 4) locations as close as possible to the circuit connection . The values of these capacitors are 100 µF and 8.2 pF .

An other important decoupling is the 2.2 µF connected at the terminal pin of the voltage tripler (pin 11) . The third important filtering is the 1 µH inductor inserted between the source pins (pin 17,14,13) and the drains of the power amplifier first three stages .

All other capacitors used around the circuit for the charge pump are 100 nF .

7. PRINTED CIRCUIT BOARD LAYOUT-LIST OF COMPONENTS

7.1 Circuit layout.

The demoboard layout using the layout describes in fig. 7 is not optimised for noise and spurious ,but the aim of it is to demonstrate the dynamic behaviour of the modulator UBA1710M in association with a power amplifier CGY2021G.
The characteristics of the substrate in use for the PCB are as follows:
-substrate type:FR4 double clad
-Relative permetivity:εr=4.7
-Thickness:H=0.8mm
-Size:35x42mm

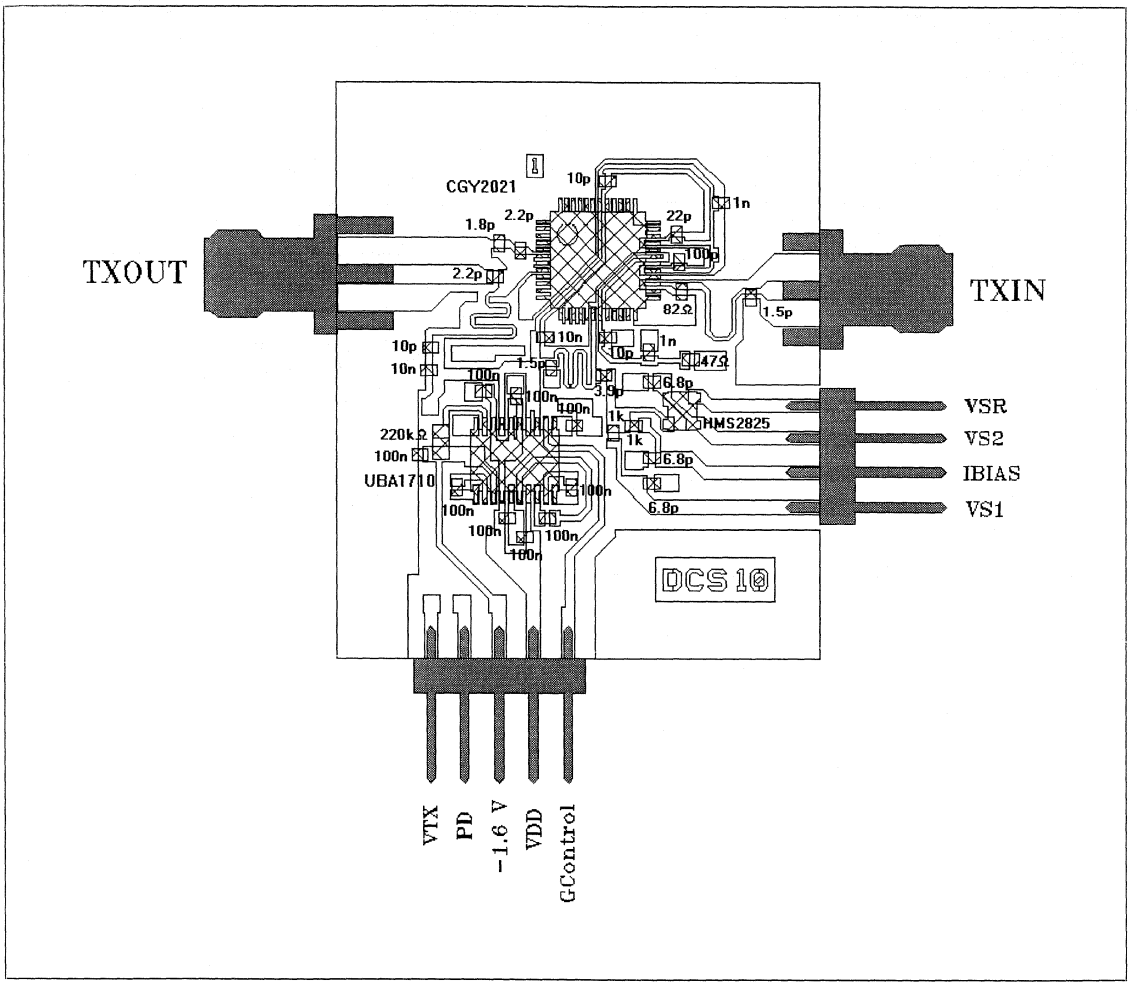

Fig. 10 Circuit layout

7.2 Part list DCS power amplifier with UBA1710

CAPACITORS (Size:0603)	
VALUE	**NUMBER**
1.5 pF	2
1.8pF	1
2.2pF	2
3.9 pF	1
6.8 pF	3
10 pF	3
22 pF	1
100 pF	1
1 nF	2
10 nF	2
100 nF	9

RESISTORS (Size:0603)	
VALUE	**NUMBER**
47 Ω	1
82 Ω	1
1kΩ	2
220kΩ	1

ACTIVE COMPONENTS	
CGY2021G	1
UBA1710M	1
HMS2825	1

8. ELECTRICAL CHARACTERISTICS

8.1 Control curve

The control curve is the one given for the association of a power and the modulator .The output power of the amplifier is plotted versus the control voltage applied to the modulator buffer input (see fig.11).

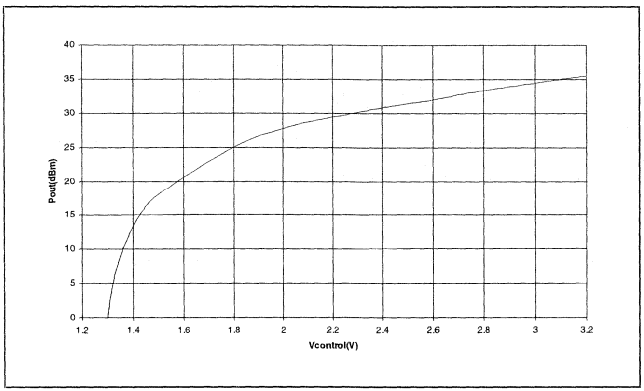

Fig. 11 Control curve

8.2 Turn-on time (tripler and negative voltage)

The turn-on time is the delay that the voltages take to establish to the nominal values when the modulator is switched on .This is an important parameter as the modulator is periodically shut down to the idle mode in order to reduce the overall consumption .These parameters are plotted in fig.12 and fig.13 .

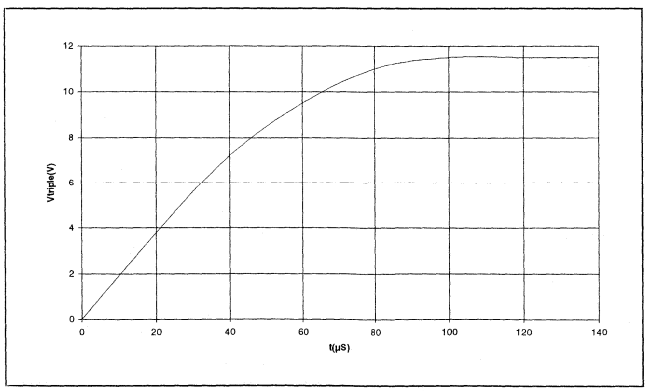

Fig. 12 Tripler turn-on time

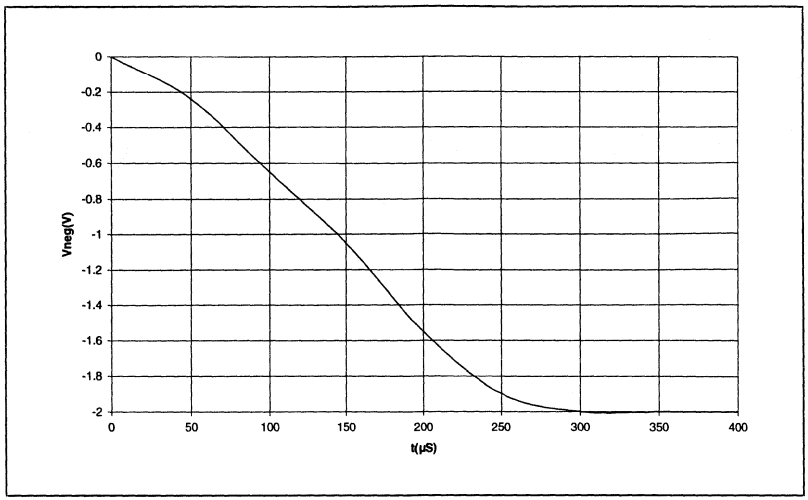

Fig. 13 Negative voltage turn-on time

8.3 Rdson versus Vcc (power MOS switches)

Rdson is also an important parameter as its value will influences the overall efficiency of the association modulator/power amplifier at the rated maximum power output level .

A plot of Rdson versus the voltage applied to the drain is shown in fig.14 and fig.15 for both MOS1 and MOS2 .

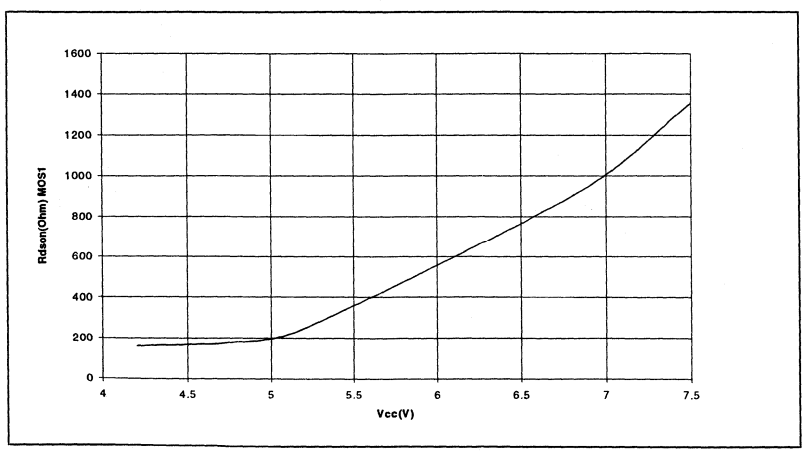

Fig. 14 MOS1 Rdson

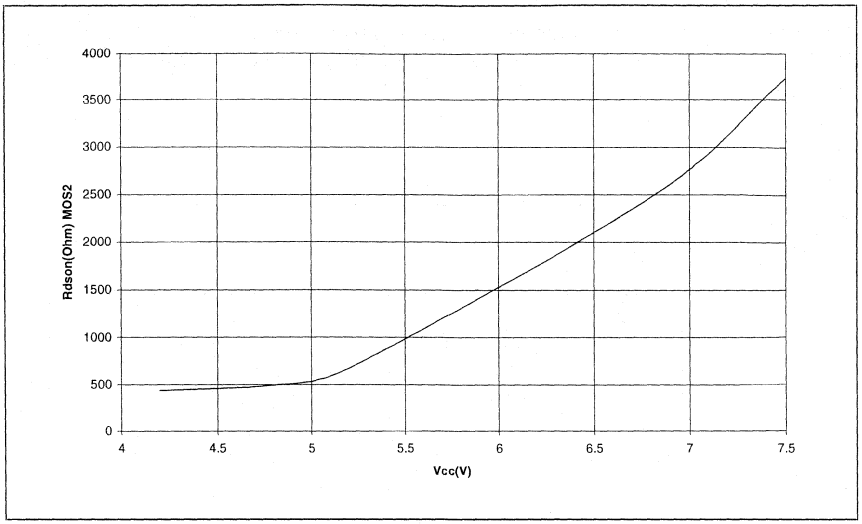

Fig. 15 MOS2 Rdson

8.4 Buffer bandwidth

The buffer bandwidth is measured between the input of the buffer and the sources of the power MOS for a given quiescent control voltage of 2.2 V .The result of this measurement is shown in fig.16 .

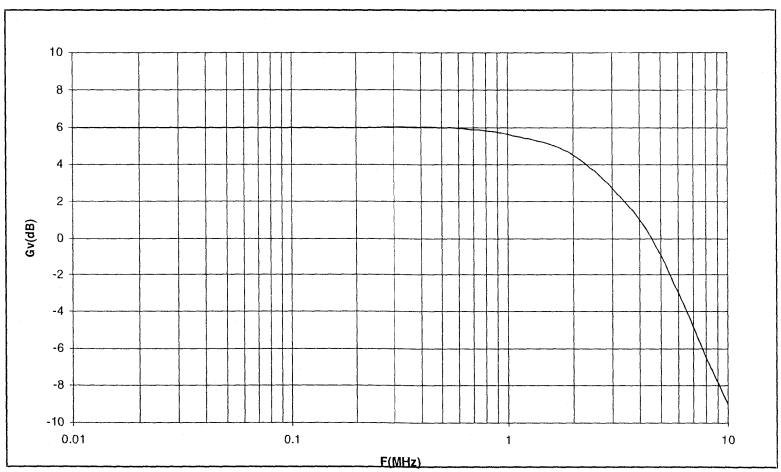

Fig. 16 Buffer bandwidth

8.5 Switching time /settling time

The switching time or settling time is characterised in terms of rise and fall times at the output port of a power amplifier using a UBA1710M as modulator .The rise/fall times are plotted versus the power level at the output of the amplifier (see fig.17) .

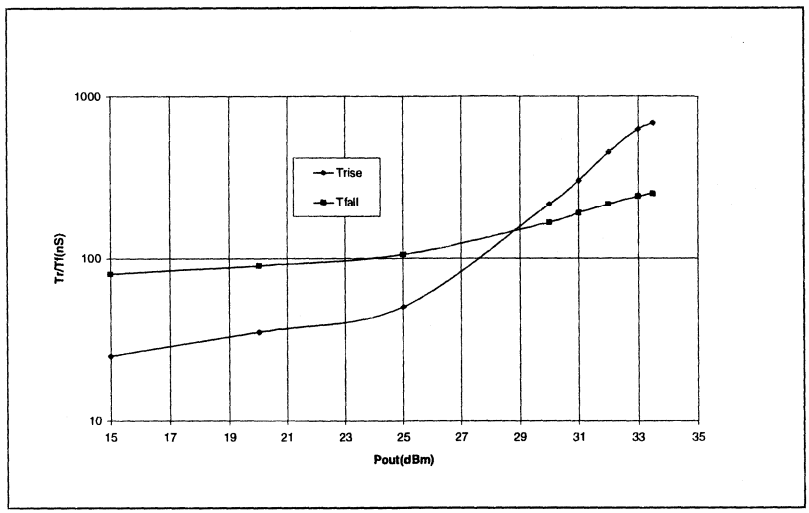

Fig. 17 Switching time/settling time

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